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UFR ISTIC

Intitulé de la thèse : Microcrystalline silicon based Thin Film Transistors fabricated on Flexible Substrate

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Introduction

Flexible electronic is a novel challenge for the electronic market and attract numerous research laboratories and industrial companies. The main applications of flexible electronic include rollable displays (LCD, OLED and EPD), RFID tags and flexible sensors. Beside low temperature compatible with flexible substrate, these applications require also high field effect mobility, good electrical stability and high flexibility of thin film transistors (TFT).

However, the conventional amorphous silicon TFT (a-Si:H TFT) used for industry TFT-LCD has well-known drawbacks as low field effect mobility and poor electrical stability. Therefore, several novel low temperature TFT technologies such as organic TFTs, metallic oxide TFTs and crystalline silicon TFTs have been emerged in order to obtain better electrical performances.

All these technologies have their advantages and drawbacks. Organic TFTs (OTFT) can have extreme flexibility and can be fabricated with several low-temperature technologies such as evaporation, spin-coating or inkjet-printing. Their mobility has been largely increased in the recent years. But TFTs are still suffered from several problems. Metallic oxide TFTs provide very high mobility. The metallic oxide semiconductors are transparent and can be deposited at low temperature. But before their commercialization, the electrical instability under the positive or negative bias stress should be carefully studied. Low temperature polycrystalline silicon (LTPS) TFTs have high mobility and good electrical stability, but laser crystallization increases their fabrication cost and limits their uniformity.

The present work focuses on the microcrystalline silicon technology. In IETR laboratory, microcrystalline silicon technology on glass and plastic substrates has been developed. The deposition has been performed at a temperature lower than 180 °C in order to be compatible with plastic substrate such as PEN. These flexible and transparent substrates are provided by DuPont Teijin Film. Precedent works in IETR have already demonstrated the possibility to fabricate microcrystalline silicon TFTs on this PEN substrate. This thesis deals with the improvement of field effect mobility, electrical stability and mechanical flexibility of these TFTs. The organization of this thesis is shown below:

In the first chapter, the state-of-the-art for flexible electronic applications will be introduced. Flexible displays, RFID tags and flexible sensors will be described. Afterwards,

different flexible substrates used for these applications will be presented. Their properties such as maximum process temperature, transparency and mechanical flexibility will be detailed. Finally, different low-temperature TFT technologies, including organic TFT, metallic oxide TFT and silicon TFT, will be presented by discussing their semiconducting principles, electrical performances and limitations.

In the second chapter, the fabrication process of microcrystalline silicon TFTs will be described. First, the technologies of thin film materials (especially for undoped microcrystalline silicon) deposition and characterization will be detailed. Afterwards, an introduction of microcrystalline silicon TFTs technology will be given. This introduction includes the fabrication steps, the basic working principles and characterization of TFTs. and will be finished by the electrical characteristics of microcrystalline silicon TFTs on glass and on plastic substrate presented by previous works in IETR.

Before the third and fourth chapter, a state-of-the-art and problematic of microcrystalline silicon TFT technology will be presented. This short introduction will summarize the previous works on flexible microcrystalline silicon TFT and give the motivation of the studies in the third and fourth chapter.

In the third chapter, electrical stability and mechanical flexibility of microcrystalline silicon TFTs will be studied. Firstly, the TFTs will be fabricated on glass substrate. They will be electrically stressed under different gate voltages at different temperatures in order to explain the mechanism of electrical characteristics shift of TFTs. Secondly, the TFTs will be fabricated on PEN substrate. They will be electrically characterized during mechanical bending, for both tension and compression for different curvature radii. The variation of their electrical characteristics under mechanical bending will be studied and discussed. The minimum curvature radius of TFTs will be also determined in this part. Moreover, the method to obtain lowest possible curvature radius of TFTs will be discussed in the end of this chapter.

In the fourth chapter, the microcrystalline silicon TFTs will be fabricated with different gate insulator materials in order to increase field effect mobility of TFTs. The gate insulator materials include silicon oxide deposited by sputtering and ECR-CVD, alumina deposited by

thermal ALD and silicon nitride deposited by PECVD. Electrical characteristics of TFTs using these gate insulators will be presented and discussed. The possibility of increasing field effect mobility of microcrystalline silicon TFTs to at least 5 cm^2/Vs, which is the mobility needed for AMOLED, without sacrificing electrical stability, will be discussed at the end of this chapter.

Chapter 1: Microcrystalline silicon thin film transistors: Applications and technologies

1. Introduction

The display industry has benefited from a large development in the past 20 years. Today's display devices trend to be more bright, flat, with high resolution and efficient. The flexible displays fabricated on the plastic or paper substrate, turned out to be a very interesting target for the future. Moreover, the other applications of flexible electronics, such as RFID and flexible sensors, have attracted large attention of numerous research laboratories supported by industries. To fabricate electronic devices on flexible substrate which could not be maintained at high temperature, there are 2 different types of technologies. The first one is to fabricate devices on glass or silicon substrate and then transfer to flexible one (paper, plastic). For this method, the low temperature fabrication is not necessary but the cost is higher. The second one is to fabricate directly on the flexible substrate. For these technologies, a low temperature thin film transistor (TFT) technology compatible with such substrate, without sacrificing electrical or mechanical performance, is needed. With this background, several novel low temperature TFT technologies such as organic TFTs, metallic oxide TFTs and silicon TFTs have been emerged envisaging the challenge of commercialization, not only for flexible displays, but also for the other applications of flexible electronics. These TFT technologies have different mechanisms, performances, advantages and drawbacks. In this chapter, the applications and the properties of such low temperature TFT technologies are introduced.

2. Low temperature TFTs for display applications

2.1 TFTs for liquid crystal display

The TFT LCDs have superiors performances compared to CRT (cathode ray tube) displays in terms of flatness, lightness, and low power consumption. LCD has replaced CRT and became the leading display technology in recent year .

The configuration of a LCD display panel is shown in figure 1.1 [1]. The Liquid crystal is deposited between the two polarization panels, one is covered by uniform conductive layer while another is covered by the TFT matrix. The TFT matrix containing lines and columns

plays an important role in the LCD operation. The TFTs are located between each line and column respectively to control the LC pixel. The TFT is also connected with a capacitance. So the role of TFT is: (1) in the on state of TFT, data current goes though the TFT to drive the liquid crystal of each pixel. (2) In the off state of TFT, the voltage applied on the liquid crystal in the passing state is kept by the capacitor until all the pixels are addressed. Figure 1.2 shows typical structure and manufacturing process of TFT matrix for LCD display [2].

To drive a LCD display panel, the voltages should be applied on the lines and columns following a regular timing. As shown in Figure 1.3, when a positive voltage (should be superior to the threshold voltage of TFT) is applied to the gate electrode, which is connected to the scan line, TFT will be turned on. Then the data voltage can be delivered from data line to LC and storage capacitor. On the other hand, if there is no voltage applied to the scan line, the TFTs are in their blocked state. The charges kept in the capacitors, which are connected with the drain of TFTs, can make a conservation of precedent pixel image.

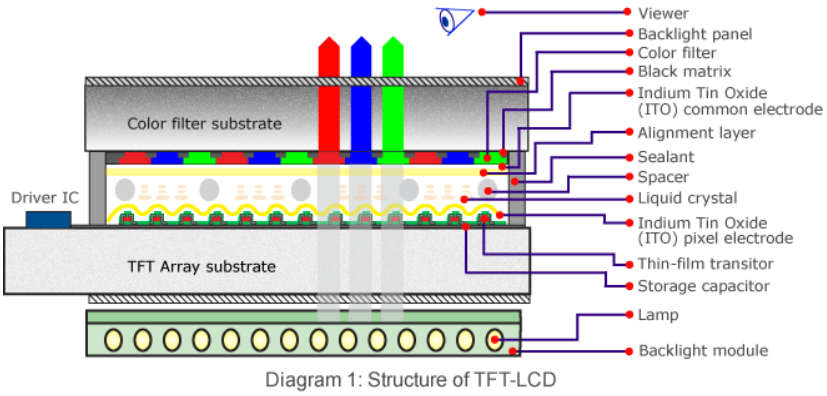


Figure 1.1: Structure of TFT-LCD [1]

For high resolution or large area LCD displays, high mobility of TFT is needed to maintain the display quality because of the short response time required for each pixel. With high mobility, charge carriers can move easily in the device to make a reduction of delay time of pixel refreshing. High stability and good uniformity are also demanded for the display long-term reliability and for the large size display, respectively.

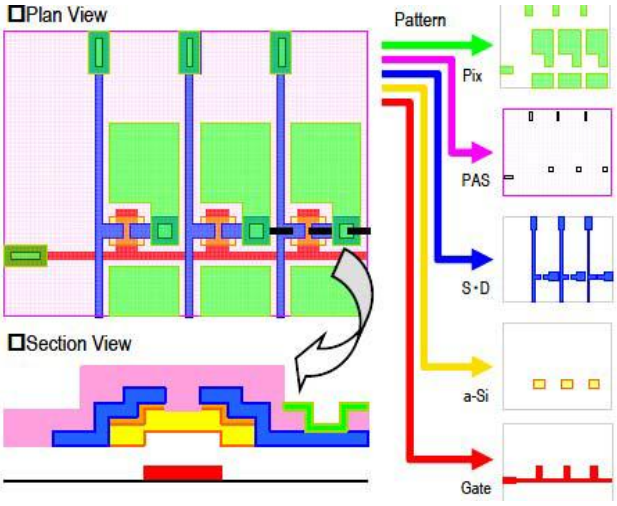


Figure 1.2: Typical TFT matrix structure and manufacturing process [2]

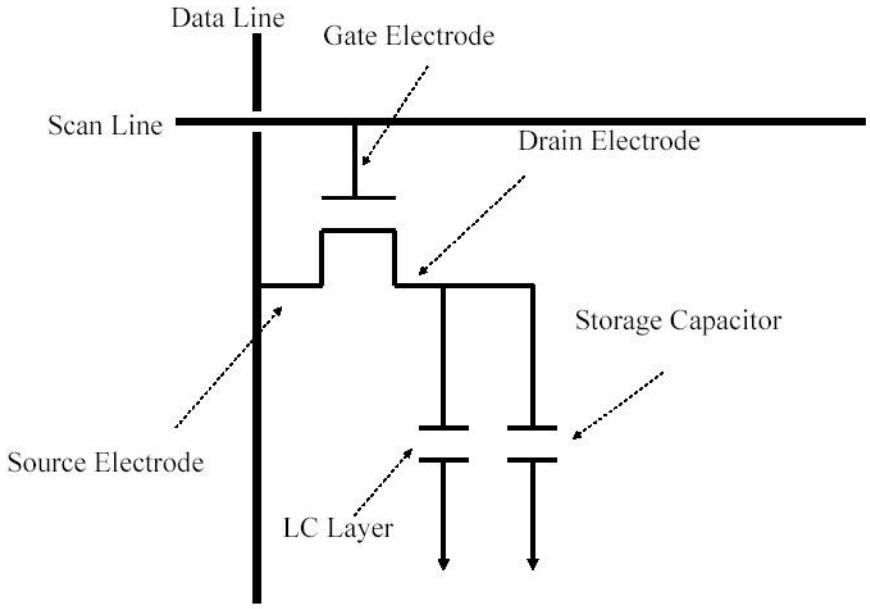


Figure 1.3 Pixel circuit for TFT-LCD [3]

Today, most of industrial productions of TFT-LCD displays are based on hydrogenated amorphous silicon (a-Si:H). They are inexpensive, reliable, and can be fabricated at low temperature [4]. However, the application of a-Si:H TFTs in the large area devices is limited by their low carrier mobility and their threshold voltage shift. Therefore, alternative TFT technologies with higher carrier mobility and electrical stability are needed. In the recent years, organic TFT, metallic oxide TFT, low temperature poly-silicon TFT (LTPS TFT) and

microcrystalline silicon TFT (μc-Si TFT) technologies have been developed. Their features and advantages will be detailed thereafter.

2.2 TFTs for OLED

With their high brightness, low power consumption, wide viewing angle and so on, OLEDs make themselves a leading next-generation technology compared to the other flat panel displays [5]. Moreover, an active-matrix OLED (AMOLED) has lower power consumption and faster refresh rate than other driving system.

The structure of OLED unite is shown in figure 1.4 [6]. The organic material is sandwiched between two conductors (anode and cathode). When a voltage is applied on the electrodes, electrons are injected from cathode and holes are injected from anode. The recombination of electron-hole is taken place into the emissive layer and release energy to produce the light.

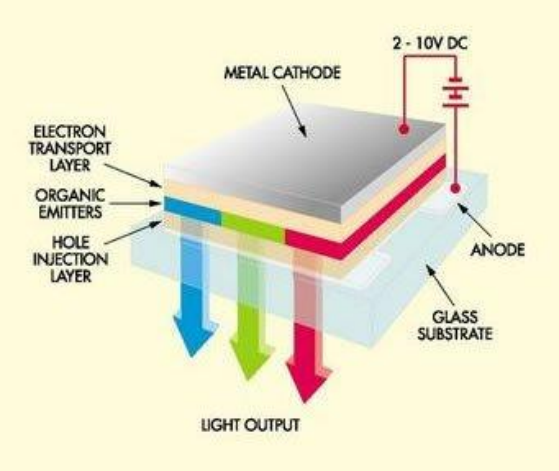


Figure 1.4: OLED unit pixel structure [6]

Since the luminance of OLED is proportional to the driving current, two TFTs at least are needed in order to supply a constant current during each frame period. Figure 1.5 shows a conventional pixel structure [7]. One transistor (T1) is switched on to charge a capacitor and the other (T2) deliver a constant current from the capacitance voltage to illuminate the pixel. In most of researches, more complicated pixel circuits are always designed using 3 TFTs, 4 TFTs and even more. (Figure 1.6) [8]. The TFT should have long-term stability under bias

stress and ambient environment. Electrical instability could lead to a threshold voltage shift that causes a reduction in the pixel luminance. In addition, the high mobility of TFT is also needed to realize a large size OLED display.

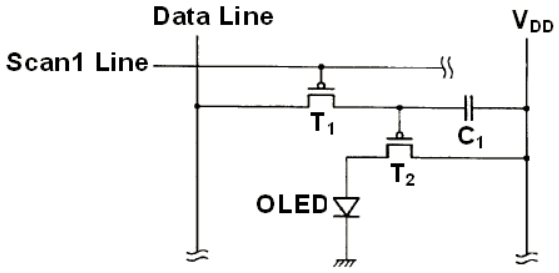


Figure 1.5: AMOLED conventional 2-TFTs pixel structure [7]

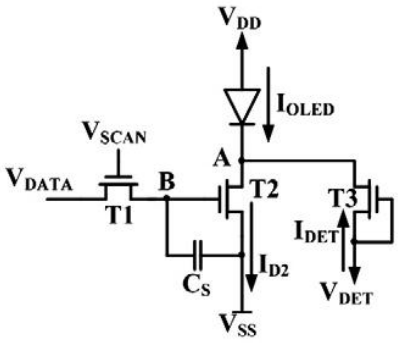


Figure 1.6: A 3-TFTs OLED pixel structure [8]

The a-Si:H TFT AMOLED suffers from their low carrier mobility and high threshold voltage shift which are related to the display degradation. One method to solve this problem is to use more complicated configurations. This way leads to an increase of electronics devices surface. The aperture ratio, which means the ratio of electronic device surface to total display surface, is thus sacrificed. In addition, an alternative technology with higher mobility and mainly better stability are needed. The µc-Si TFT could be an alternative technology. Indeed, we demonstrated the possibility to use µc-Si TFT in an AMOLED circuit with Thomson R&D France [9].

2.3 Quantum-dot light emitting display (QLED)

Since the first report in 1994 [10], quantum-dot LEDs have attracted much attention in the past years. Thanks to their unique properties, such as solution process [11], low energy consummation, compatibility with flexible substrate, tunable emitting wavelength over the entire visible spectrum [12] and improved color saturation, the quantum-dot LEDs become an interesting candidate for the application of thin film displays.

The mechanisms of quantum-dot light emitting diode (QLED) and OLED are very closed. The only difference is the material used as the active luminescent layer. For OLED display, organic material is used as the luminescent layer. For the QLED display, the luminescent layer is made of particularly treated II- VI or III-V component based semiconductor. Figure 1.7 shows an example of a blue QLED device.

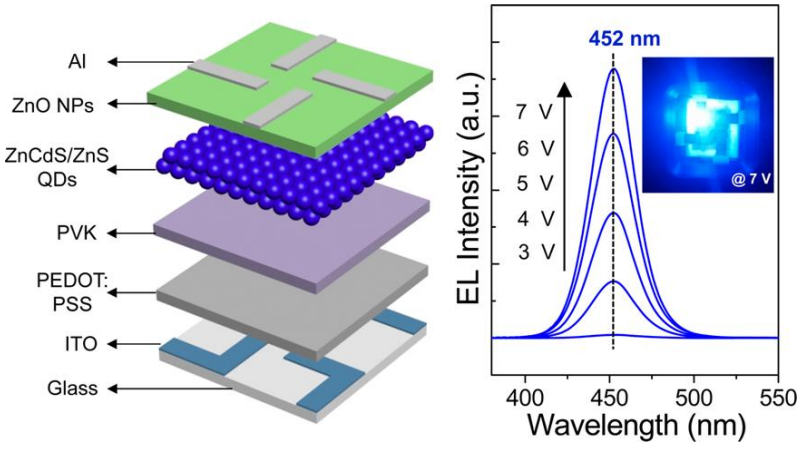


Figure 1.7: Structure of blue quantum-dot LED [13]

In this structure, the ZnCdS/Zns quantum dot (QDs) is used as active luminescent layer. The ZnO NPs, PVK and PEDOT:PSS are used as electron transport , hole transport and hole injection layer, respectively. In the other report, CdSe/Cds QDs [14] and ZnCdSeS QDs [11] have been used as QDs luminescent layer. In the common QDs fabrications, different QDs size can be obtained by controlling the reaction temperature and time. Moreover, the band-gap of QDs is governed by their size. Therefore, size-controlled tunable light emitting can be achieved. This might be the most interesting property of QLED device.

Since their first report in 1994 [10], the light emitting efficiency of QLEDs has been increased by a factor of more than 1800, from less than 0.01% to around 18% [Yasuhiro Shirasaki Nature Photonics 7 13-23 (2013)], which are comparable to those of OLEDs. The major challenge is their lifetime. Today's QLEDs lifetime at the initial brightness can reach 1,000 hours while more than 10,000 hours is needed for displays.

The Southeast University of Nanjing, China, has begun their studies on QLEDs very recently. They developed an all solution-processed method to fabricate blue and green QLEDs by optimizing the thickness of all the electron transport, the hole transport and the hole injection layers [11]. The collaboration between Southeast University and University of Rennes 1gives us a possibility to carry out on a novel TFT application: the QLED display addressed by microcrystalline silicon TFT fabricated at low temperature.

3 TFTs for Flexible electronics

3.1 Flexible displays

The flexible displays have been extensively studied by a large number of electronics manufacturers to transfer this concept to the market in the recent years. A lot of flexible display production has begun to enter into our horizon. In 2005, Arizona State University created a flexible display center by receiving 43.5 million dollars from Army Research Lab. With Hewlett Packard, their partnership, they have presented a flexible e-paper [15]. In 2010, Samsung has begun to develop a 4.5-inch flexible AMOLED and try to start mass production of this kind of displays. On 8 October 2013, they announced the world's first flexible-display phone that carries a 5.7-inch touchscreen with a resolution of 1080×1092 [16]. However, this kind of screen cannot be strictly seen as 'flexible', but merely 'bendable' displays. In the underside of figure 1.8 is the 4.1-inch rollable OLED displays reported by Sony [17].

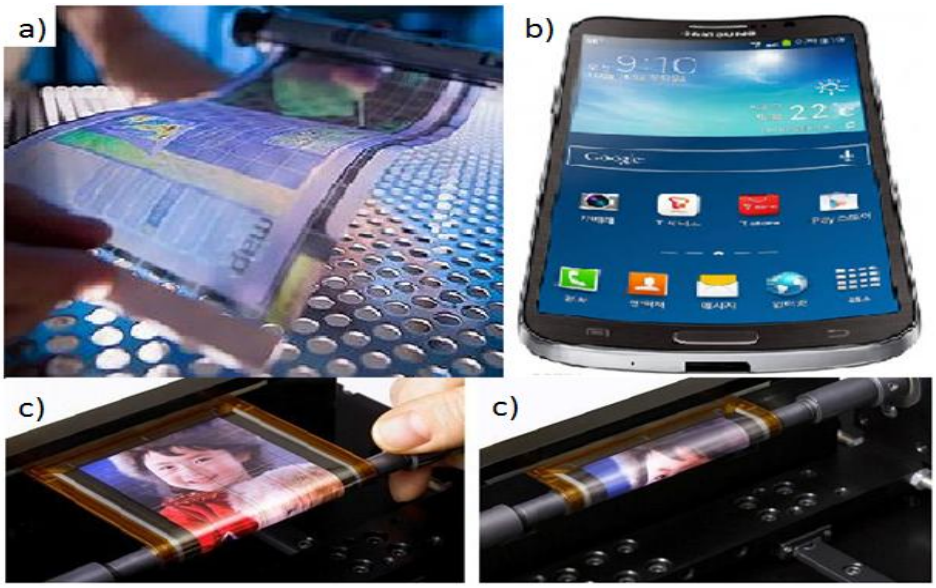


Figure 1.8: Applications of flexible displays. a) Electronic paper by HP and ASU [15]. b) Smart phone by Samsung [16]. c) Rollable screen by Sony [17].

The development of low temperature TFT is also a key issue for the progress of flexible displays. The low temperature fabrication makes plastics possible as substrate of flexible display. In many research laboratories, flexible displays using low temperature fabricated TFT have been reported. For flexible OLED displays, the organic TFTs and silicon TFTs have been used since more than 10 years [18, 19]. These flexible displays present matrix with low pixel resolutions. Recently, as the device fabrication technologies have been well developed, some research laboratories demonstrate their flexible TFT with higher resolution [20, 21]. The electrical and mechanical stabilities of these TFTs are also improved. Indeed, the mobility and the flexibility of TFTs, especially for organic TFTs, have been largely improved based on numerous efforts of researchers.

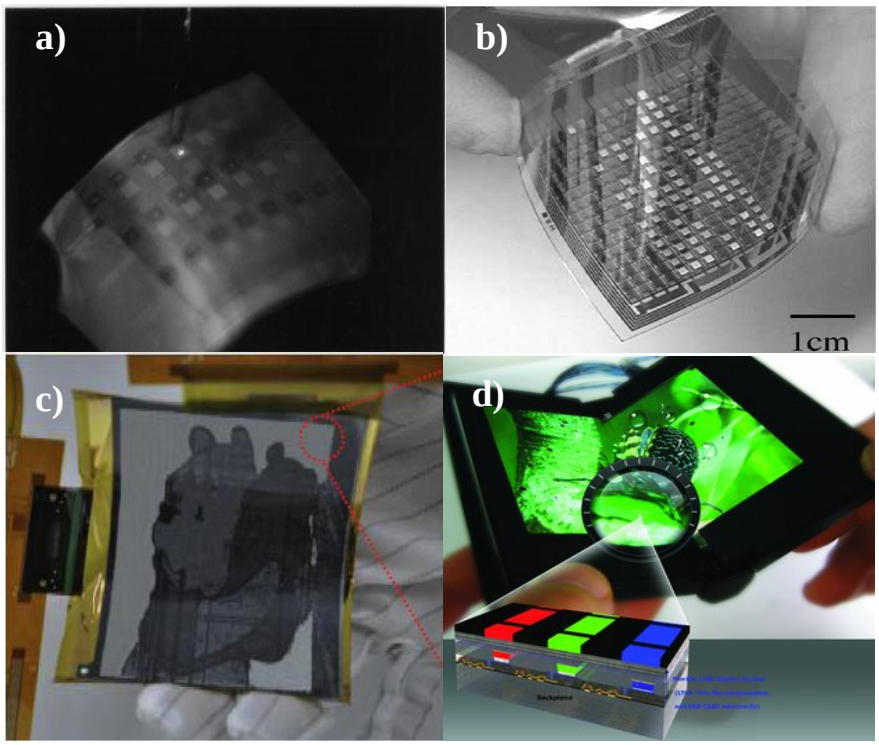


Figure 1.9 Flexible displays in research laboratories: a) OLED using a-Si:H TFTs on metal foil substrate [18], b) OLED using bottom gate OTFTs on plastic substrate [19], c) EPD using solution-processed OTFT [20], d) Flexible OLED device [21].

3.2 Flexible sensors

The flexible sensors are also important in flexible electronics. The main flexible sensors include the bio-chemical sensors, the medical patches, the artificial skin and other as temperature, pH and gas sensors. A research group has developed a flexible chemical sensor [22, 23]. This sensor is based on bottom gated TFT using SWNTs (Single-Wall Carbon Nanotube) as active layer. The sensor is stable when functioned in the water. The high sensitivity of the sensor permits the detection of poison in water or explosive compounds such as TNT (Figure 1.10 a)). Another application field is the artificial skin. In 2013, C. Wang et al [24] presented a user-interactive electronic sensor. During their experiment, finger pressure upon surface of sample can be detected and visualized by illuminating OLED pixel on the opposite side of sample. The light intensity corresponds with the pressure. A

research group at Tokyo University has developed a matrix based on organic TFT sensors [25]. This tactile sensor can be used for health care and monitoring (Figure 1.10 c). The organic TFTs used for the sensor matrix has extreme flexibility (Figure 1.10 d). They maintain stable function even after some extreme bending conditions such as bending curvature radius of 5µm within the active area and tensile strain of 233%.

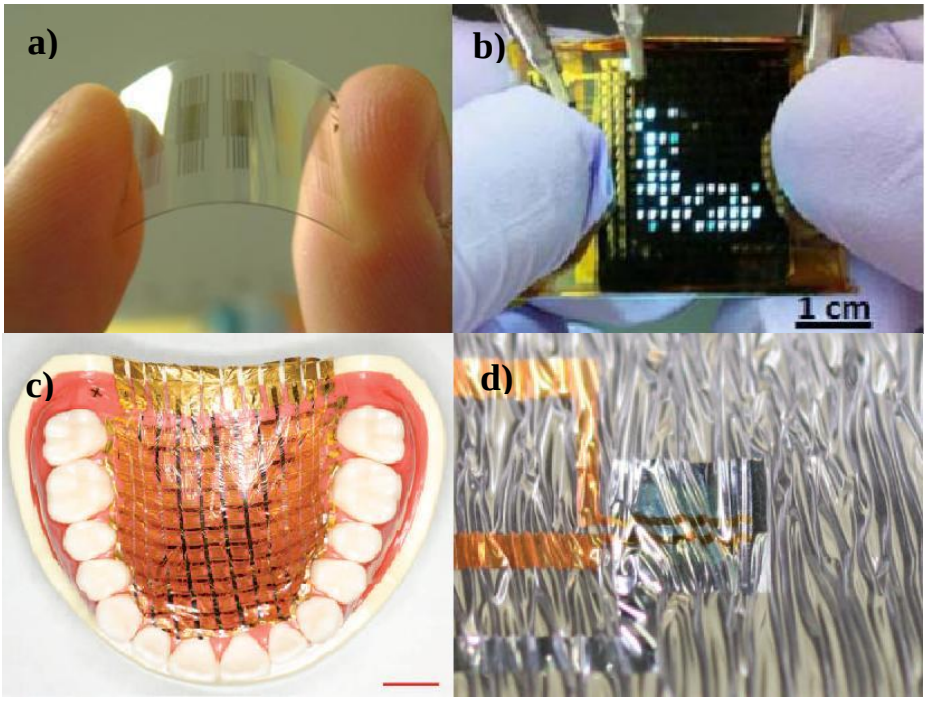


Figure 1.10 Different types of flexible sensors: a) chemical compound sensor [22], b) user-interactive electronic skin [24], c) and d) ultra-flexible organic TFT sensor [25].

3.3 RFID tags

The RFID tag (Radio Frequency Identification) is a wireless system used for the identification with certain distance using electromagnetic signal. The data of an item or an animal can be saved inside the RFID tag with electromagnetic format. Then a special reader will be used to identify it. The RFID is used like a barcode but the RFID is not necessary to be in the sight of the reader.

Now, two types of RFID exist: active RFID and passive RFID. The active RFID has a local power source like a battery, which supplies the power consummation for reading or

writing data. Therefore, the data of an active RFID can be modified. On the other hand, the power source, which is need to be inside the active RFID, makes the flexible devices more expensive.

The second type, passive RFID, need to be powered by electromagnetic fields produced by or near the reader. The battery-free passive RFID is possible to be flexible. Figure 1.11 presents simplified schema of a RFID system. This system is composed by 3 parts: RF antenna, rectifier and CMOS circuit. The RF antenna is used for the communication between reader and RFID by sending or receiving RF signal. Then the AC signal is converted to DC signal by rectifier. The CMOS circuit, which has some oscillators and logic gates, will save the converted DC signal.

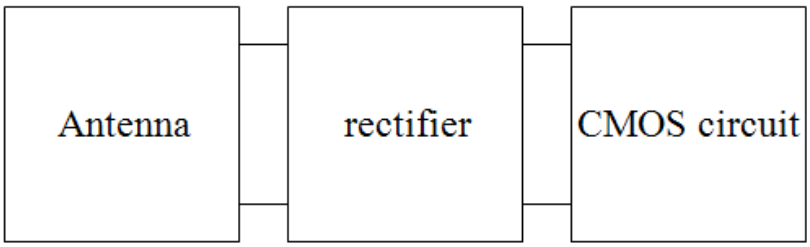


Figure 1.11 Simplified schema of RFID

Recently W. Huang *et al* [26] integrated RFID and flexible sensor technologies by realizing a passive RF pH-sensor. The flexible pH-sensor tag can measure the pH value in food and the data can be sent to a reader (computer terminal) by RF technology. This kind of devices provides an open way for the researchers to further exploration of novel and interesting applications based on flexible electronics.

4. Different flexible substrates

There are mainly 4 types of different flexible substrates for the flexible electronics devices: thin glass, stainless steel foil, plastic and paper. The choice of substrate is depending on the application. For example, the flexible displays require the substrate to be transparent. For the flexible display applications, the surface quality of substrate is also needed to be sufficient.

On the other hand, the low-cost substrate is needed for some disposal electronics. To choose a flexible substrate, these factors are generally considered:

- The maximum temperature that substrate can hold.
- The thermal expansion coefficient of substrate
- The transparency
- The cost
- The surface roughness
- The robustness with environment

4.1 The thin glass

The glass will be flexible when its thickness reduced less than 200 μm [27]. Some commercialized thin glass's thickness can be reduced until 25 μm [28]. The main advantages of thin glass as flexible substrate include the quasi-perfect surface with roughness normally less than 0.5 nm, the high optical transparency, the high process temperature without thermal deformation, the impermeability of water or oxygen and the high chemical resistance. Benefiting from these properties, the TFTs or LCD and OLED can be fabricated on thin glass substrate with high performances. For example, S. M. Garner *et al* [29] present a high-quality and high-resolution electrophoretic display driven by organic TFT on flexible glass substrate. Benefit from the high quality of glass surface, the organic TFTs are electrically stable. S. Hoehla *et al* [30] use 75-μm-thick flexible glass for an active matrix LCD display. The TFTs have been directly fabricated on the glass substrate without degradation compared to the TFTs fabricated on thicker glass. On the other hand, the main drawback of thin glass substrate is its fragility and the high fabrication cost.

4.2 Flexible stainless steel foil

The flexible stainless steel foils have normally a thickness around 100 μm. They are impermeable to oxygen and water. They can be processed at high temperature without deformation. They also offer high mechanical strength. Therefore, the TFTs fabricated on flexible stainless steel foil are suitable for some high performance and/or large area

applications. For example, T. Serikawa and F. Omata [31] reported poly-Si TFTs on flexible stainless steel foil. The silicon is crystallized by excimer laser and has high mobility of 106 cm^2/Vs. D. Jin *et al* [32] demonstrated a very thin AMOLED display based on LTPS TFT which has a mobility of 71.2 cm^2/Vs. High quality display images have been shown in this work. The main drawback of flexible stainless steel foil is its opacity, the need of encapsulation layer due to its conducting nature and the high surface roughness. The opacity restricts its applications in certain situation in which transparency of substrate is required. The need of encapsulation or planarization layer limits the maximum temperature of process. Moreover, the fabrication cost of flexible stainless steel is high.

4.3 Paper substrate

The paper is human-friendly, low-cost and disposable material. Recently the paper begins to be employed as substrate for flexible electronics including flexible display, flexible sensor and RFID [33]. The paper is a good candidate for some low-cost and disposable applications. The main drawbacks of paper for flexible electronics include the opacity, the high surface roughness and the weak chemical resistance. The printing technology might be the best way to use paper as substrate for flexible electronics because it can reduce the cost compared with conventional photolithograph process. Different printing technologies exist in the research area, including inkjet printing, screen printing and gravure cylinder, etc. Unfortunately the printing technologies are not matured yet. So the electronics on paper substrate have still large challenge to be considered in a mass-production.

4.4 Plastics

The plastics present better flexibility compared to thin glass and flexible stainless steel foil. The mainly used plastics for flexible electronics are PET, PEN and Kapton. The maximum process temperatures for PET, PEN and Kapton are 150°C, 180°C and 400°C, respectively. These plastics present high deformation under high temperature process because of their high thermal expansion coefficient. For example, the PEN Q65FA produced by DuPont Teijin Film has deformation of 0.2% after heating at 200 °C during 10 minutes

[34]. This deformation causes alignment error during the photolithography masking process. Therefore, the maximum temperature during process using these substrates should be well controlled.

The PET and PEN substrates are transparent with optical transparency higher than 80% for visible light, while the Kapton is yellow-colored. The water and oxygen permeability of Kapton is also higher than that of PET and PEN. For this reason, an encapsulation layer is probably necessary for their application.

4.5 Conclusion

As a conclusion of all flexible substrates, the Table 1.1 gives the material properties of substrates and the Table 1.2 summarizes the main advantages and drawbacks of the 4 types of flexible substrate.

Properties	Thin glass	Stainless steel foil	Paper	Kapton	PEN	PET
Maximum process temperature (°C)	>600°C	800°C	Very low	400	180	150
Transparency (%)	>91	0	0	Yellow-colored	>80	>80
Young's module (GPa)	70	200	10-20	2.5	6.5	5.3
Chemical resistance	Good	good	weak	good	good	weak
Impermeability	Good	good	weak	weak	weak	weak
Planarization	No	Yes	No	No	No	No

Table 1.1 Material properties of mentioned flexible substrates for flexible electronics

Substrates	Advantages	Drawbacks
Thin glass	High transparency, low surface roughness, high process temperature, strong chemical resistance and water, oxygen impermeability, low thermal expansion coefficient.	Expensive, fragile
Stainless steel foil	High process temperature, strong chemical resistance and water, oxygen impermeability, robust mechanical strength, low thermal expansion coefficient.	Opacity, high surface roughness, expensive.
Paper	Low-cost, disposable, low thermal expansion coefficient, flexibility.	Opacity, high surface roughness, low process temperature, low chemical resistance, high water and oxygen permeability
Plastic	Low-cost, transparency, flexibility.	High thermal expansion coefficient, low process Temperature

Table 1.2 Advantages and drawbacks of mentioned flexible substrate for flexible electronics

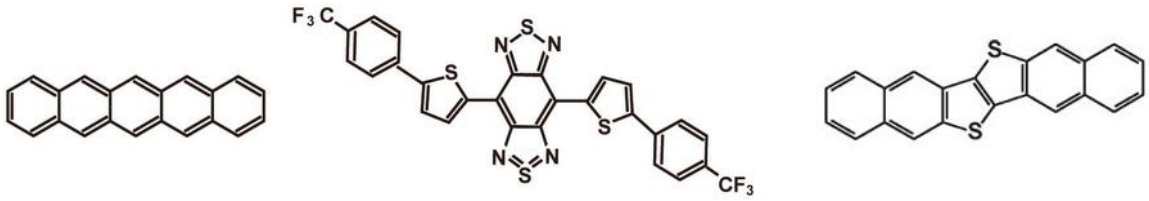
5. State-of-the-arts of low temperature TFTs

As mentioned before, flexible electronics can be fabricated by two technologies: 1) directly fabricate on flexible substrate, and 2) fabricate on glass or silicon substrate and then transfer to flexible one. For the 1st technology which has lower cost, the devices should be fabricated at a low temperature compatible with flexible substrate. This section will describe the state-of-the-art of such low temperature fabricated TFTs using different semiconductors.

5.1 Organic thin film transistors

Recently organic TFT has been largely studied because of their advantages such as low fabrication cost, light weight, low fabrication temperature and mechanical flexibility that made them a promising candidate for the applications of large area and/or flexible displays. They have been drastically improved in the last 20 years. Before 1990, the typical mobility value was 10^{-5}-10^{-3}cm²/V.s [35, 36]. Recently, it has been demonstrated field effect mobility as high as 2.8 cm²/V.s [37]. A high resolution AMLCD driven by organic TFTs has also been reported, in which the organic TFTs show an average mobility of 0.3cm²/V.s and good uniformity [38].

Obviously, to make OTFT, the active layer of TFT should be made of organic semiconductor. A key role to get high mobility is the use of thin organic films with high structural order as active layer [39]. Therefore, many organic materials have been researched such as pentacene, FPTBBT, DNTT, poly (3-hexylthiophene) (P3HT), Poly (3-octylthiophene) (P3OT) and C60. Figure 1.12 shows some structures of organic materials used as transistor active layers.



a) b) c)

Figure1.12: Structure of some organic semiconductors used as active layer of TFT: a) Pentacene, b) FPTBBT, c) DNTT

Among these materials, pentacene, a p-type channel, shows the best TFT performance. There are two methods to fabricate pentacene, vacuum deposition and solution-based deposition. Vacuum thermal deposition has some advantages such as solvent-free deposition and compatibility with well-established OTFT technology. The solution-processed OTFT

has attracted much attention thanks to their low-cost non-vacuum process ability. Among several solution-process methods, inkjet-printing technology is one of the most promising candidates because the patterns with size of tens-of-micrometers can be directly printed without any photomasks. The inkjet-printing technology is studied for various applications such as active-matrix display, radio-frequency identification and sensor [40]. Moreover, a vapor-inkjet method which combines the benefits of jet printing and thermal evaporation has been demonstrated [41]. Today, the mobility of solution-processed OTFT can be around 1 $cm^2/V.s$. [42]

Beside of p-type channel material like pentacene, the enhancement of n-type channel OTFT is especially needed to enable OTFT-based technologies. N-channel OTFT exhibiting high mobility (2-3cm^2/V s) and exceptional stability has been reported [43].

The materials for OTFT dielectric are also studied. These materials need high resistivity to avoid too high leakage current and high dielectric constant to have enough capacitance [40]. There are some important materials for OTFT dielectric: Thermal SiO_2 polymide, PMMA (polymethylmethacrylate), Al_2O_3, and SOG (spin on glass). In addition, meeting the requirements of flexible displays using plastic substrate, gate insulator should be organic to reduce the thermal stress induced by the difference in the thermal expansion coefficient between TFT organic semiconductor and substrate [40].

The source/drain(S/D) contact should also be optimized to enhance the OTFT performance. Changhun Yun et al [42] have optimized their OTFT by using a reverse offset printing (ROP) method instead of vacuum thermal evaporation to enhance the S/D contact. In their work, high work function and small dipole of pentacene-metal interface of ROP-based Ag lead to a low interfacial energy barrier.

In spite of their advantages, the OTFTs suffer from some limitations. Firstly, the organic semiconductors or organic gate insulators that have good performances are very expensive. For example, the N1200 produced by Polyera corporation (organic semiconductor) and the Cytop (organic gate insulator). Secondly, the OTFTs using organic gate insulator are usually operated under high V_{DS} and have high threshold voltage. Thus, the power consumption is increased. Finally, the instability of OTFTs such as the degradation with environmental

conditions after long duration should be explored and optimized. These instabilities maybe due to the chemical structure of OTFT compound [40]. Bias and thermal stress stable OTFT devices are needed [43].

5.2 Oxide semiconductor thin film transistors

TFTs fabricated using oxide semiconductors exhibit good mobility as high as 5 to 50 cm^2/Vs. Except the high mobility, this relative new class of materials possesses other advantages such as: 1) amorphous crystal structure can make a good uniformity and easier fabrication; 2) low-temperature processing which is compatible with flexible substrate; and 3) transparency in visible region. These make them a good candidate for the AMLCD, AMOLED and other large-area electronics applications.

Another unique feature of oxide semiconductor TFT is that they can have large electron mobility even in the amorphous structure, while amorphous silicon exhibits much poor mobility compared with crystallized silicon. This is attributed to the difference between covalent and ionic semiconductors. For covalent semiconductors like silicon, the chemical bonds are made of sp^3 or p orbitals that have strong spatial directivity. In contrast, the transport properties of the ionic semiconductors that have the s orbitals to form the ionic bonds are not affected largely by amorphous structure. That is why the amorphous oxide semiconductors (AOSs) show large moblities even in amorphous structure.

Normally, Zn-based oxide materials have been used to make TFT or transparent TFT [44], including In_2O_3, SnO_2, InGaZnO (IGZO), ZnSnO (ZTO), ZnInO (ZIO), SnGaZnO (TGZO), InGaO (IGO), ZnInSnO (ZITO) and ZnON. All of these materials are n-type. Among these materials, IGZO is one of the most promising materials to make TFT for display application because the IGZO-TFT combines good uniformity and high mobility. In fact, the incorporation of Ga into an In-rich IGZO film leads to obtain stable TFTs. Moreover, it is reported that the mobility degradation along with the channel length, which was a disadvantage of a-Si:H TFTs, is not observed for short channel a-IGZO TFTs. This may benefit the a-IGZO TFTs in the area of ‘retina-like’ AM-LCD, which means higher pixel density [45]. Besides IGZO, the other multi-component oxide (MCO) TFT shows also

promising performances. For example, Eugene Chong *et al*. [46] reported the use of Hafnium into active layer for their HfInZnO TFTs can make an increase of stability under light and bias conditions thank to the presence of Hf^{4+}. Se Yeob Park *et al*. [47] fabricated IZO TFTs with high mobility and improved stability using oxygen high-pressure annealing.

Today, oxide TFTs could not replace a-Si:H in AMLCD industry. However, they are good candidate for upcoming and potential applications such as AMOLED display [48], flexible electronics [49] and photosensor-based interactive display [50]. In order to be sufficient for these novel applications especially for AMOLED, instability problem of oxide TFTs should be identified and characterized. Today, this work is still at an early stage.

The instabilities of oxide TFTs can be caused by bias stress, illumination, impact of surface passivation and so on. Most of the instability studies focus on staggered bottom gate (SBG) structure because it is the mostly used structure.

The studies of gate-drain bias stress effect on oxide TFTs can be subdivided [44] into low-field (<1MV/cm) positive gate bias stress [51]-[53], high-field (>1MV/cm) positive gate bias stress [54, 55], negative bias stress [56, 57], dynamic bias stress, bias stress under illumination and process dependence. The recovery when unbiased is also considered, because the transistor is not always turned on for AMLCD application. The results can be summarized as below: 1) In contrast to a-Si:H/Si_3N_4 TFTs, the majority of oxide TFT present recoverable shift of threshold voltage under low-field gate bias stressing without any annealing. This may be explained by the trapping at pre-existing defects at or near dielectric/channel interface with little creation of new defects [44], while the a-Si:H/Si_3N_4 TFTs degraded irreversibly with creation of new defects in the channel or at the dielectric/channel interface under gate bias stress. 2) After high-field gate bias stress, the annealing might be needed for the recovery of oxide TFTs. More researches are needed for these topics.

The unpassivated SBG oxide TFTs exhibit the sensitivity of ambient environment [58] and molecules interaction with O_2 and H_2O. Therefore, proper passivation is needed to realize stable SBG oxide TFT. Now, it is also a critical issue for the commercialization of oxide TFTs.

5.3 Silicon thin film transistors

5.3.1 Amorphous silicon thin film transistors

The hydrogenated amorphous silicon thin film transistors (a-Si:H TFT) has dominated the flat-panel display industry for a long time. This may be attributed to these five reasons [59]: 1) Amorphous silicon has all the typical semiconducting properties; 2) Possibility of plasma deposition on large area; 3) Good reproducibility; 4) Good interface properties between a-Si:H and other thin films; 5) Low temperature fabrication. The typical threshold voltages are in the range 2-4V and state-of-the-art motilities are in the range 0.4-1.0 $cm^2/V.s$ [60].

A-Si:H has a random covalent network structure in which the Si-Si and Si-H have different lengths and angles. Figure 1.11 shows a model of a-Si:H structure. Despite its importance for the electronic properties of a-Si:H, hydrogen has some negative effects. If the Si-H bond is broken, Si dangling bond generate and act as a trap in the a-Si:H. The Si dangling bonds correspond to the deep states in the a-Si:H, while another localized states was recognized as tails states which is situated just below the conduction band mobility edge. Figure 1.12 gives an example of density of states for a-Si:H [59].

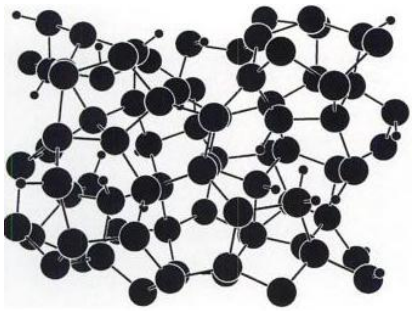


Figure 1.11: Model of a-Si:H network structure [59]

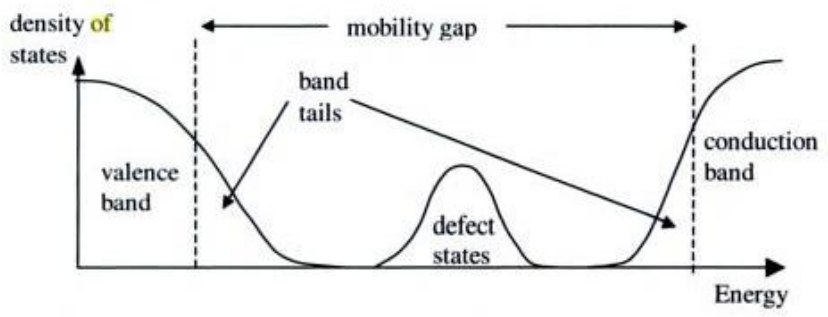


Figure 1.12: Density of states for a-Si:H [59]

A-Si:H TFTs show threshold voltage shift under gate bias stressing which has been studied extensively [60]-[62]. Two instability mechanisms have been investigated to explain these phenomena: 1) defect state creation in the a-Si:H and 2) charge trapping in the gate dielectric or at the dielectric/channel interface . M. J. Powell *et al* [60] reported that the defect state creation is the dominant mechanisms at low gate bias stress and the charge trapping in the gate dielectric is dominant at high gate bias stress. They reported also a power law time dependence for defect creation in the a-Si:H film and a logarithmic dependence for charge trapping in the gate dielectric. N. Nickel *et al* [62] reported that the state creation in the a-Si:H has much weaker influence than charge trapping. They have found that the density of state is enhanced by a factor of two only even with strong bias stress. They have investigated the activation energy for defect formation which is about 0.7eV. They suggested that the charge trapping in the gate dielectric causes more limitations of a-Si:H TFT applications.

As mentioned in section 1.1, a-Si:H TFTs suffer from their low mobility and instability which limit their applications of AMLCD and AMOLED. Although there are some studies on the realization of high-quality a-Si:H TFTs for AMOLED [63, 64], they might be replaced by the other TFT technology in the future.

5.3.2 Low-temperature polycrystalline silicon (LTPS) thin film transistors

Recently, the low-temperature polycrystalline silicon thin film transistor (LTPS TFTs) has been used for the TFT-LCD applications with high resolution [65]. This type of TFT has

several orders of magnitude higher carrier mobility comparing with a-Si:H TFT [65]-[67]. The high mobility leads to a simplification of integrated driving circuit for active matrix addressed displays. This advantage can be attributed to their relatively larger grain size. This is also the reason why LTPS TFT is a promising choice for the advanced display applications.

The conventional way to get LTPS TFTs is crystallizing an a-Si:H film after its deposition. There are many crystallization methods: solid-phase crystallization [66], metal-induced lateral crystallization [67] and excimer laser crystallization [65]. Different crystallization technologies result in different grain structure which causes different device behaviors [68]. In addition, these methods need high temperature or laser crystallization. Consequently the fabrication cost increase. Therefore the application of LTPS TFTs for large area electronics is limited [68].

Another limitation of LTPS TFTs is the presence of many grain boundaries between the poly-grains. A great number of grain boundaries exist in the channel and act as traps. The performance of LTPS TFTs is strongly suffered from them. The enlargement of grain size can reduce the reduction of performance by the grain boundaries. Changing the thickness of LTPS film or controlling the deposition conditions affects the grain size or the grain boundaries' degradation effect [69, 70]. Moreover, the grain boundaries make also the LTPS TFTs less uniform. That is another reason why the application of LTPS TFTs in large area is limited.

The instability of LTPS TFTs is also a key issue that has to be well studied for their applications. For example, J. C. Liao *et al* [71] found the frequency dependence of dynamic negative bias temperature instability of LTPS TFTs, which means the operation frequency of LTPS TFTs influences threshold voltage shift of TFT. I. H. Peng *et al* [72] investigated the influence of mechanical strain on LTPS TFTs fabricated on stainless steel substrate. They found that the mobility and threshold voltage shift after bias stress of TFT are influenced by tensile and compressive strain due to the variation of electrical properties of drain region caused by mechanical strain. C. A. Dimitriadis [73] has investigated the gate bias instability with different stressing durations. For short stress duration, the degradation of transfer characteristics is due to electron tunneling into gate oxide and interface states. For longer

stress duration, the degradation is due to enhancement of the donor-like interface states generation.

5.3.3 Microcrystalline silicon thin film transistors

5.3.3.1 Performances of microcrystalline silicon TFTs

The microcrystalline silicon TFTs show better mobility and stabilities than those obtained with a-Si:H TFTs. In some reports, the mobility of microcrystalline silicon TFTs is in the range from 0.5 cm^2/Vs to 30 cm^2/Vs [74]–[77]. Beside their mobility, some groups investigated the stabilities of microcrystalline silicon TFTs and found:

1) The shift of threshold voltages after positive and negative gate bias stress for microcrystalline silicon TFTs towards the same direction of stress, respectively. The recovery of the initial characteristics has been observed without annealing. In contrast, the a-Si:H TFTs shows only the shift towards positive gate voltage and the device cannot be recovered without annealing. This phenomenon has been attributed to different instability mechanisms. Shift of threshold voltages for microcrystalline silicon TFTs is caused by charge trapping in the gate dielectric [77].

2) R. B. Wehrspohn *et al* [78] compared the electrical stability of a-Si:H and microcrystalline silicon TFTs. In their research, the microcrystalline silicon TFT is more stable. They found that the a-Si:H and microcrystalline silicon TFTs have almost the same defect creation barrier energy. The better electrical stability of microcrystalline silicon TFTs compared with amorphous silicon TFTs is due to a much lower attempt frequency which means the probability that an electron attempts to break the bond.

3) M. Oudwan *et al* [79] reported that the bottom gate microcrystalline silicon TFTs show lower threshold voltage shift (0.05V after 10h stress under the conditions: V_g=12V and V_d=10V) compared with polymorphous and amorphous silicon TFTs. They concluded that the main degradation mechanism is due to charge trapping in the gate dielectric while defect state creation is almost absent. In the case of polymorphous and amorphous silicon TFTs, both charge trapping and defect creation mechanisms existed.

With their high mobility and good stability, microcrystalline silicon TFTs is an interesting and promising candidate for the active matrix display applications. In fact, the study on microcrystalline silicon is one of the main research topics in microelectronic and micro-sensors group in Institute of Electronics and Telecommunications of Rennes (IETR). The optimization of the material and the realization of devices using PECVD at low temperature (<200°C) have been carried out by previous works in different PhD thesis. In the thesis of K. Kandoussi [80], the optimized PECVD deposition parameters, especially the argon flow added to the reaction gas mixture, are obtained at temperature lower than 200°C. The stable n-type Top-gate TFTs with mobility of 10 cm^2/Vs are obtained. P-type TFTs, bottom TFTs and TFTs on the plastic substrate are also fabricated.

In the thesis of S. Janfaoui [81], both N-type and P-type microcrystalline silicon TFTs are fabricated on PEN Q65FA (Polyethylene naphthalate), a flexible and transparent substrate. N-type TFTs are stable but P-type TFTs show large threshold voltage shift under gate bias stress. Furthermore, both types of TFTs are mechanically stressed and their behaviors are studied.

5.3.3.2 Material properties of microcrystalline silicon

a) Structure and growth mechanisms of microcrystalline silicon

Microcrystalline silicon films have crystalline structure but the grain size is smaller than polycrystalline silicon. Beside the crystalline structure, they have also amorphous phase and voids. The distribution of crystalline phase, amorphous phase and voids depends on the deposition conditions.

The four-phase growth mechanism of microcrystalline silicon has been demonstrated by P. Roca i Cabarrocas [82] as below:

1) Incubation

In the beginning of microcrystalline silicon growth, an amorphous layer is formed. This incubation layer is highly porous and hydrogen-rich. The thickness of incubation layer can

be reduced by the use of highly diluted silane-in-hydrogen or by the modification of interface using argon and hydrogen plasma.

2) Nucleation

The nucleation of crystallites takes place after the highly porous and hydrogen-rich incubation layer has been formed. The density of nucleation depends on the quantity of active site on the interface which is created during the incubation phase. The nucleation needs the incorporation between hydrogen plasma and SiH_x radicals.

3) Growth

In the growth phase, the crystalline volume fraction increase until a steady-state. This phase leads an expense of amorphous phase.

4) Steady-state

The steady-state can be seen as equilibrium between competing factors such as hydrogen flux and quantity of radicals. The crystalline volume fraction at steady-state is influenced by the plasma conditions.

b) Density of states in microcrystalline silicon

It is well known that the subthreshold slope of TFTs is closely related to density of deep states [83]. The density of states can be measured directly using the isothermal capacitance transient spectroscopy (ICTS) [84]. A comparison between the state distributions in microcrystalline silicon and a-Si:H is shown in figure 1.13. The density of deep states (away from conduction band more than 0.5eV [83]) in microcrystalline is smaller than in a-Si:H.

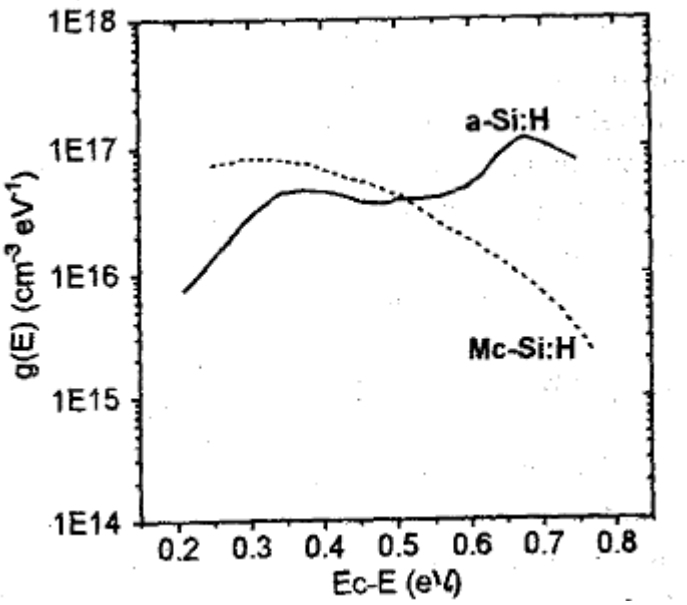


Figure 1.13: Density of states in microcrystalline silicon and a-Si:H measured by ICTS [83].

The density of states in microcrystalline can also be calculated from the analysis of the TFT field-effect conductance, which has been used in the case of a-Si:H and polycrystalline silicon [85]. In some previous works [86], the densities of states in the microcrystalline silicon films fabricated by different gas mixture conditions have been calculated using an incremental method [85], as shown in figure 1.11 [86].

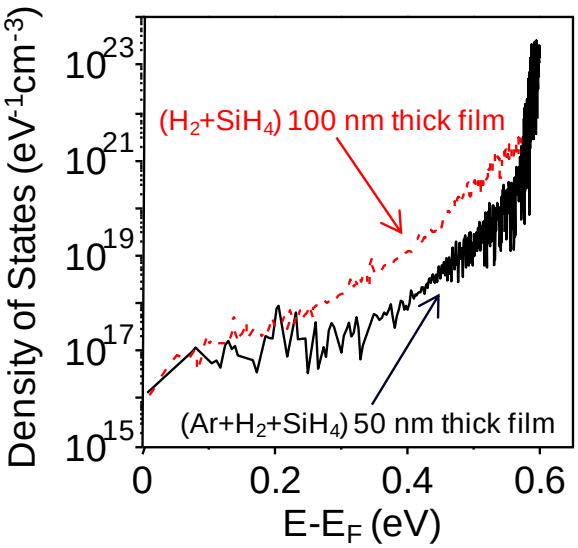


Figure 1.14 Density of states in microcrystalline silicon calculated using incremental method.

c) Crystalline volume fraction of microcrystalline silicon

The microstructure of microcrystalline as a function of crystalline volume fraction is shown in figure 1.15 [87]. The crystalline volume fraction can be influenced by the deposition conditions. For example, K. Y. Chan *et al* [87] change the crystalline volume fraction of microcrystalline silicon by varying the silane concentration during the deposition.

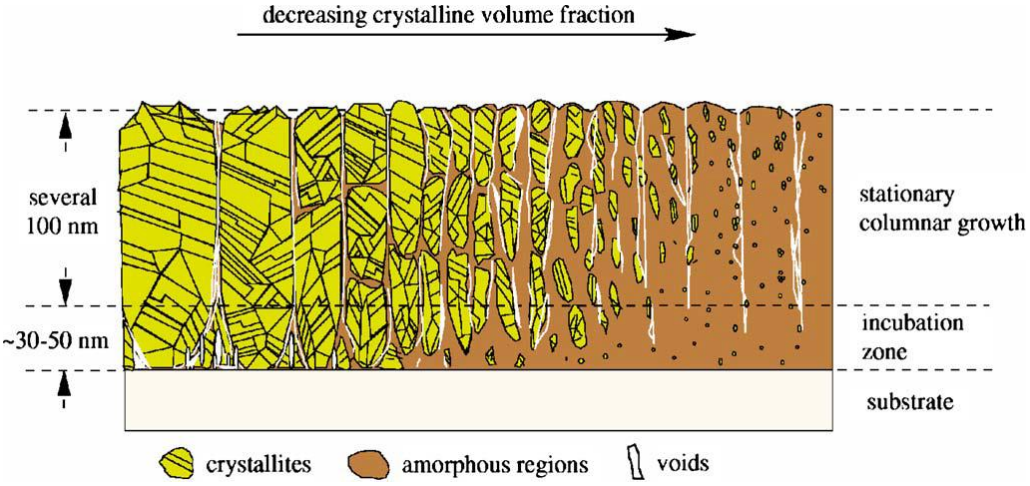


Figure 1.15: Microstructure of microcrystalline silicon as a function of crystalline volume fraction.

It is commonly assumed that the highest charge carrier mobility of thin film transistor will be achieved for films with high or very high crystalline volume fraction. However, in some reports [77][87][88], the best characteristics of microcrystalline silicon films have been obtained for material near the transition to the amorphous growth regime. K. Y. Chan *et al* [87] reported that the microcrystalline silicon thin film transistor with best characteristics such as mobility, subthreshold slope and defect density is found for near the transition to the amorphous growth.

6. Conclusion

The TFTs used for flexible electronics should be fabricated at low temperature. The main potential applications include flexible display, flexible sensor and RFID, etc. To realize these applications, the TFTs fabricated at low temperature should have sufficient mobility and be electrically stable. Several low-temperature TFT technologies have been largely studied to

overcome the well-known drawbacks, low mobility and electrical instability, of conventional a-Si TFTs which have been regarded insufficient for the future display devices.

The lightweight and inherently flexible organic TFT can be solution-processed at very low temperature thereby decreases the cost. Their mobility has been remarkably increased in the recent years and reaches the same or higher magnitude of order of a-Si TFT. However, they need more robust fabrication process and deeper understanding of function mechanism to up onto the next stage of final mass production.

Oxide TFTs exhibit promising performances for the application of AMLCD or AMOLED. They have also the challenges: 1) Finding the dielectric and channel material; 2) Instabilities identification; 3) finding the proper passivation. This technology is also in an early stage.

The LTPS TFTs has very high mobility and good stability. But the excimer laser crystallization process limits their uniformity and increases the cost.

The microcrystalline silicon TFTs has higher mobility and better electrical stability than a-Si TFT. Therefore the TFTs using the microcrystalline silicon fabricated at low temperature and optimized in our laboratory might be a good candidate for the applications of high-resolution and flexible display.

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Chapter2: Technologies for the microcrystalline silicon TFT fabrication

1. Introduction

The studies on the technologies for the microcrystalline silicon TFT fabrication at microelectronic and micro-sensor department of IETR were started from the thesis of K. Kandoussi in 2004. The main goal of this thesis was to develop a microcrystalline silicon process at low temperature, lower than 180 °C, which is compatible with flexible substrates like PEN. The microcrystalline silicon layer deposited by PECVD was optimized during this work. The TFTs use undoped microcrystalline silicon layer deposited at 165 °C as active layer and silicon oxide layer as gate insulator. The TFTs have high mobility but are electrically unstable.

Envisaging the electrical stability problematic for the TFTs with silicon oxide as gate insulator, K. Belarbi has worked on an alternative material, silicon nitride, as gate insulator of TFTs in order to improve the electrical stability. This silicon nitride layer was deposited by PECVD at 150 °C, an optimized temperature compatible with PEN substrate. The electrical stability has been largely improved by replacing silicon oxide with silicon nitride as gate insulator of TFT but the mobility, ranging from 0.49 cm^2/Vs to 2 cm^2/Vs, was decreased.

Then the microcrystalline silicon TFTs with silicon nitride gate insulator has been fabricated on flexible substrate in the thesis of S. Janfaoui. Both N-type and P-type TFTs have been fabricated on 125 µm thick PEN Q65FA substrate produced by DuPont Teijin Film. The microcrystalline silicon and silicon nitride have been used as active layer and gate insulator. The electrical characteristics of TFTs on PEN have been investigated and degradations in terms of mobility, subthreshold slope and electrical stability, compared with TFT on glass, have been discussed. Then the mechanical behavior of TFTs on PEN has been studied. The N-type microcrystalline silicon TFTs showed an increase of mobility and a decrease of threshold voltage with tensile bending and a decrease of mobility and an increase of threshold voltage with compressive bending. In the case of P-type TFTs, the trends are contrary. The TFTs on 125 µm thick PEN could work until bending radius of 10 mm.

In this chapter, these works are summarized. The material used and the process developed by these precedent works were presented in this chapter. The techniques and equipment

utilized for the deposition and characterization of thin film, and basic working principle and characterization of TFT was also presented in this chapter.

2. Deposition technologies and material properties for the realization of low temperature microcrystalline silicon thin film transistor

2.1 Undoped and doped microcrystalline silicon

2.1.1 Deposition of undoped and doped microcrystalline silicon film

There are many methods to fabricate microcrystalline silicon films: HWCVD (Hot-wire chemical vapor deposition), photo-CVD, microwave CVD and PECVD (Plasma enhanced chemical vapor deposition). The last one, PECVD, is the mostly used technology to fabricate microcrystalline silicon. Because PECVD is also the current industrial technology of the a-Si:H deposition, the microcrystalline silicon TFTs fabricated by PECVD provide an inexpensive way to replace the a-Si:H TFT in industry.

A PECVD system uses chemical reaction of plasma, which is created from the dissociation of reaction gases, to deposit thin film from vapor to solid phase. The gases used for the deposition of microcrystalline silicon film are SiH_4 diluted in the H_2 or Ar or (H_2 + Ar) mixture. The plasma is generally created by RF frequency at 13.56 MHz discharging between two electrodes. The space between these two electrodes is filled with the reaction gases.

Figure 2.5 presents the PECVD system used in IETR for the deposition of microcrystalline silicon thin film at low temperature. It is composited by 3 parts: deposition reactor, pumping system and gases management system.

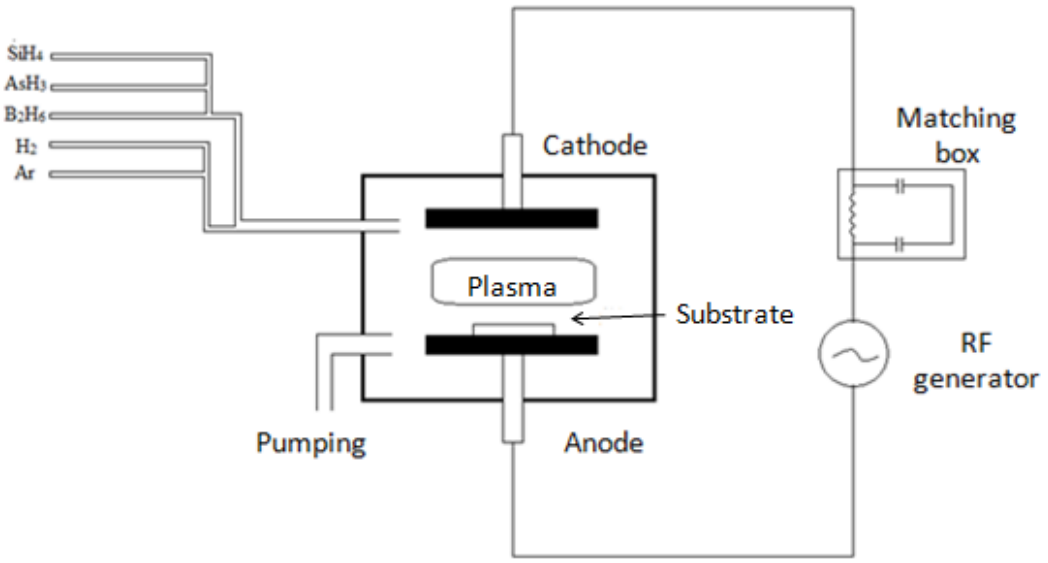

Figure 2.5: Schematic of the PECVD system in IETR

The deposition reactor has two electrodes in parallel which have 15 cm of diameter. These two electrodes are the anode and cathode used for the plasma generation. The anode supports the samples and is connected to ground. A heating system, which contains a heater and a thermocouple, is placed under the anode for the temperature controlling during the deposition. The inter-electrodes distance can also be adjusted by moving vertically the anode. The cathode is connected with a RF source. Between the cathode and the RF source, there is a resonance box. By adjusting this resonance box, an optimum RF power is applied on the plasma.

The pumping system is constituted by a primary pump, 'Varian', and a secondary pump, 'Edward'. The primary pump provides a vacuum level at about 2.10^{-2} mbar. Then secondary pump continues until the vacuum level arrives at an order of magnitude of 10^{-6} mbar.

The gases used for the deposition of undoped or doped microcrystalline silicon are introduced into the reactor during the deposition. These gases flow are controlled by flow meters which situated behind the reactor. Gases used for the undoped film deposition are the SiH_4, H_2 and Ar. For the N-type and P-type doped film, AsH_3 and B_2H_6 are added respectively.

The work on the microcrystalline silicon deposited by PECVD in IETR was started with the thesis of K. Kandoussi. The optimized microcrystalline silicon was deposited at 165 °C. Using this microcrystalline silicon as the active layer and silicon oxide as the gate insulator, the N-type TFTs have mobility of 6 cm^2/Vs. In the thesis of S. Janfaoui, the TFTs use this undoped microcrystalline silicon as active layer are fabricated on PEN substrate. The P-type TFTs was also realized.

2.1.2 Material properties of undoped and doped microcrystalline silicon

2.1.2.1 Undoped microcrystalline silicon

The undoped microcrystalline silicon is used as active layer of TFTs. This layer is optimized by K. Kandoussi [1]. In his works, the effect of argon gas in the gas mixture during the deposition was studied. Moreover, the influence of the other deposition parameters such as pressure, RF power and gas ratio has been also evaluated. The temperature of this deposition is fixed at 165 °C because the goal of this study is to develop a reproducible fabrication process of microcrystalline silicon TFTs on flexible substrate. The deposition pressure and RF power have firstly been studied. Indeed, when the pressure increases, the number of ions collision increases and the ions bombard energy decreases. The best quality of microcrystalline silicon has been obtained with high pressure. On the other hand, the increase of RF power leads to an increase of plasma sheath. The ions energy increases consequently. The best microcrystalline silicon has been deposited with weak RF power. The pressure and RF power have been fixed at 0.9 mbar and 15 W, respectively.

The gas ratio has also been studied. The gases used for the microcrystalline silicon deposition are SiH_4, Ar and H_2. The influence of the addition of Ar in the gas mixture (Ar-H_2) is studied by fixing SiH_4 at 1% of the Ar-H_2 mixture. Therefore, the studies have been realized by varying Ar ratio in the Ar-H_2 mixture. According to this study, the optimum microcrystalline silicon is obtained when the Ar-H_2 mixture is composited by 50 % of argon and 50% of hydrogen. Figure 2.6 presents the crystalline fraction of microcrystalline as a function of Ar ratio in the Ar-H_2 mixture. This film is deposited with pressure p = 0.9 mbar,

RF power P = 15W, and $SiH_4/(Ar+H_2)$ = 1%. The result shows that the best crystalline fraction is obtained when $Ar/(Ar+H_2)$ ratio is 50 %.

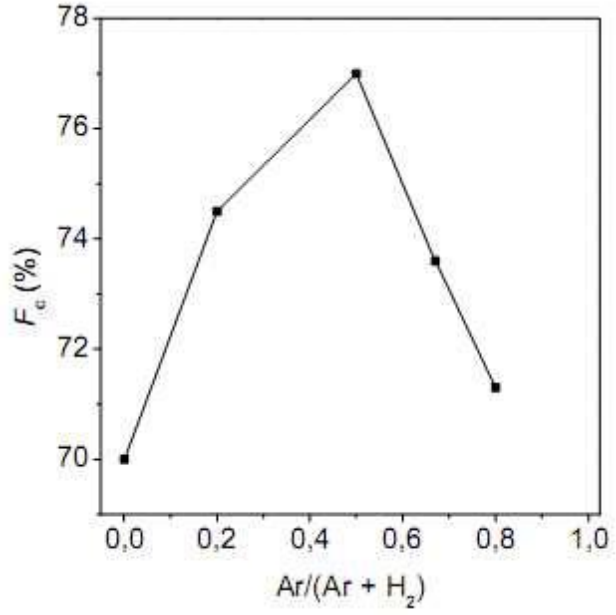

Figure 2.6: Crystalline fraction of microcrystalline silicon as a function of argon ration in the $(Ar-H_2)$ mixture [1].

The benefit of adding Ar in the reaction gases is then studied. The added Ar is excited by plasma charging into metastable state Ar*. The metastable argon ions accelerate the dissociation of silane by the following reaction:

$SiH_n + Ar^* \rightarrow SiH_{n-1} + H + Ar$

The hydrogen dissociation is also accelerated by:

$H_2 + Ar^* \rightarrow 2H + Ar$

These accelerated dissociation reactions cause the improvement of crystalline fraction of microcrystalline silicon and the increase of the deposition rate. However, if the Ar ratio in mixture $(Ar-H_2)$ is overmuch, the number of hydrogen atoms decreases and the surface roughness increases. The overmuch Ar causes also powders during the deposition. This explains why the optimum film is obtained with $Ar/(Ar+H_2)$ = 50 %.

Then the microcrystalline silicon deposited using silane diluted only in hydrogen and in Ar-H_2 mixture are compared. Figure 2.7 a) shows crystalline fraction of these 2 types of deposition with different thicknesses. Figure 2.7 b) shows the transfer characteristics of TFT using these 2 types of microcrystalline silicon as active layer. These results reveal the improvement benefited from the adding of argon in terms of the quality of microcrystalline silicon film and the electrical performance of TFTs using these films as active layer.

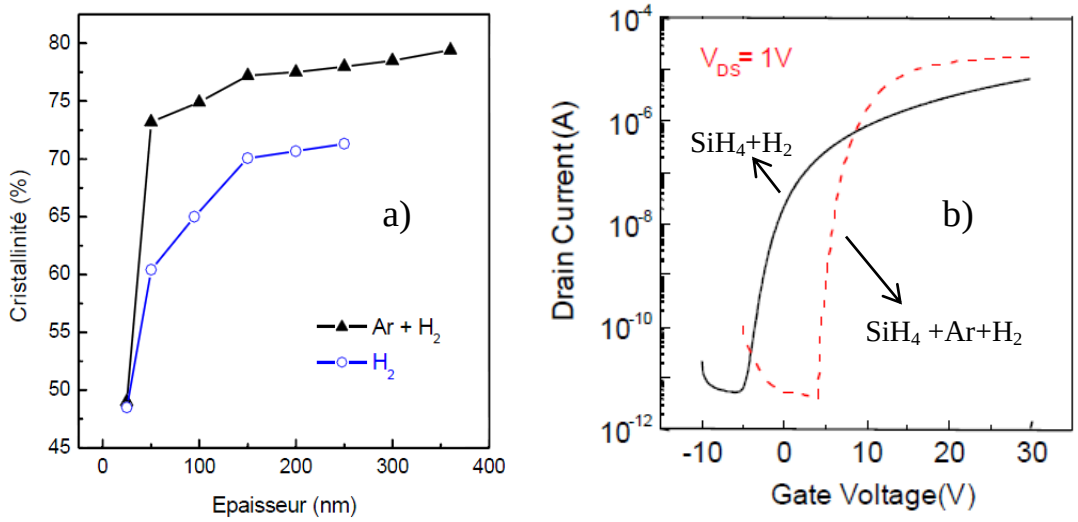

Figure 2.7 a): Crystalline fraction as a function of microcrystalline silicon thickness for deposition with Ar+H_2 and with only H_2, b): Transfer characteristics of microcrystalline silicon TFTs fabricated using Ar+H_2 and using only H_2

The deposition conditions of microcrystalline silicon using Ar-H_2 mixture have been optimized by R. Cherfi [2] in 2009. Table 2.1 presents these conditions.

RF power (W)	Pressure (mbar)	D_{A-K} (cm)	Temperature (°C)	SiH_4 (sccm)	Ar (sccm)	H_2 (sccm)
32	0.9	4.5	165	1	40	60

D_{A-K}: Distance between two electrodes

Table 2.1: Deposition conditions of undoped microcrystalline silicon

By using these deposition conditions, undoped microcrystalline silicon film has crystalline fraction varying between 73% and 78% for a thickness varying between 50 nm and 200 nm, and has an activation energy varying between 0.4 eV and 0.6 eV.

In this work, undoped microcrystalline silicon film deposited for active layer of TFT have been achieved in these conditions.

2.1.2.2 N-type doped microcrystalline silicon

The N-type doped microcrystalline silicon is used to form the source and drain region of TFTs. This layer is deposited using same technology as undoped film deposition. The deposition conditions are always following the optimization of undoped microcrystalline silicon deposition. Here, doping gases should be added during the deposition. In our case, the doping gas used is AsH_3. Moreover, two deposition technologies have been used. The first one is monolayer deposition. By this technology, undoped silicon and doped silicon are deposited without breaking vacuum and interrupting plasma. Only the doping gas is added for the doped silicon deposition. The second one is bilayer deposition. This technology achieves undoped and doped silicon deposition in two different machines. The bilayer deposition may create an interface between undoped and doped layer reducing the mobility of final TFT device.

In microelectronic and micro-sensor department of IETR, the studies on the optimization of N-type doped microcrystalline silicon have been started from the thesis of K. Kandoussi. Then in the thesis of K. Belarbi [3], the quality of N-type doped microcrystalline silicon has also been improved. Since 2009, the optimum N-type doped microcrystalline silicon layer has been deposited using gas mixture composited by 50% of argon and 50% of hydrogen. The maximum conductivity obtained is 55 $S.cm^{-1}$ for a thickness of 200 nm. The following table illustrates the N-type doped microcrystalline silicon deposition conditions which are used for the N-type TFTs in this work.

RF power (W)	Pressure (mbar)	D_{A-K} (cm)	Temperature (°C)	SiH_4 (sccm)	Ar (sccm)	H_2 (sccm)	AsH_3 (sccm)
15	0.9	4.5	165	1.5	75	75	10

Table 2.2: Deposition conditions of N-type doped microcrystalline silicon

2.2 Deposition of gate insulator

The gate insulator plays an important role for the TFT performances. These performances depend on both quality of gate insulator and interface between gate insulator and silicon. The quality of a gate insulator is studied using a MIS capacitor (metal insulator semiconductor), by measuring C-V curve in quasi-static regime (QS-C(V)) and in high-frequency regime (HF-C(V)). For a gate insulator with good quality, its MIS capacitor characteristics should present:

- ✓ Capacity saturation in the quasi-static regime
- ✓ Same value of capacitance in both accumulation and inversion regimes of QS-C(V)
- ✓ Identical HF-C(V) and QS-C(V) curves in both depletion and accumulation regimes
- ✓ A minimum depth of the QS-C(V) characteristics
- ✓ Weak flat band voltage (V_{FB})

There are some choices for the gate insulator: silicon oxide (SiO_2), alumina (Al_2O_3) or silicon nitride (Si_3N_4). Lots of technologies can achieve the low temperature deposition for these gate insulator materials. Silicon oxide can be fabricated by sputtering, PECVD or ECR-CVD (electron cyclone resonance CVD), etc. Alumina can be deposited by ALD (atomic layer deposition). Silicon nitride can be obtained by sputtering, PECVD or ECR-CVD, etc.

2.2.1 Silicon oxide deposited by sputtering

The sputtering system uses ions bombardments to capture atoms on the surface of the target, which is made by the materials that we want to deposit. Then the atoms are projected on the substrate to form the gate insulator film. This system usually has two electrodes to produce plasma. The target and the substrate are installed on the cathode and anode respectively. This technology provides the fabrication of silicon oxide film used as gate insulator of TFT at very low temperature.

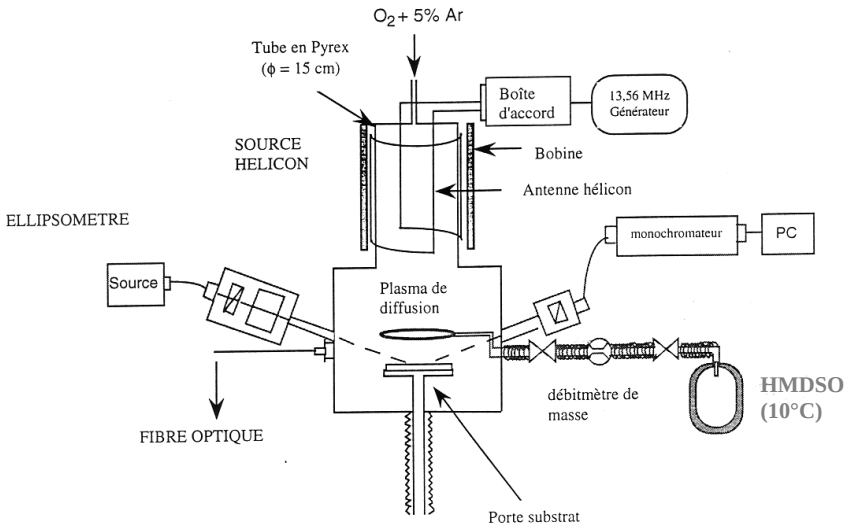

Figure 2.8: Schematic of sputtering system

The deposition of silicon oxide by sputtering at room temperature has been developed during the internship work of A. Gorin [4]. Figure 2.8 shows the schematic of this sputtering deposition. The gases used for the deposition is a mixture of Ar-O_2 without heating. H_2 and O_2 mixture is used for the post-treatment in order to improve the film quality. Finally, a 180°C annealing under nitrogen is performed to improvee the electrical characteristics. Table 2.3 a) and b) present the conditions of these deposition and post-treatment.

Deposition	Power (W)	Pressure (mbar)	D_{A-K} (cm)	Mixture Ar-O_2
SiO_2	200	$5\ 10^{-3}$	8	30%(O_2)

Table 2.3 a): Deposition conditions of sputtering SiO_2

Post-treatment	Power (W)	Pressure (mbar)	D_{A-K} (cm)	H_2 (sccm)	O_2 (sccm)
SiO_2	100	$5\ 10^{-3}$	8	20	10

Table 2.3 b): Post-treatment conditions of sputtering SiO_2

The result of the capacity-voltage characteristics measurement at 1MHz and quasi-static of MIS capacitor fabricated by using this type of silicon oxide is shown in the following figure:

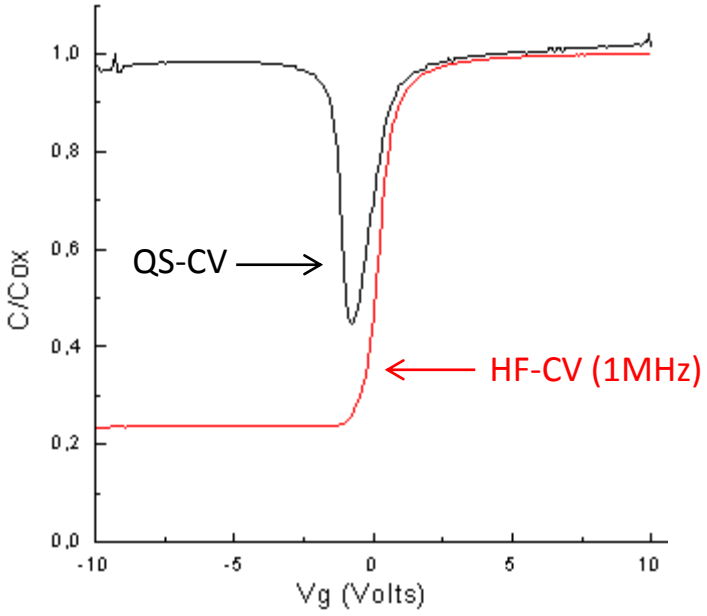

Figure 2.9: C-V characteristics of N-type sputtering silicon oxide MIS capacitors, measured at 1MHz (HF-CV) and quasi-static (QS-CV). The thickness of silicon oxide is 70nm. [4]

This figure shows clearly identical HF and QS characteristics in depletion and in accumulation regime, a large slope of HF characteristic in depletion regime, and a presence of a peak in QS characteristic. These properties indicate a good quality of sputtering silicon oxide as gate insulator.

2.2.2 Silicon oxide deposited by ECR-CVD

The ECR is a phenomenon observed in plasma physics. An electron in a static and uniform magnetic field will move in a circle due to the Lorentz force. The ECR-CVD uses

ECR condition to excite gases into plasma, using commonly a microwave at 2.45 GHz and a magnetic field of 875 gauss. Then the chemical reaction occurs by the incorporation of the ionized gases to form the material wanted.

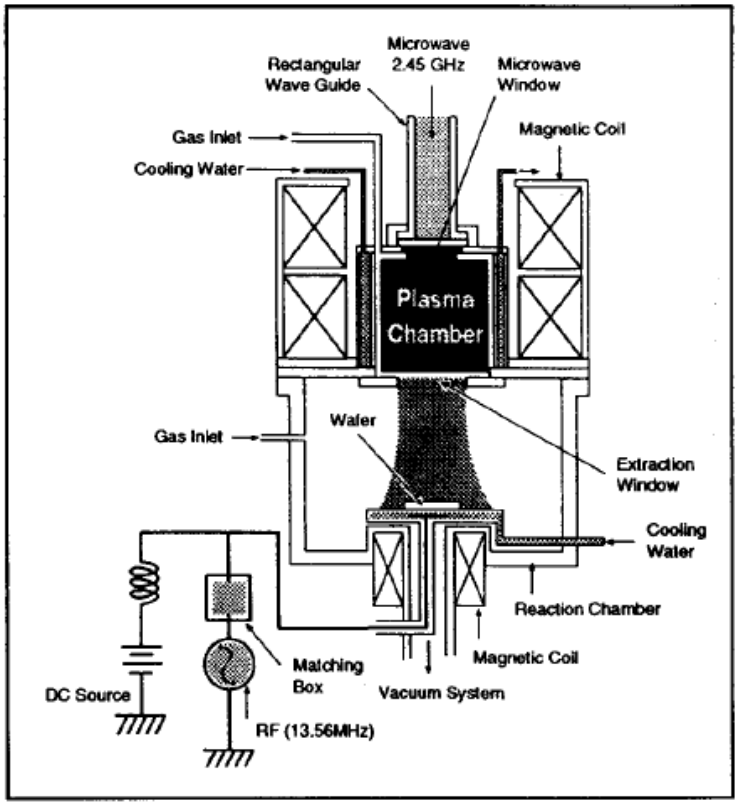

Figure 2.10: Schematic of ECR-CVD system [5]

Figure 2.10 shows an example of ECR-CVD system [5] for SiO_2 deposition. This system consists of two chambers, microwave chamber used for plasma forming and downstream chamber for chemical reaction. The oxygen and argon are excited to ions by magnetic field and then enter the downstream chamber. After that, silane reacts with oxygen to form SiO_2 with the assistance of argon.

2.2.3 Alumina deposited by ALD

The ALD deposition technology is based on the sequential use of self-terminating gas-solid reaction [6, 7]. The basic 4 steps of ALD deposition is: the first surface reaction on the substrate, the removing of the residual non-reacted gases, the second surface reaction and the

purge. The whole ALD deposition is the repeating of these 4 steps which could be referred as an ALD reaction cycle until sufficient thickness will be deposited. By using this method, ALD presents good film uniformity even on a complex substrate surface. The deposition temperature of ALD could also be lower than 180°C which is compatible for a flexible substrate. Figure 2.11 presents an example of ALD system used for low temperature Zno, TiO_2 and Al_2O_3 deposition [8].

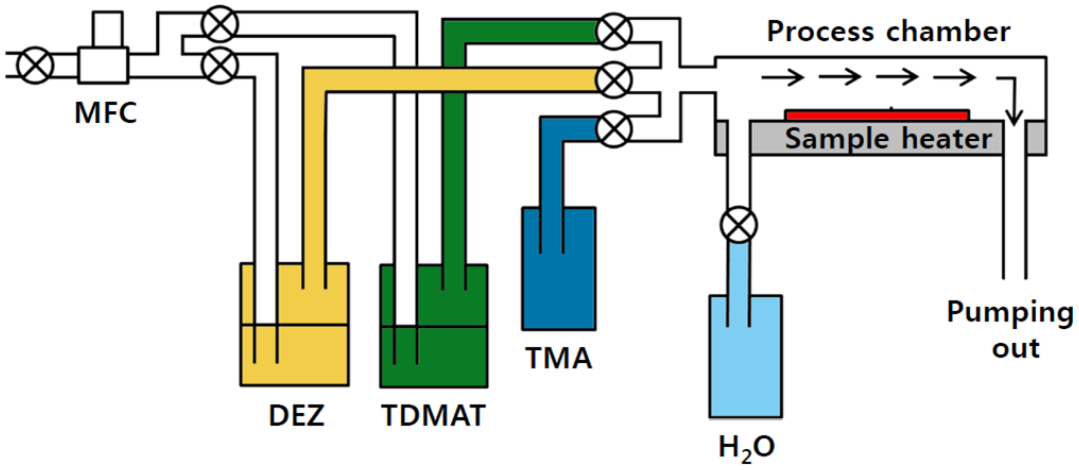

Figure 2.11 ALD system used for ZnO, TiO_2 and Al_2O_3 deposition. tetrakis (dimethylamino) titanium (TDMAT), trimethylaluminum (TMA), and diethylzinc (DEZ) are employed as precursors for ALD TiO_2, Al_2O_3, and ZnO, respectively [8].

The Al_2O_3 is one of the most studied materials of ALD deposition. The deposition usually uses trimethylaluminum (TMA) and H_2O in order to perform an overall reaction:

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 3CH_4$$

Figure 2.12 [9] presents the C-V characteristic for serials frequencies of a N-type and a N-type MIS capacitor using ALD Al_2O_3 deposited in IMEC, Leuven, Belgium. The thickness of this ALD AL_2O_3 film is 10nm.

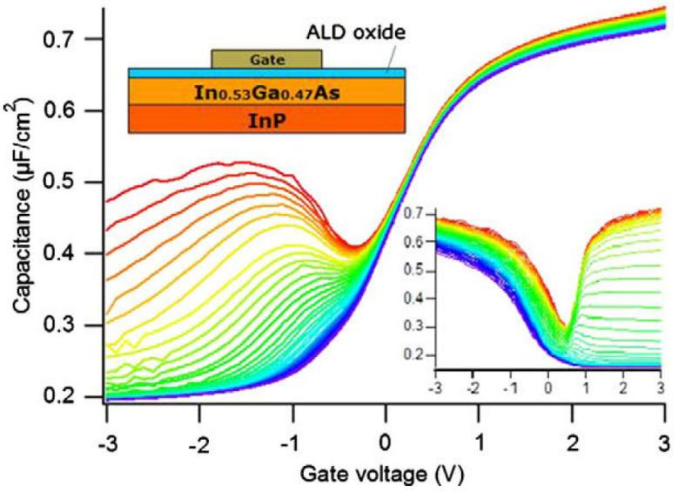

Figure 2.12: C-V characteristic of N-type ALD alumina MIS capacitors measured from 3 KHz to 1 MHz. Inset: P-type C-V characteristic measured from100 Hz to 1 MHz. [9]

2.2.4 Silicon nitride deposited by PECVD

The PECVD is also used for the silicon nitride deposition in IETR. The deposition parameters have been optimized by K. Belarbi [2]. For this optimization, SiH_4, N_2 and NH_3 have been used as the reaction gases. The temperature has been fixed at 150 °C. Table 2.4 presents the detailed deposition conditions.

Deposition	Power (W)	Pressure (mbar)	D_{A-K} (cm)	Temperature (°C)	SiH_4 (sccm)	N_2 (sccm)	NH_3 (sccm)
Si_3N_4	30	0.6	4.5	150	2	80	40

Table 2.4 Deposition conditions of silicon nitride

After the deposition, annealing at 180°C under nitrogen gas is carried out during 2 hours to densify the layer. The C-V characteristic at 1MHz and the quasi-static C-V characteristic of a MIS capacitor using Si_3N_4 deposited in the precedent conditions are shown in the figure 2.13. The thickness of this Si_3N_4 layer is 300 nm.

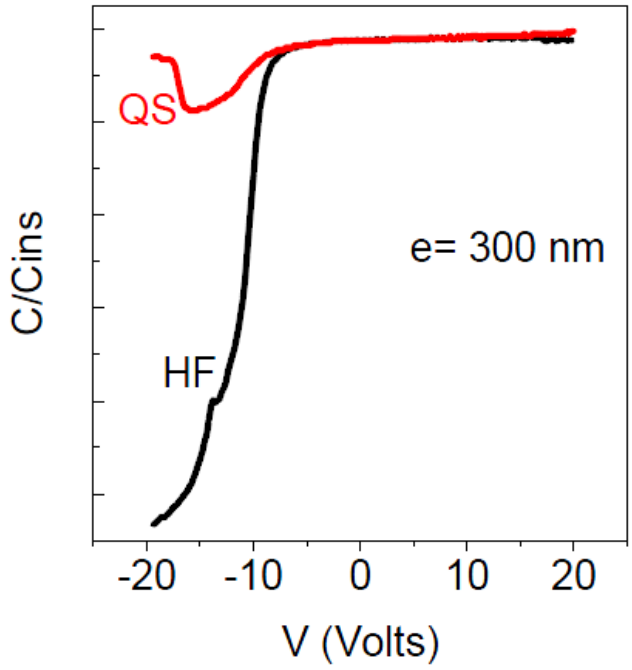

Figure 2.13: C-V characteristics of N-type PECVD silicon nitride MIS capacitors, measured at 1MHz (HF-CV) and quasi-static (QS-CV). The thickness of silicon nitride is 3000nm. [2]

This figure presents same capacitance value of QS-C(V) and HF-C(V) in accumulation regime, large slope of HF-C(V) in depletion regime and a presence of a small peak in QS-C(V). These results indicate interesting quality of silicon nitride as gate insulator of TFT.

3. Technologies for thin film characterization

3.1 Thickness measurement by profilometer

The thicknesses of different thin films, which are deposited for TFT architecture, have been measured by profilometer. To measure the thickness of a thin film, which covers normally an entire surface of substrate, a step between thin film and substrate should be realized by photolithography etching. Then, a scanning stylus moves across the step vertically to get profile information of the thin film.

In the microelectronic and micro-sensor group of IETR, the profilometers utilized is a KLA-TENCOR P6 [10]. This profilometer has a high resolution with order of magnitude of

Angstrom. The P6 offers serials benefiting features such as low noise, top view objective lens of 4.0X, step height repeatability of 6Å, etc [11]. The applications of P6 include 3D imaging, 2D stress analysis, surface roughness measurement, etc.

3.2 Roughness and morphologies measurement by AFM

The atomic force microscopy (AFM) is used to characterize the thin film surface morphology and to measure the surface roughness. The AFM can analyze very weak thickness variation on the sample surface and realize 3D images. The AFM uses a probe, which can scan the film surface. The probe has a sharp tip which is usually on the scale of a few nanometers to a few tens of nanometers and is fabricated typically with piezoresistive element acting like a strain gauge [12]. Depending on the different area on the surface, the deflection of the probe is different. The most common method for the detection of this deflection is producing a laser beam from a laser diode. The laser beam will be reflected from the probe into a photodiode array. The photodiode array treats the reflected laser and produces an output signal to create the 3D image of scanned surface.

In microelectronic and micro-sensor department of IETR, a VEECO model AFM caliber is used. This microscopy has been used to measure the surface roughness of microcrystalline silicon deposited by PECVD, as shown in Figure 2.1 a). This AFM is also used for the determination of surface roughness of PEN or Kapton, as shown in Figure 2.1 b).

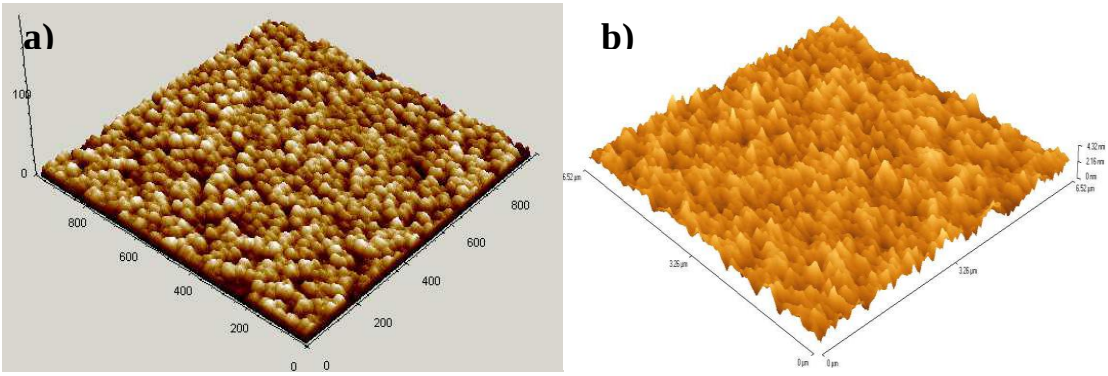

Figure 2.1 a): AFM image of microcrystalline silicon thin film [1], b): AFM image of planarized PEN Q65FA [13]

3.3 Scanning electron microscopy (SEM)

The scanning electron microscopy (SEM) is a simple and fast way to detect the morphology of thin film with high resolution lower than 1 nanometer. The SEM produces electron beam on the sample surface. The electrons interact with atoms in the sample and produce different signal depending on the surface topography. The signal produced is detected by SEM to create an image of sample surface.

In microelectronic and micro-sensor department of IETR, a SEM model JSM 6301 which has a magnification until 1,000,000 times has been used for the analysis of microcrystalline silicon thin film deposited by PECVD [1] and the structure of TFTs fabricated on PEN [13]. The mechanical behavior of TFTs on PEN substrate has been investigated by observing SEM image of TFTs on PEN after mechanical bending. Figure 2.2 presents a mechanical failure of TFTs on PEN after a mechanical bending with curvature radius R = 5 mm from the thesis of S. Janfaoui.

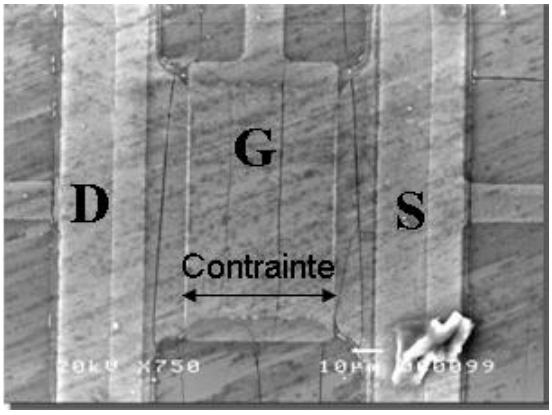

Figure 2.2: SEM image of TFT suffered from a mechanical bending with R = 5 mm [13]

3.4 Measurement of the electrical conductivity

There are 2 methods for electrical conductivity measurement of microcrystalline silicon thin film deposited by PECVD.

The first technology is I-V characteristics measurement. The metallic contact is thermally deposited on the microcrystalline silicon thin film surface. Then, a voltage V is applied between 2 neighboring contacts. By measuring the current passed through these 2 contacts, the conductivity σ is expressed as:

$$\sigma = dI/(L.t.V)(S.cm^{-1})$$

where d is the distance between 2 contacts, I is the measured current, L is the length of the contact pattern, t is the thickness of the film, V is the applied voltage.

This technology is also used for the determination of activation energy of undoped microcrystalline silicon. For this measurement, the microcrystalline silicon thin film will be put under vacuum condition, around 10^{-6} mbar. By measuring the current passing through 2 metal contacts at different temperature, from -150°C to 200°C, the activation energy of undoped microcrystalline silicon can be determined. Indeed, pure and un-contaminated microcrystalline silicon presents activation energy of 0.5 eV. If the sample has some oxygen injection or contamination which will acts like donor in the semiconductors, the activation energy will be lower. Therefore this measurement can be used for the oxygen contamination detection of microcrystalline silicon.

The second method is 4-points measurement [14]. Figure 2.3 shows the simplified demonstration of the 4-points method. For a sample with thickness t, the 4 points are placed on the sample surface with same distance. A current is applied on the two outside points. Then the voltage between the two inside points is measured. The expression of conductivity is:

$$\sigma = 1/\rho(S.cm^{-1})$$

with $$\rho = 4.53.t.V/I\ (\Omega.cm)$$

This expression will be used only when t<<d, the distance between 2 contacts. This technology has been used for the conductivity measurement of doped microcrystalline silicon.

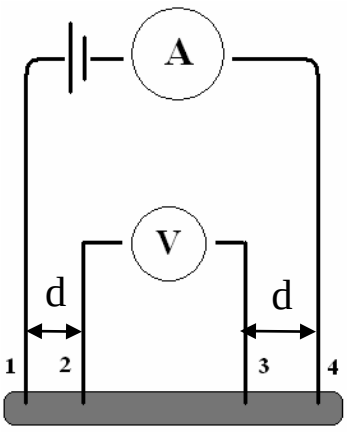

Figure 2.3: Simplified schema of 4-points method for the conductivity measurement [14]

3.5 Measurement of the crystalline fraction of microcrystalline silicon by Raman spectroscopy

The Raman spectroscopy is a common method to analyze the molecular properties of material. The mechanism of this technology is described as follow: when a monochromatic light is induced on a molecule, it will be absorbed or dispersed. Most of the dispersed part of the light is diffused with same frequency υ_0 than incident light. This part is called Rayleigh diffusion or elastic diffusion. Another part of light is diffused with different frequency and is called Raman diffusion or inelastic diffusion. The phenomenon is called Raman Effect. A Raman spectroscopy measures the diffused light as a function of the frequency. The measured Raman spectra presents different vibration mode of analyzed material.

In precedent work, a micro Raman HR 800 (Jobin Yvon) has been used at wave length of 632.8 nm. The crystalline fraction of microcrystalline silicon deposited by PECVD is analyzed by this Raman spectroscopy. Figure 2.4 shows the Raman spectra of a microcrystalline silicon film. This spectrum is dissociated by 3 Gaussian contributions as shown in the figure.

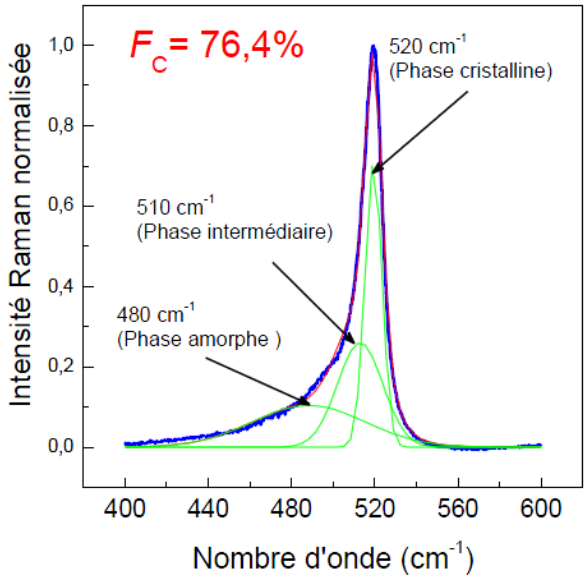

Figure 2.4: Raman spectra of microcrystalline silicon deposited by PECVD [13]

In this figure, the 3 Gaussian contributions represent different crystalline state of the microcrystalline silicon.

- The Gaussian contribution centered at 520 cm^{-1} corresponds to the crystallized phase of the material. The position and the width of the Gaussian contribution is depending on the grain size [15, 16] and the stress inside the material [17].
- The Gaussian contribution centered at 510 cm^{-1} corresponds to the grain joints [18] and the crystallized phase with grain size less than 10 nm [19, 20].
- The Gaussian contribution centered at 480 cm^{-1} corresponds to the amorphous phase.

The crystalline fraction F_C is expressed by the following equation:

$$F_C = (I_C + I_I)/(yI_A + I_I + I_C)$$

where, the I_C, I_I, and I_A are the intensity in the Raman spectra for Gaussian contribution centered at 520 cm^{-1}, 510 cm^{-1}, and 480 cm^{-1}, respectively. y is a corrective term. The value of y depends on the crystalline size and the excitation wave length [21]. In this thesis, the value of y is fixed at y = 1 for the sample analyzed.

4 Fabrication of microcrystalline silicon thin film transistor

The Top-gate TFT, which uses microcrystalline silicon as its active layer needs not only the low temperature deposition technologies, but also the photolithographic equipment which has to be used in the clean-room. The fabrication procedure presented here is not only available for TFT on glass, but also for TFT on plastic. The detailed fabrication steps are:

4.1 Preparation of substrate

The glass or plastic substrate is cleaned by acetone and alcohol for 10 minutes respectively before all the manipulation on the samples in order to eliminate the impurities on the substrate surface. Then the substrate is dried by N_2.

Figure 2.14: Structure obtained after the cleaning of substrate

4.2 Deposition of undoped microcrystalline silicon used as TFT channel

Undoped microcrystalline silicon film used as active layer of TFT is deposited by PECVD. For this deposition, mixture gas of SiH_4, H_2 and Ar is injected in the reactor. The deposition rate is about 3.3nm/minute. Because the deposition temperature is lower than 180°C, TFT fabrication on plastic substrate can be realized. The thickness of this layer is 50 nm or 100 nm.

Figure 2.15: Structure obtained after deposition of undoped microcrystalline silicon

4.3 Deposition of doped microcrystalline silicon

N-type doped microcrystalline silicon film for drain and source region is deposited directly on the undoped film by PECVD using arsine as doping gas. The conductivity of this 70 nm-thick film is about 5S/cm at ambient temperature.

Figure 2.16: Structure obtained after the deposition of doped microcrystalline silicon

4.4 Definition of channel area (Mask 1)

To form the TFT channel area, the doped film has to be etched until the undoped film. This etching can be performed by plasma etching method, RIE (Reactive ion etching). SF_6 is used as the plasma gas. The plasma discharging space is formed between two electrodes using a radio frequency source at 13.56 MHz. Ions are formed and accelerated to the silicon film surface and then react with it. The gas produced from this reaction is then evacuated by the pumping system.

The plasma etching is anisotropic comparing with the wet etching. It means, in the plasma etching, the vertical etching rate is largely faster than the lateral one, providing good reproduction of mask pattern.

In this etching step doped silicon should be completely and carefully removed. The end of this etching can be confirmed by measuring the current level on the etched region.

In IETR, we use a plasma etching machine, Microsys 400 provide by Roth & Rau. By using this machine, thickness of etched material can be known by counting the wave number of reflected interfered laser. The etching conditions are shown in the table 2.5:

Etched material	Reactive gas	Gas flow (sccm)	Pressure (mTorr)	Power (W)	Etching rate (nm/min)
µc-Si	SF_6	10	4	20	≈120

Table 2.5: Plasma etching conditions for µc-Si

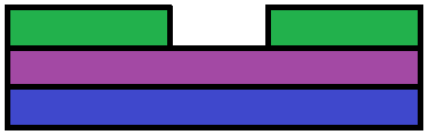

Figure 2.17: Structure obtained after the definition of channel area

4.5 Definition of TFT geometry (Mask 2)

After the channel region has been formed, the undoped silicon is etched until the substrate to define the TFT geometry. The end of this step is clearly visible from the etching machine's monitor.

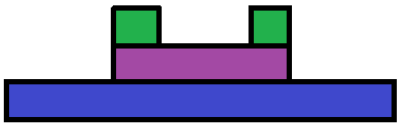

Figure 2.18: Structure obtained after the definition of TFT geometry

4.6 RCA cleaning of the silicon surface

It is well known that the silicon-insulator interface quality is critical for the TFT performance. A RCA cleaning method which ameliorates silicon surface quality is done to improve the interface by eliminating the organic and metallic impurities in the TFT active area.

The mechanism of this RCA cleaning is: create an oxide layer on the silicon surface with a few nanometers thickness in which the organic and metallic impurities are trapped. Then this thin oxide layer is removed. Silicon surface obtained has less contamination. Table 2.6 summarized the operation steps of this RCA cleaning.

Step description	Solution used	Time
Preparation of the solution SC1 Hold the solution at 70°C, then add H_2O_2 solution Put the samples into the solution SC1	H_2O(200mL) + NH_4OH(10mL) + H_2O_2(40mL)	10 minutes
Cleaning in the DI water		10 minutes
Preparation of the solution SC2 Hold the solution at 80°C, then add H_2O_2 solution Put the samples into the solution SC2	H_2O(200mL) + HCL(40mL) + H_2O_2(40mL)	10 minutes
Cleaning in the DI water		10 minutes
Preparation of the deoxidation solution Put the samples into the deoxidation solution based on HF	H_2O(400mL) + HF(16mL)	Until hydrophobia
Cleaning in the DI water		10 minutes

Table 2.6: Detailed steps of RCA cleaning

4.7 Deposition of gate insulator

As mentioned in 2.2 of this chapter, for the gate insulator deposition, different low temperature technologies and materials could be chosen. The materials used as gate insulators are SiO_2, Al_2O_3 and Si_3N_4.

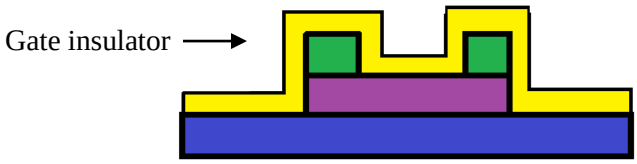

Figure 2.19 Structure obtained after the deposition of gate insulator

4.8 Gate insulator etching for source and drain contact (Mask 3)

The gate insulator material is etched by either plasma or wet etching method in order to get source and drain contact. Table 2.7 a) and b) summarized etching parameters for these two types of etching. The finish of plasma etching is visible from interfered laser monitor of the Microsys 400. On the other hand, the stop of wet etching is determined by hydrophobic phenomena on the silicon surface.

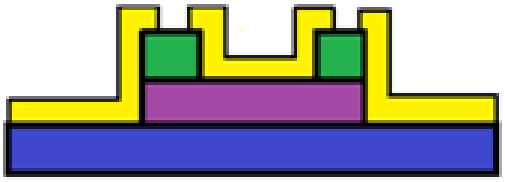

Figure 2.20 Structure obtained after the etching of gate insulator

Material to etch	Reactive gas	Gas flow (sccm)	Pressure (mTorr)	Power (W)	Etching rate (nm/min)
SiO_2	SF_6	10	4	50	≈25
Si_3N_4	SF_6	10	4	20	≈180

Table 2.7 a): Plasma etching parameters for gate insulators

Material to etch	Etching solution	Etching rate (nm/min)
SiO_2	Buffered HF (7%)	200
Al_2O_3	Buffered HF (7%)	70
Si_3N_4	HF (2%)	900

Table 2.7 b): Wet etching parameters for gate insulators

4.9 Deposition of aluminum and definition of source, drain and gate electrode. (Mask 4)

The deposition of aluminum, which is used as source, drain and gate electrode, is deposited by thermal evaporation utilizing joule effect under vacuum condition (10^{-6}mbar). - The aluminum is then wet etched using the conditions as shown in Table 2.8. The etching is finished when the TFT pattern becomes visible by eyes. After the etching, an annealing under nitrogen gas at 180°C is processed in order to improve the contact between doped silicon and aluminum.

Material to etch	Etching solution	Temperature (°C)	Etching rate (nm/min)
Aluminum	701 vol. H_3PO_4(85%) + 28 vol. HNO_3(70%) + 139 vol. CH_3COOH + 132 vol. H_2O DI	50	300

Table 2.8: Wet etching parameters for aluminum

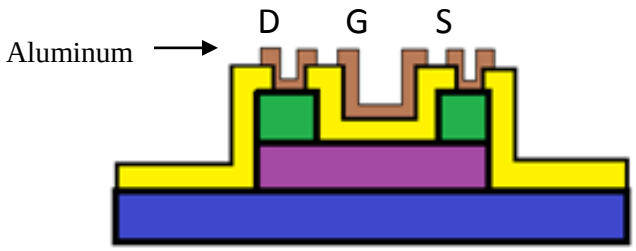

Figure 2.21: Structure obtained after the deposition and etching of aluminum as drain, source and gate electrode

5. Basic working principle and characterization of microcrystalline silicon TFTs

5.1 Basic working principle of TFTs

The basic working principle of microcrystalline silicon TFTs is similar with MOSFET transistors. The performance of microcrystalline silicon TFTs is evaluated by studying some crucial electrical parameters. These parameters that we will analyze for fabricated TFTs are:

- ✓ The threshold voltage V_{TH}
- ✓ The field effect mobility of carriers at on state μ_{FET}
- ✓ The subthreshold slope S
- ✓ The on/off ratio I_{ON}/I_{OFF} and R_{DSON}/R_{DSOFF}

The working of TFT depends on enrichment of carriers. It means when the gate voltage reaches a certain value (V_{TH}), a conductor channel is created by accumulation of major carriers (electrons or holes) in the semiconductor. This channel allows the current passing from source to drain.

a) Off state

When the gate voltage is insufficient to create a channel ($|V_{GS}|<|V_{TH}|$), there is only a weak leakage current, which is called `$I_{Off}$`, between drain and source. This is due to the inverse polarization of drain-channel junction.

b) On state

When the gate voltage becomes lager than V_{TH}, a channel of carriers is created between drain and source. Current can pass through the channel by drain-source polarization. The TFT is in on state.

When TFT is in on state, two operation regimes, linear regime and saturation regime, are defined as shown in the figure 2.23.

5.1.1 Linear regime

For a weak drain voltage ($V_{DS} \leq V_{GS} - V_{TH}$), the drain-source current I_{DS} is expressed by:

$$I_{DS} = \frac{W}{L}\mu C_{OX}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad (2.1)$$

W (μm) : channel width

L (μm) : channel length

μ (cm^2/V.s) : field effect mobility

C_{OX} (F/cm^2) : capacity of gate insulator per unit area

V_{TH} (V) : threshold voltage

For a very weak drain voltage ($V_{DS} << V_{GS} - V_{TH}$), the channel has a constant conductance so the TFT acts like a simple resistance. The value of this resistance is directly depending on the TFT dimension (W/L). The current variation is proportional to the drain-source voltage V_{DS}. Equation (2.2) describes the drain current under very weak drain voltage:

$$I_{DS} = \frac{W}{L}\mu C_{OX}(V_{GS} - V_{TH})V_{DS} \qquad (2.2)$$

From the equation (2), the transconductance g_m and the conductance g_t of the drain are defined as following:

$$g_m = \left\{\frac{\partial I_{DS}}{\partial V_{GS}}\right\}_{V_{DS}=cte} = \frac{W}{L}\mu C_{OX}V_{DS} \qquad (2.3)$$

$$g_t = \left\{\frac{\partial I_{DS}}{\partial V_{DS}}\right\}_{V_{GS}=cte} = \frac{W}{L}\mu C_{OX}(V_{GS} - V_{TH}) \qquad (2.4)$$

5.1.2 Saturation regime

When the V_{DS} reaches the value of $(V_{GS} - V_{TH})$, a pinch-off happens on the drain side. The drain-source voltage is called saturation voltage (V_{Dsat}). From V_{Dsat}, if the drain-source voltage continues to increase, the pinch-off point moves from drain to source. The resistance of the depletion region is very superior compared with channel region, so the drain current retains its value at an approximately constant value called saturation current (I_{Dsat}). The expression of I_{Dsat} is:

$$I_{DSsat} = \frac{W}{L}\mu C_{OX}(V_{GS} - V_{TH})^2 \qquad (2.5)$$

Thus the transconductance can be deduced from the relation as below:

$$g_{msat} = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)_{Vdssat} = \frac{W}{L}\mu C_{OX}(V_{GS} - V_{TH}) \qquad (2.6)$$

5.2 TFTs electrical characteristics

5.2.1 Transfer characteristics

The transfer characteristics corresponds to the measurement of current I_{DS} as a function of the gate voltage V_{GS} for a constant drain voltage V_{DS}. Figure 2.22 presents a typical transfer characteristic of a TFT. From this curve, we can define 4 operation zones of TFT.

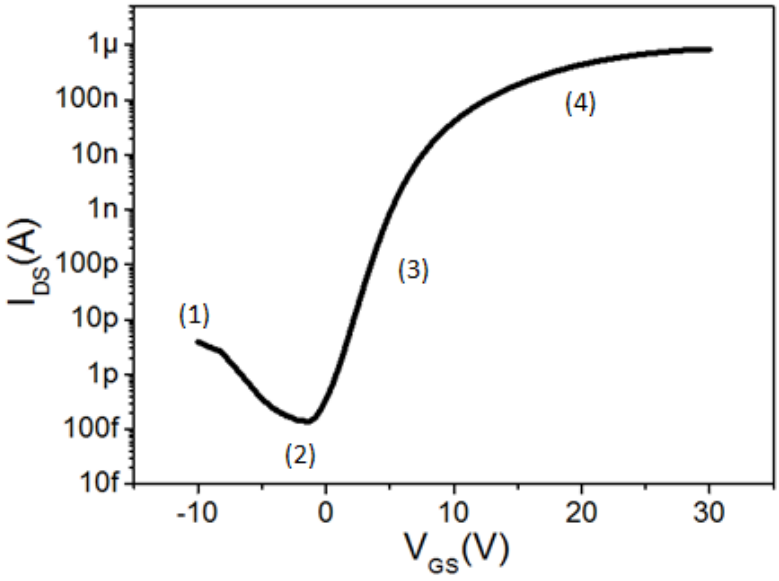

Figure 2.22: Typical transfer characteristic of N-type TFT on semi-logarithmic scale.

The zone 1 represents the TFT behavior in off state with a current (I_{DS}=I_{OFF}) caused by the generation of carriers trapped and accelerated by the strong negative polarization at drain region.

The zone 2 represents the ohmic conduction for the intrinsic materials.

The zone 3 represents that the formation of the channel and the drain current increases rapidly with the gate voltage.

The zone 4 presents the on state of TFT (I_{DS} = I_{ON}).

5.2.2 Output characteristics

The transfer characteristics corresponds to the measurement of current I_{DS} as a function of the gate voltage V_{DS} for a constant gate voltage V_{GS}. Figure 2.23 presents a typical output characteristic of a TFT. This figure presents clearly the linear regime under a weak drain voltage and the saturation regime occurs when V_{DS} becomes lager then (V_{GS} - V_{TH}). This figure shows also the drain current variation with different gate voltages.

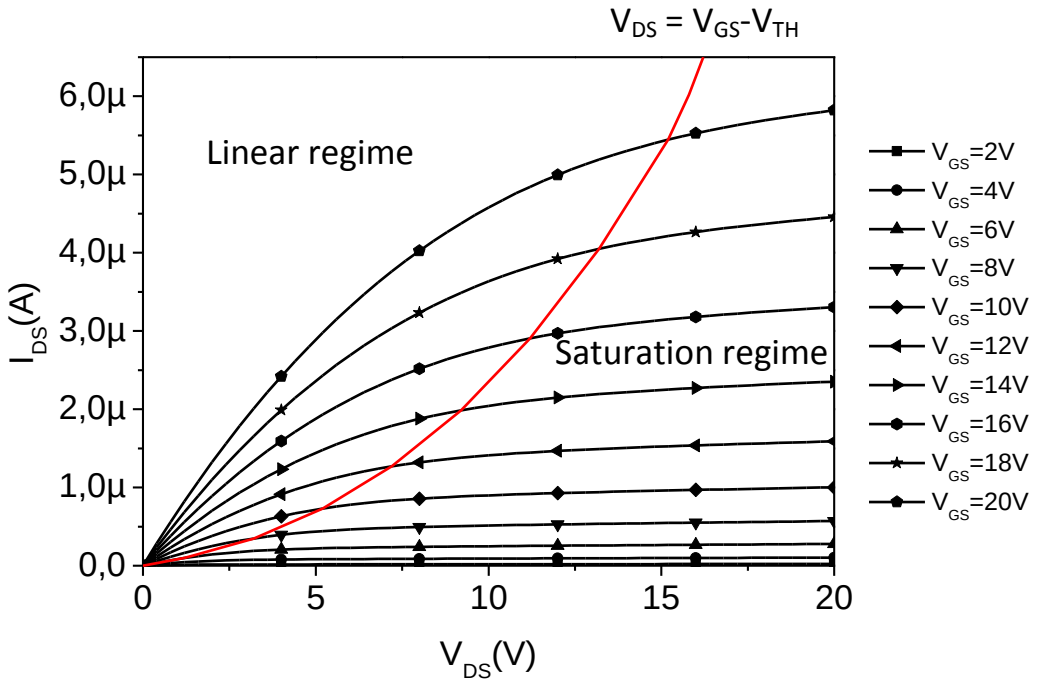

Figure 2.23: Output characteristic of an N-type TFT

5.3 Extraction of characteristics parameters

The characteristics parameters that we can extract from transfer and output characteristics are:

5.3.1 Threshold voltage:

Threshold voltage is a gate voltage value. For a TFT, the strong accumulation of carriers forming the channel happens when the gate voltage applied is superior to threshold voltage.

Threshold voltage represents the limit of TFT conduction. The threshold voltage can be extracted by 2 methods.

In the first method, the threshold voltage is extracted graphically from transfer characteristic $I_{DS} = f(V_{GS})$ of TFT in linear scale. Figure 2.24 presents an example of the extraction of TFT threshold voltage.

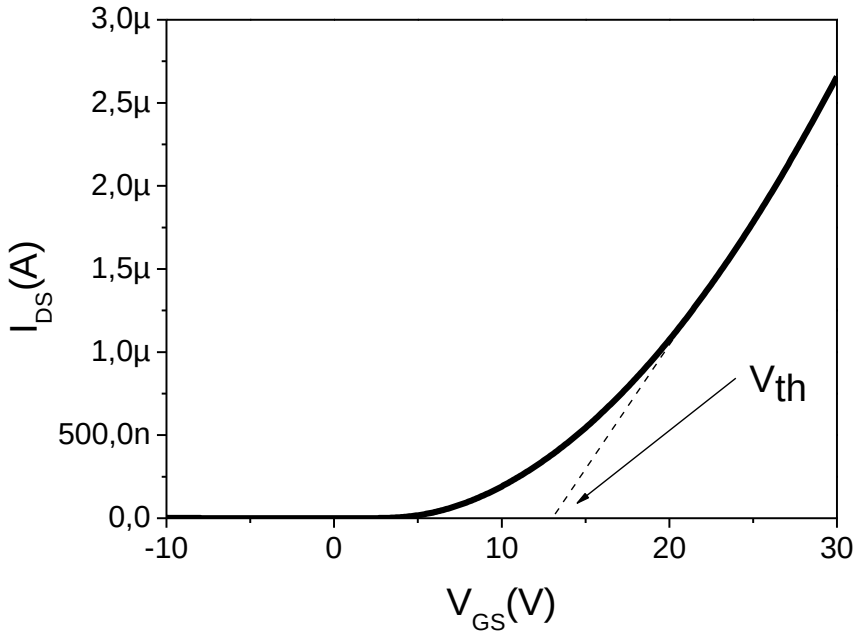

Figure 2.24: Extraction of threshold voltage from $I_{DS}=f(V_{GS})$ of an N-type TFT.

The curve $I_{DS}=f(V_{GS})$ presents a linear part. From this linear part, we draw a tangent line of the curve $I_{DS}=f(V_{GS})$. The threshold voltage value is then read from the node of the tangent line and drain current axis ($I_{DS}=0$).

The second method uses output characteristic to extract the threshold voltage. As mentioned in equation (2.5), the saturation current of TFT can be expressed as:

$$I_{DSsat} = \frac{W}{L}\mu C_{OX}(V_{GS} - V_{TH})^2 \qquad (2.5)$$

Output characteristic of TFT presents $I_{DS} = f(V_{DS})$ under different V_{GS}. On the other hand, from Output characteristic, we can extract $I_{DS} = f(V_{GS})$ for a fixed V_{DS}. Figure 2.25 shows an

example of $I_{DS} = f(V_{GS})$ in saturation regime. According to equation (2.5), the saturation current of TFT, $I_{DSsat} = f(V_{GS})$ can be fitted as:

$$I_{DSsat} = P_1(V_{GS} - P_2)^{P_3} \qquad (2.7)$$

where, P_1, P_2 and P_3 are the fitting parameters. The threshold voltage value is equal to the fitting parameter P_2.

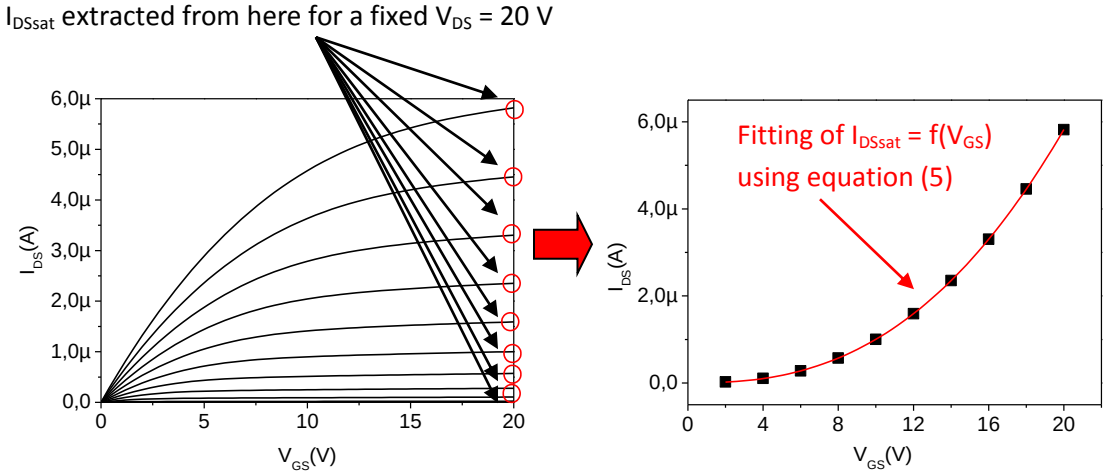

Figure 2.25: Example of the extraction of threshold voltage from output characteristic of an N-type TFT. Fitting of $I_{DSsat} = f(V_{GS})$ using equation (2.5) in order to extract V_{TH} of TFT.

5.3.2 Field effect mobility

The field effect mobility represents how fast transport the carriers in the TFT active layer. The expression of field effect mobility is:

$$\mu = g_m \frac{L}{W} \frac{1}{C_{OX}} \frac{1}{V_{DS}} \qquad (2.8)$$

where the g_m is the transconductance (Equation (2.3)) which corresponds the slope of curve $I_{DS}=f(V_{GS})$. The mobility is expressed in $cm^2/V.s$.

The mobility can also be extracted from output characteristic of TFT using the same method for V_{TH} extraction. Indeed, in equation (2.7), the fitting parameter P_2 corresponds to

the threshold voltage and P_1 corresponds to the value of $\mu C_{OX}W/L$. Therefore, the mobility can be expressed as:

$$\mu = \frac{P_1 L}{C_{OX} W} \qquad (2.9)$$

Like threshold voltage, the mobility is an important parameter which gives us the TFT performance information. Higher is the mobility, lager is the drain current can be driven by TFT. As shown in equation (1) and (5), the drain current of TFT is proportional to $\mu W/L$. For a fixed drain current of TFT, higher mobility leads to lower value of W/L. Therefore, high mobility makes TFT smaller when the drain current is fixed. The smaller TFT is important for high integration applications such as high-resolution displays. The high mobility is thus need for these applications.

On the other hand, the high mobility can increase the response speed of TFT. Indeed, the cutoff frequency of TFT, F_C, can be expressed as:

$$F_C = \frac{\mu V_{DS}}{L^2} \qquad (2.10)$$

Obviously, the cutoff frequency of TFT is proportional to mobility. High mobility is essential for some high-frequency applications of TFT.

5.3.3 Subthreshold slope

The subthreshold slope corresponds to the gate voltage value applied for increase the drain current for one decade (when the voltage is inferior to the threshold voltage). The subthreshold slope depends largely on the defects in the silicon and at the interface insulator/semiconductor. Its value is extracted from the log-linear plot of the transfer characteristics. This value is expressed in V/dec. and corresponds to the facility of the channel forming.

$$S = \left(\frac{\partial V_{GS}}{\partial (\log(I_{DS}))} \right)_{V_{DS}=cte} \qquad (2.11)$$

The subthreshold slope depends largely on the defects in the silicon and at the interface insulator/semiconductor. Indeed, the subthreshold slope can also be expressed as:

$$S = \frac{kT}{q} \times \ln 10 \times \left\{1 + \frac{C_{IT}+C_{EP}}{C_{INS}}\right\} \qquad (2.12)$$

where C_{INS} is the capacity per unit area of the gate insulator, C_{IT} and C_{EP} present the capacitance corresponds to trap sites at gate insulator/active layer interface and inside the grain boundary, respectively. Therefore, a high subthreshold slope value of TFT indicates a large number of trap sites in the channel of TFT or at the gate insulator/active layer interface.

5.3.4 The I_{ON}/I_{OFF} and R_{DSON}/R_{DSOFF} ratio

The I_{ON}/I_{OFF} ratio presents the difference between off state and on state current. Higher is the I_{ON}/I_{OFF}, better is the TFT performance. These two current value, I_{ON} and I_{OFF}, are extracted from the curve $I_{DS}=f(V_{GS})$ in linear-logarithmic plot. I_{ON} corresponds to the maximum current on the transfer characteristic and I_{OFF} represents the minimum current at off state.

Another important parameter to distinguish the on/off state of TFT is R_{DSON}/R_{DSOFF} ratio. This parameter is extracted from output characteristic of TFT. R_{DSON} and R_{DSOFF} present the drain-source resistance in saturation regime and linear regime of TFT, respectively. Higher is the R_{DSON}/R_{DSOFF}, better is the TFT performance. R_{DSON} is extracted from the slope of output characteristic of TFT in saturation regime, where the V_{DS} is high and V_{GS} is low, and the R_{DSOFF} is form the slope in linear regime, where the V_{DS} is low and V_{GS} is high, as shown in Figure 2.25.

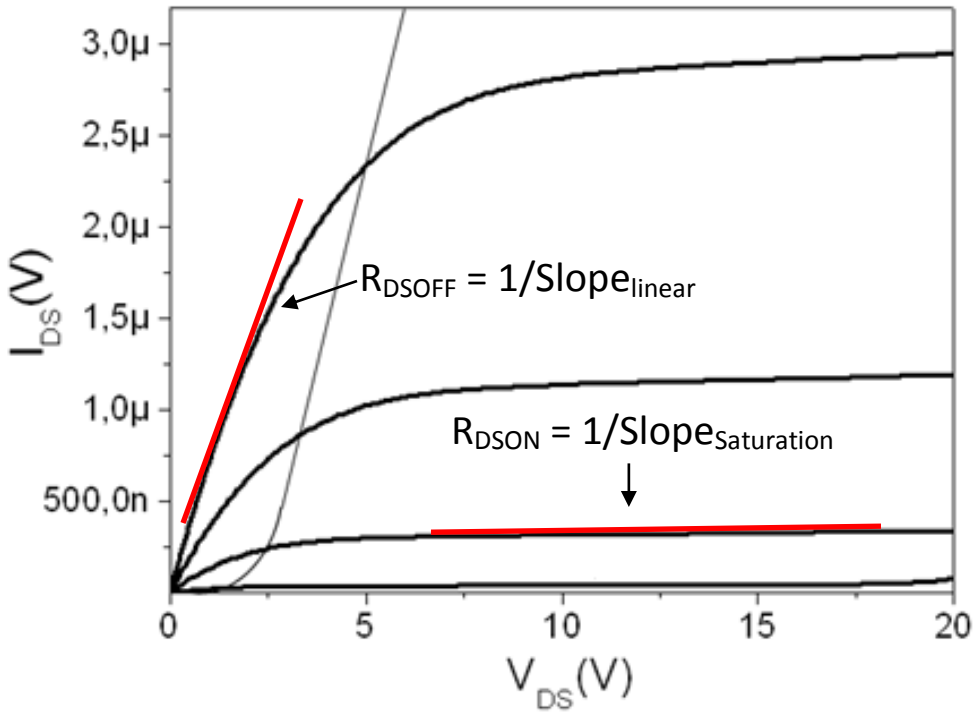

Figure 2.25: Extraction of R_{DSON} and R_{DSOFF} from output characteristic of TFT.

6. Conclusion

The technology of microcrystalline silicon TFTs fabricated at temperature lower than 180 °C have been developed and optimized in the microelectronic and micro-sensor department of IETR since 2004. The substrates used for this process are glass and PEN.

The active layer of TFTs is undoped microcrystalline silicon. This layer is deposited at 165 °C using silane, hydrogen and argon. The quality of the active layer is benefited from the adding of argon into the deposition gases. The activation energy of the active layer is in the range of 0.4 eV to 0.6 eV. The crystalline fraction is in the range of 73% to 78%.

There are several low-temperature deposited materials that can be used as gate insulator of TFT, including SiO_2 deposited by sputtering and ECR-CVD, Al_2O_3 deposited by ALD and Si_3N_4 deposited by PECVD.

The low temperature deposition technologies of active layer and gate insulators will be utilized in Chapter 3 and Chapter 4 for the fabrication of microcrystalline silicon TFT on glass and PEN substrate.

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State-of-the-art and problematic of microcrystalline silicon TFT technology in IETR laboratory

State-of-the-art of microcrystalline silicon TFT technology in IETR laboratory

Microcrystalline silicon TFTs fabricated on flexible substrate, PEN, have been realized and studied in the precedent works in IETR [1-3]. The main goal of these previous works was the development of low temperature TFT's process based on microcrystalline silicon. The maximum temperature of the process that is compatible with usual flexible and transparent plastic substrate, was fixed at 180°C. This temperature is compatible with PolyEthylene Naphtalate (PEN) substrate developed by Dupont Teijin Films under the reference TEONEX Q65FA. Its thermal shrinkage is lower than 0.1% at 180°C. Microcrystalline silicon was chosen due to the ability to produce both N-Type and P-type transistors leading to efficient CMOS electronics when using it. The other reason was its assumed much better stability than amorphous silicon.

Firstly the TFTs on glass substrate were fabricated at temperature lower than 180 °C. Two gate insulator materials, silicon nitride deposited by PECVD and silicon oxide deposited by sputtering, have been studied. The following figures present microcrystalline silicon TFTs, fabricated in previous thesis in IETR [2], using these two gate insulators.

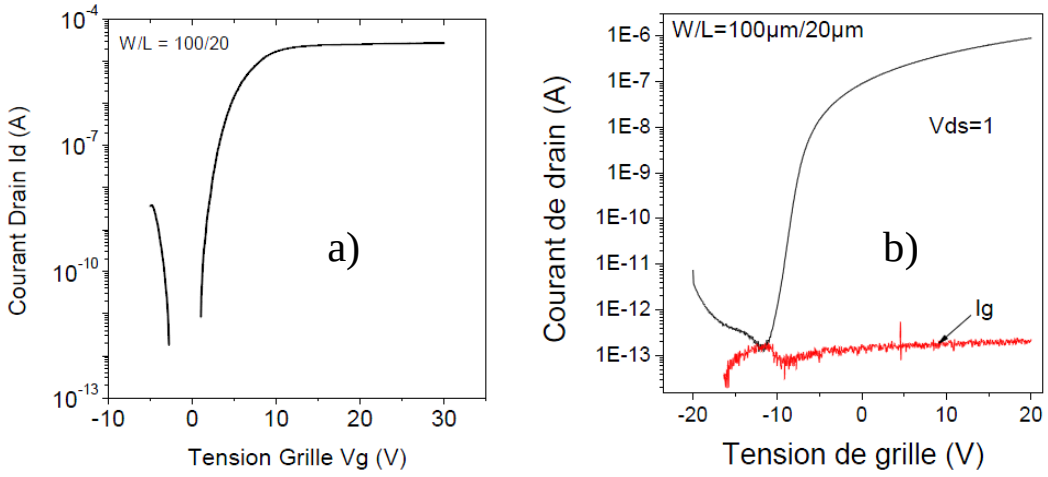

Figure 1 a): Transfer characteristic of TFTs using silicon oxide as gate insulator [2], b): Transfer characteristic of TFTs using silicon nitride as gate insulator [2]

The TFTs with silicon oxide as gate insulator present high mobility, 40 cm²/V.s. But their electrical stability was very poor. On the contrary, the mobility is very weak (on the order of 1 cm^2/V.s) and the electrical stability very excellent when using silicon nitride deposited by PECVD at 150°C as gate insulator.

CMOS simple circuits as inverters and ring oscillators were also fabricated on glass at a maximum temperature of 180 °C during the process [1, 2]. The process was transferred on PEN sheets leading to first TFTs and CMOS inverters produced on flexible and transparent substrate. Their behavior under mechanical strain was studied [3]. Although the maximum process temperature used by K. Kandoussi and K. Belarbi is sufficiently low for the substrate, some technical issues exist concerning the PEN substrate. S. Janfaoui has studied on the technical optimization of fabrication process of TFTs on PEN substrate. Then he has also studied the electrical stability and mechanical behavior of TFTs on PEN substrate.

Figure 2 presents a comparison of our microcrystalline silicon TFTs on glass and on PEN substrate. Their electrical parameters are summarized in Table 1.

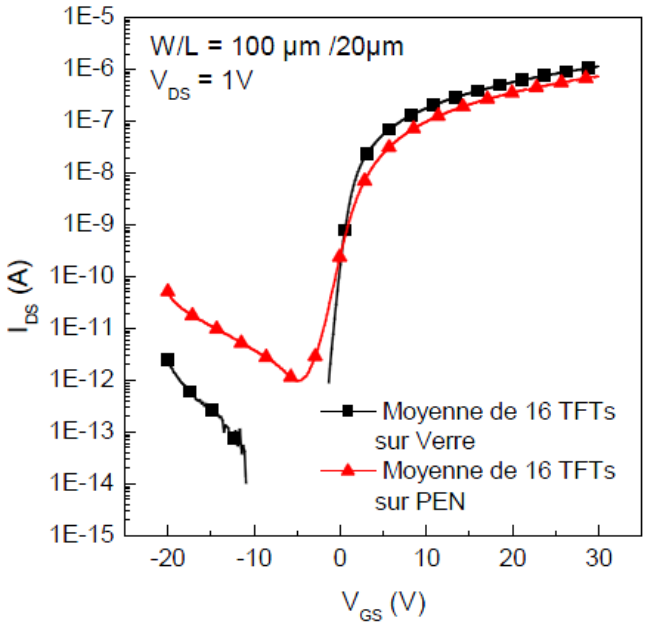

Figure 2: Comparison between the mean transfer characteristics of TFTs fabricated on glass and on PEN

The TFTs on glass present higher I_{on}/I_{off} ratio, higher mobility and lower subthreshold slop than TFTs on PEN. Moreover, The TFTs on PEN present higher standard deviation of threshold voltage and mobility than that of TFTs on glass. This comparison indicates the degradations happened when the TFTs are fabricated on PEN substrate. To explain these degradations, S. Janfaoui demonstrated 2 explications. The first one is higher surface roughness of PEN. The second one might be more important. That is the different detail during RCA cleaning. For the glass substrate, a typical RCA cleaning process as mentioned in Table 2.6 is used, i.e. 10 minutes in SC1, 10 minutes in SC2 and 10 second in HF. On the other hand, the TFTs on PEN have silicon nitride, which are easily attacked by acid solution like HF, as encapsulation layer on the substrate. The time of HF deoxidation has been forced to be reduced to 2 second in order to protect device from acid attack. This 2 second deoxidation might be insufficient for the remove of all the oxidations and contaminations on the silicon surface.

	Mean V_{TH} (V)	Standard deviation of V_{TH} (V)	Mean µ (cm^2/Vs)	Standard deviation of µ (cm^2/Vs)	Mean S (V/Dec)	Mean I_{ON}/I_{OFF}
glass	11.68	0.17	0.7	0.006	0.66	$>10^7$
PEN	12.19	0.52	0.46	0.013	1.35	$>10^6$

Table 1: Comparison of electrical parameters of TFTs fabricated on glass and on PEN

The mechanical behavior of TFTs on PEN substrate is studied by applying tensile and compressive deformations with different curvature radii. Different curvature radii induce different mechanical strain in tension and in compression. The mechanical strain causes the variation of characteristics of TFTs. In the thesis of S. Janfaoui, uniaxial tensile and compressive strain is applied on TFTs on PEN and the transfer characteristics are measured during the bending. Figure 3 a) and b) represent the relative variation of threshold voltage and mobility of TFTs on PEN as a function of tensile strain. Indeed, different trends of both parameters have been found N-type or P-type, crystallized or non-crystallized silicon TFTs. These trends depend on the type of TFTs and the type of bending. Table 2 summarized the different trends of both parameters.

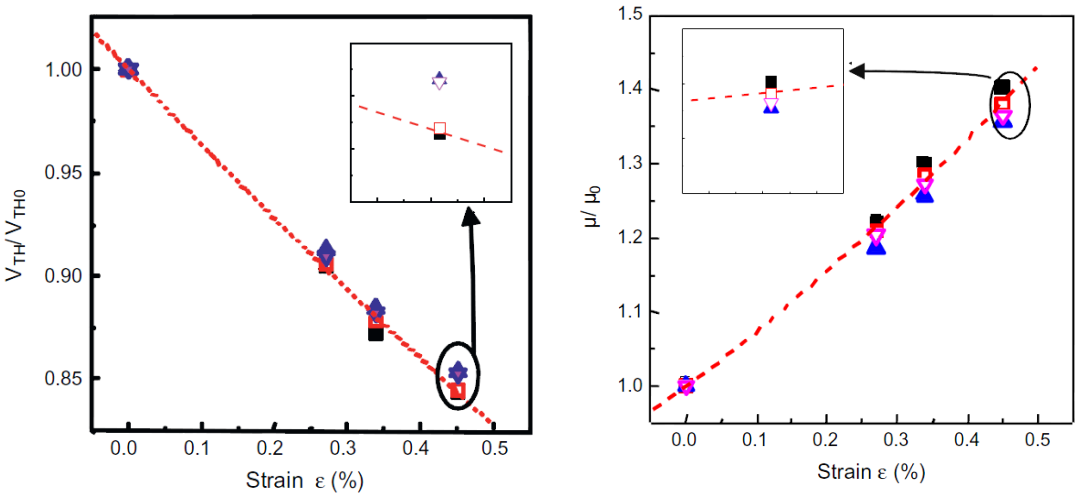

Figure 3: Relative variation of a) threshold voltage and b) mobility of microcrystalline silicon TFTs on PEN as a function of tensile strain

Stress	TFT	V_{TH} trend	μ trend
Tensile	N	Decrease	Increase
	P	Increase	Decrease
Compressive	N	Increase	Decrease
	P	Decrease	Increase

Table 2.7: Trend of the threshold voltage VTH and the mobility μ for N-type and P-type microcrystalline silicon TFTs fabricated on PEN under tensile and compressive stress [3]

Problematic of works on microcrystalline silicon TFT in IETR laboratory

From these previous works, it can be possible to notice 2 main problems.

The first one concerns the mechanical behavior of the TFTs fabricated on flexible substrate. The minimum curvature radius that can hold these TFTs without losing their performance was found higher than 1 cm. The main goal of the previous works and the present one is the development of flexible electronics requiring high flexibility and bendability to be able to be fold nearly in two. Curvature radius of a few millimeters is then needed.

The second problem concerns the field effect mobility value and its link with the electrical stability. As mentioned before, when using silicon dioxide deposited by RF sputtering as gate insulator, TFTs present thigh mobility but very poor electrical stability [2]. On the contrary, the mobility is very weak and the electrical stability very excellent when using silicon nitride deposited by PECVD at 150°C as gate insulator. Silicon dioxide deposited on microcrystalline silicon produces high interface quality leading to high mobility but poor stability due to oxygen penetration in silicon during the Sputtering deposition [1].

Both problems will be addressed in the following chapters 3 and 4.

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Chapter 3: Flexible microcrystalline silicon TFTs: Stability and flexibility

1. Introduction

Present chapter is devoted to flexible TFTs that can hold lowest possible curvature radius. TFTs fabricated on glass will be presented first. These TFTs were previously studied in IETR. Here, complementary studies, concerning the important problem of the electrical stability, will be described.

Then new TFT's process leading to high flexibility will be described and the mechanical behavior of these TFTs presented and discussed

2. TFTs fabricated at low temperature compatible with the use of transparent flexible substrate

Before fabricating TFTs on flexible substrate, we will optimize the TFT's process on glass substrate that has to be easily transferred on plastics. Previous works made in IETR have developed this process. Here, we continue this development studying particularly the TFT's reliability and trying to explain the origin of the slight change of TFT's characteristics during the functioning.

2.1 Electrical characterization of TFTs

µc-Si TFTs was fabricated following the process described in chapter 2. The process used in this work starts by cleaning the glass substrate and then depositing 2 successive microcrystalline silicon films. The first 100 µm thick one is undoped. The second 70 µm thick one is arsenic doped (N-type).

Then the doped film is totally but carefully removed by SF_6 etching to define the channel zone. The success in this etching step determines the reproducibility of the process.

After removing both doped and undoped films to define the total area of the TFT, the surface of undoped film in the channel zone is cleaned to prepare it for the gate insulator deposition. This cleaning and the time between it and the deposition of the insulator are the second challenge contributing to the success of the process.

Silicon nitride was chosen here as gate insulator. Its deposition was previously optimized at 150°C in IETR [1]. TFTs using silicon nitride as gate insulator presents outstanding stability comparing with the TFTs using silicon oxide as gate insulator. The thickness of silicon nitride was chosen to be 300 nm here.

Windows were opened in this gate insulator to define the zones of drain and source contacts. Deposition of aluminum and its etching followed, forming then source, drain and gate contacts.

An example of the transfer characteristics of the TFTs fabricated here is shown in Figure 3.1. The electrical parameters of this TFT are summarized in Table 3.1. The off-current is very weak for this type of TFT, 1.6 pA at V_{GS} = -20 V and 23 pA at V_{GS} = -30V, demonstrating the high quality of the gate insulator.

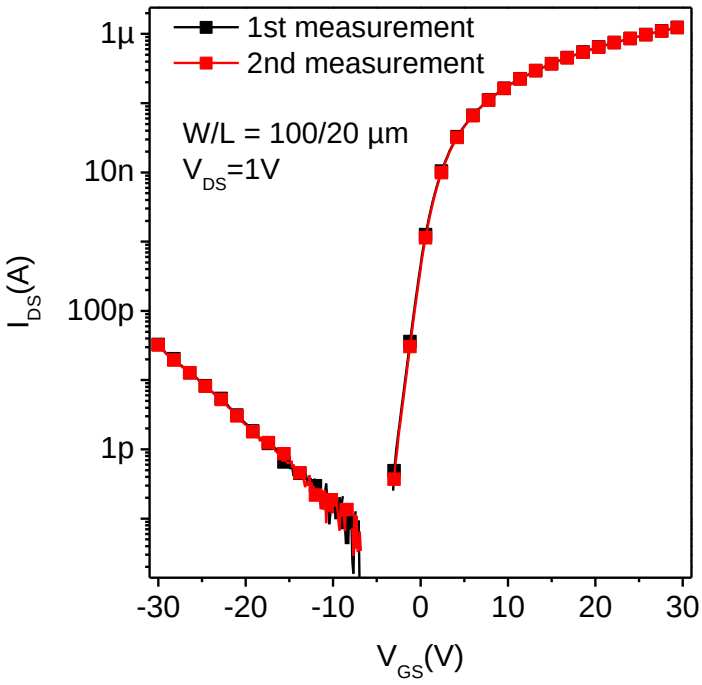

Figure 3.1: 2 successive measurements of transfer characteristic of microcrystalline silicon using silicon nitride as gate insulator

Mobility (cm²/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)
0.77	1.1	10.12

Table 3.1: Electrical parameters of microcrystalline TFT using PECVD deposited silicon nitride as gate insulator

Even if the off-current is very low and the subthreshold slope and threshold voltage acceptable, the mobility is low, lower than 1 $cm^2/V.s$. Low mobility can be acceptable when not so high working frequency is needed. Particularly, mechanical or chemical sensors do not need high frequency. In this case, reliable electronics is much more important. It is important to check now the reliability of present TFTs.

2.2 Electrical stability of microcrystalline silicon TFTs

Reliability of TFTs can concern their long term functioning. An accelerated ageing consists on applying high gate voltage, higher than its value in usual functioning, during a long time, following the behavior of the TFT's parameters. This ageing, named gate bias stress, causes threshold voltage shift in disordered material based transistors. Amorphous silicon (a-Si:H) based TFTs, for example, are known for the large shift of the threshold voltage during this stress. Microcrystalline silicon TFTs are less sensitive to this stress due to their crystallinity. As mentioned in Chapter 1, two instability mechanisms are widely accepted for a-Si:H TFTs: 1) defect creation in a-Si:H and 2) charge trapping in the gate insulator. However these mechanisms are also involved for other materials. The first mechanism is involved in most of disordered materials. The second mechanism describes the trapping of carriers coming from the transistor channel inside gate insulator containing defects. In this section, the same mechanisms and instability models are induced for microcrystalline silicon TFTs in order to define the dominant mechanism of instability.

2.2.1 Threshold voltage shift models

The defect creation in a-Si:H or in disordered regions in microcrystalline silicon is caused by reaction between electron and weak Si-Si bonds, producing dangling bonds, which is negatively charged and will trap electrons. The defect creation and the band-banding caused by the dangling bonds are shown in Figure 3.2 a) [2] and b) [3], respectively. By applying gate bias stress, these dangling bonds are created and then the TFT need higher gate voltage to be turned on. Therefore, the threshold voltage shifts. The defect creation in disordered silicon involves mainly the behavior of hydrogen inside the material using diffusion controlled models [4]. However, other models involve only an exponential distribution of weak Si-Si bond energies without hydrogen diffusion [5].

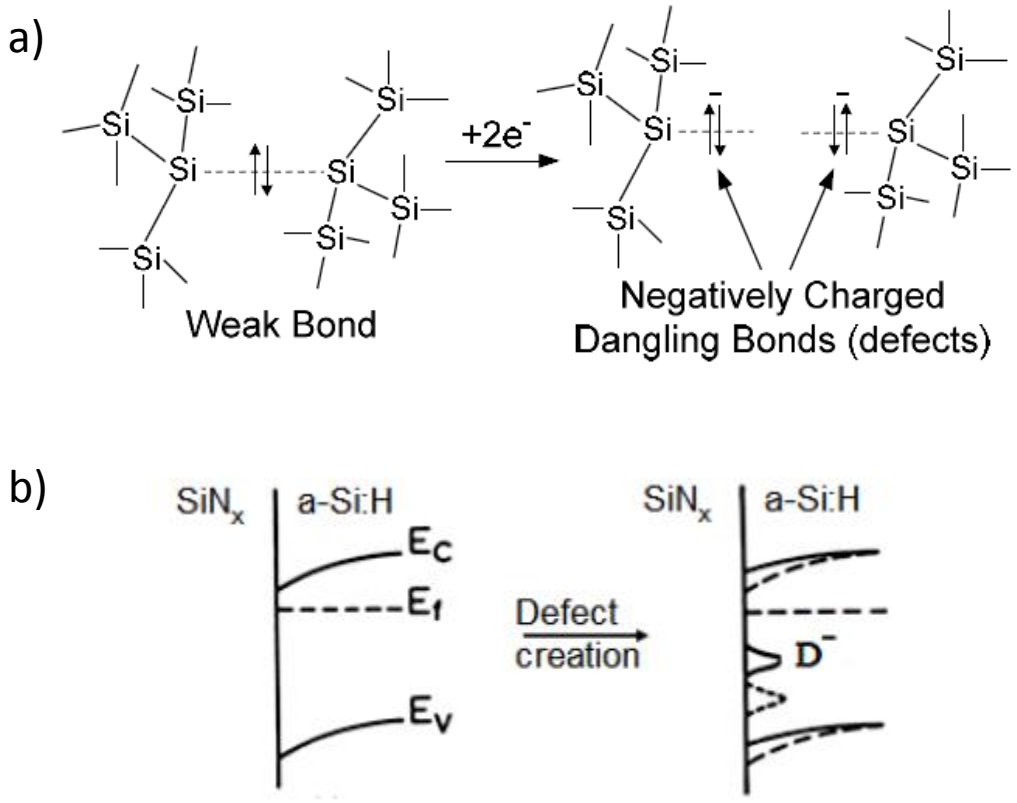

Figure 3.2: a) Defect creation in silicon [2] b) Band-bending diagram after defect creation [3]

Both types of models occur on the same equation giving the kinetics of defect-creation and relaxation with the same parameters. This equation, named stretched exponential law, is given by:

$$V_{TH}(t) - V_{TH}(0) = (V_{GStress} - V_{TH}(0)) \left\{ 1 - \exp\left[-(t/t_0)^{\beta} \right] \right\} \qquad (3.1)$$

where $V_{Gstress}$ is the gate voltage applied during the stress, $V_{TH}(0)$ is the initial threshold voltage, t_0 and β are fit parameters.

This stretched exponential law is usually involved generally to describe relaxation phenomena in glasses towards equilibrium under different stresses [6]. It was established that considered particles diffuse in a medium containing randomly distributed states in the space, able to trap these particles [7]. It is involved in disordered structures to describe the time behavior of different parameters like the conductivity [8], the threshold voltage of TFTs [4] or the magnetization [6]. In amorphous silicon TFTs, this effect has been associated to a dispersive diffusion coefficient of atomic hydrogen [4]. This dispersion comes from the nature of any disordered medium where the trapping sites present a distribution of energy states. The β parameter is linked to this distribution of states and to the temperature.

This law is general enough to be used in the effect description of any stress applied to a wide panel of situations like in glasses, at the disordered interface between the gate insulator and the channel in single crystalline silicon based MOSFETs [9], and in polycrystalline silicon based TFTs, where dispersive diffusion in disorder structure can be involved. We can assume that in disordered structures, any energy absorption inducing new charge carriers distribution can change the state of the weakest bonds disturbing the not-stable equilibrium. The deformation can diffuse leading to a new equilibrium characterized by new defect distribution.

The second model is the trapping one. It involves an injection of carriers inside the gate insulator due to the applied gate bias. These carriers are trapped inside the insulator fixing an electrical charge inside it. Consequently, the effective gate voltage inducing the charge accumulation in the channel changes leads to a variation of the drain-source current

Figure 3.3 a) and b show the charge trapping mechanism and the induced band-banding diagram, respectively.

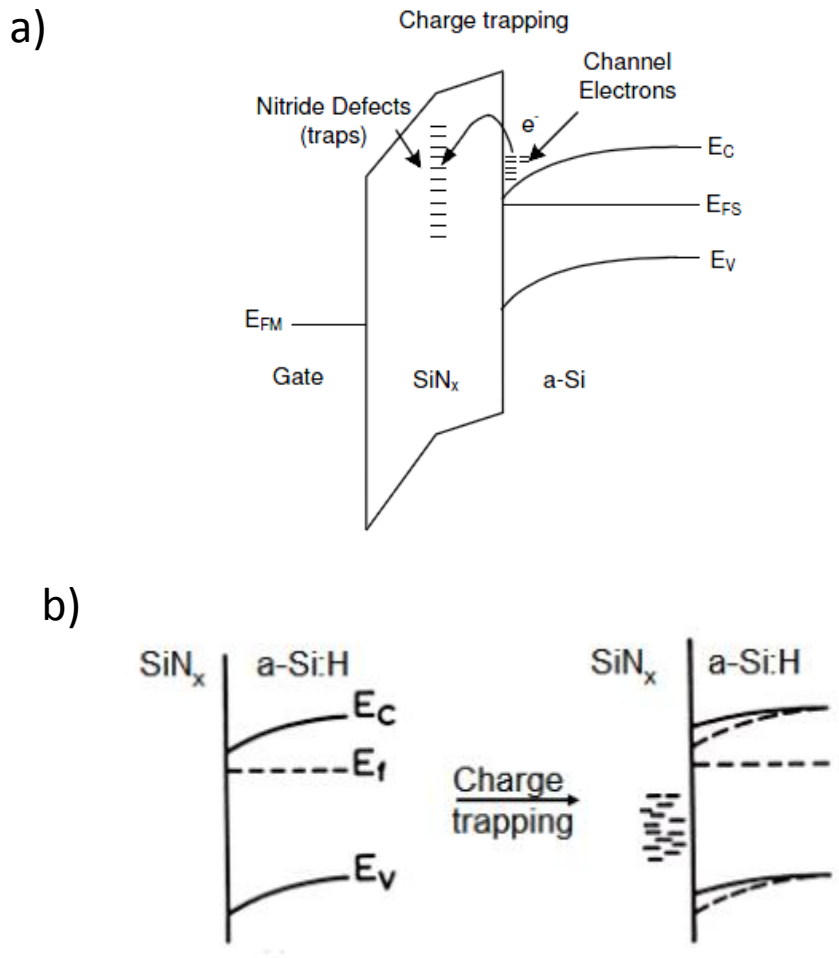

Figure 3.3: a) Charge trapping in gate insulator [6] b) Band-bending diagram after charge trapping [8]

When this trapping mechanism is involved, the threshold voltage shift vs. time can be expressed by a logarithmic law as following [10].

$$V_{TH}(t) - V_{TH}(0) = r_d \log\left(1 + \frac{t}{t_0}\right) \qquad (3.2)$$

where $V_{TH}(t)$ is the threshold voltage at the stress time t, $V_{TH}(0)$ is its initial threshold, r_d and t_0 are fit parameters. r_d is a decay rate constant which is proportional to density of traps inside the gate insulator N_{tr} (cm^{-3}) and λ (cm) a tunneling constant [11].

It is difficult to define the dominant mechanism that causing the threshold voltage shift in microcrystalline silicon TFT. However, the crystalline structure insures a much better stability to microcrystalline silicon comparing to amorphous silicon. In this case, trapping inside the gate insulator can be dominant for microcrystalline silicon TFTs.

2.2.2 Gate bias stress for microcrystalline silicon TFTs

Gate bias stress has been applied on microcrystalline silicon TFTs fabricated as described before. The stresses have been realized with different gate bias stress voltages and measurement temperatures. Fixed 35V stress gate voltage ($V_{GSstress}$) is applied to the transistor when source and drain contacts are short-circuited. 35V is much higher than the threshold voltage that is around 11V for this type of TFTs. This means that TFTs are strongly in on-state during the stress even if the source-drain voltage is 0. The duration of the stress is 5.5 hours. During the stress, the transfer characteristics are measured each 10 minutes. At the end of this stress, gate and source are short-circuited and then the transfer characteristics are measured each 10 minutes.

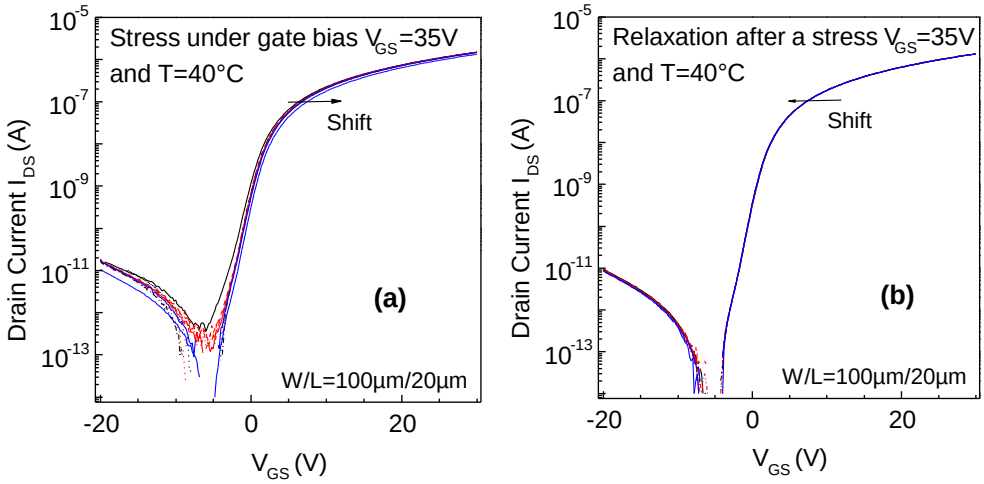

Figure 3.4: a) transfer characteristics of TFTs plotted some times during the 35V gate bias stress at 40°C, or b) during the relaxation (V_{GS}=0, V_{DS}=0) after the previous stress.

Figure 3.4 a) shows the transfer characteristics of TFTs plotted some times during the 35V gate bias stress at 40°C. The TFT's channel is 100 µm wide (W) and 20 µm long (L). The curves shift towards higher gate voltage during the stress. However the shift is very small comparing to the threshold voltage. Figure 3.4 b) shows the behavior of the transfer characteristics during the relaxation. The curves shift towards lower gate voltage. It seems the threshold voltage comes back towards its initial value before the stress. However, the shift during the relaxation is low, meaning a not complete recovery. The behavior of the shift of the threshold voltage during both the stress and the relaxation is shown if figure 3.5.

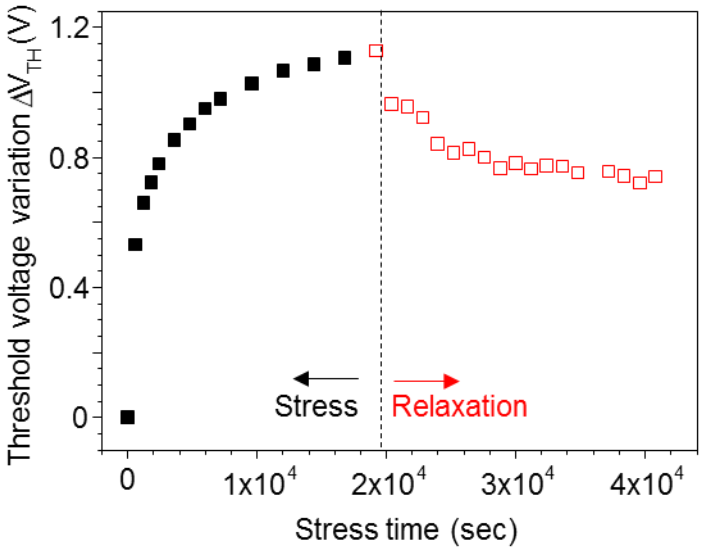

Figure 3.5: Shift of the threshold voltage during a 35V gate bias stress at 40°C and during the following relaxation with V_{GS}=0V.

Firstly, the threshold voltage variation during the stress is fitted by the stretched exponential law (equation 3.1), describing a state creation. The fit is shown in figure 3.6. The fitting parameters, β, describing the extent of the defect distribution inside the active layer, and t_0, the time constant for the defect creation, are 0.20 and $4.5x10^{10}$ seconds respectively. The time constant is similar to the usual value found for a-Si:H TFTs [12]. However, the present experimental threshold voltage shift, 1.1V after 5.5 hours of 35V gate bias stress at 40°C, is much weaker than the usual one found for a-Si:H TFTs [12]. The structure of µc-Si films deposited in the present work is obviously well crystallized with a Raman crystalline fraction higher than 70% and then it is far from amorphous. Moreover, in the defect creation

model the parameter β is given by the ratio T/T_0 [13] where T is the temperature during the stress and T_0 is the characteristic temperature of hydrogen hopping energies that are around 600-700K. With β=0.20 and T=40°C=313K, the experimental value of T_0 is 1565K, much higher than expected.

Finally, making the same stress but at other temperatures, 30°C and 50°C for example, and fitting the threshold voltage shift by stretched exponential law, we obtain 0.18 and 0.17 for β parameter and $6.8x10^{11}$ s and $4.6x10^{10}$ s for t_0 parameter. β values are much lower than expected giving incredible values for T_0. Moreover β is lower than its value at 40°C for both 30°C and 50°C temperatures. t_0 at 50°C is the same than its values at 40°C. β value have to increase with the temperature and t_0 value to decrease with the temperature in the defect creation model. Here no such behaviors are observed. It seems the fit fully not reliable.

Similarly to the fit of the shift during the stress, the shift of the threshold voltage during the relaxation has been fitted by a stretched exponential curve. Here, exactly we used the next equation:

$$\Delta V_{TH} = V_{TH}(t) - V_{THStress} = -(V_{THStress} - V_{TH}(0))\left\{1 - \exp\left[-\left(\frac{(t - t_{Stress})}{t_0}\right)^{\beta}\right]\right\} \qquad (3.3)$$

where $V_{THStress}$ and t_{Stress} are the threshold voltage and the time at the end of the stress respectively.

The fit is shown in figure 3.6. The fitting parameters, β and t_0, 0.49 and $9.7x10^3$ seconds respectively. The time constant is much lower than its value during the stress. This means that the kinetics of the defect creation and relaxation are very different in the contrary of the expected result where both kinetics are similar [4, 5].

With all these arguments, it seems difficult to attribute the present threshold shift to defect creation.

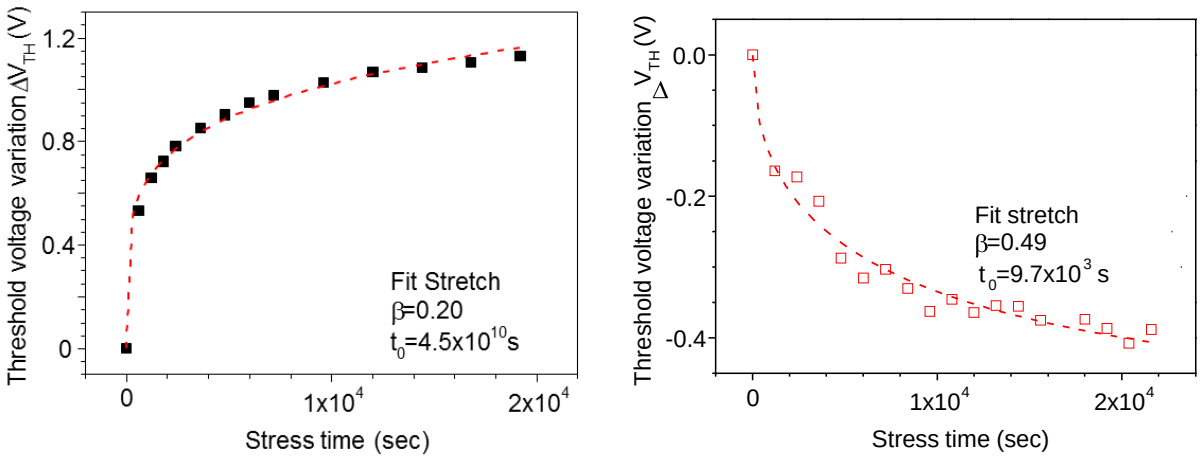

Figure 3.6: Fit of the shift of the threshold voltage during a 35V gate bias stress at 40°C and during the following relaxation with V_{GS} = 0. The fit uses the stretched exponential law (equation 3.2). The fitting parameters β and t_0 are given in the insets.

The second possible model to explain the shift of the threshold voltage is carrier trapping inside the gate insulator. To check this possibility, gate bias stress has been performed also at constant temperature 25°C and 3 values of the stress bias, 30V, 35V, and 40V.

Figure 3.7 a) to c) represent the transfer characteristics measured at different time during these gate bias stresses. Obviously, the shift increases with the stress voltage but stays very low. Plotting the threshold voltage shift vs. time at these different stress voltages (Figure 3.8) confirms this observation. The other observation is that the curves seem parallel indicating constant subthreshold slope.

The fit with the carrier trapping equation 3.2 is very good as demonstrated by the correlation factor of the fit R^2 given inside figure 3.8.

Similarly, the fit with the carrier trapping equation 3.2 of the threshold voltage shift during the gate bias stress made at 35V stress gate voltage and 30°C, 40°C and 50°C is obtained with very good correlation factor as shown in Figure 3.9.

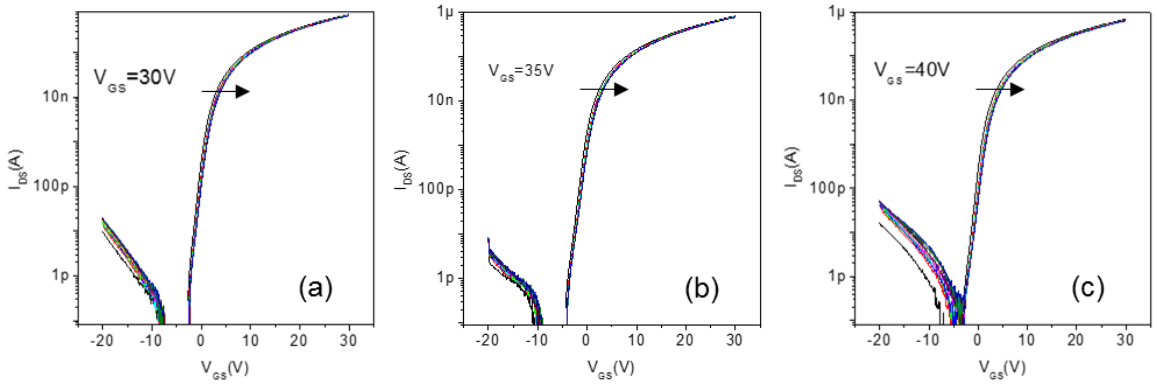

Figure 3.7: Transfer characteristics during gate bias stress at 25°C and stress biases (a) +30V, (c) +35V and (d) +40V.

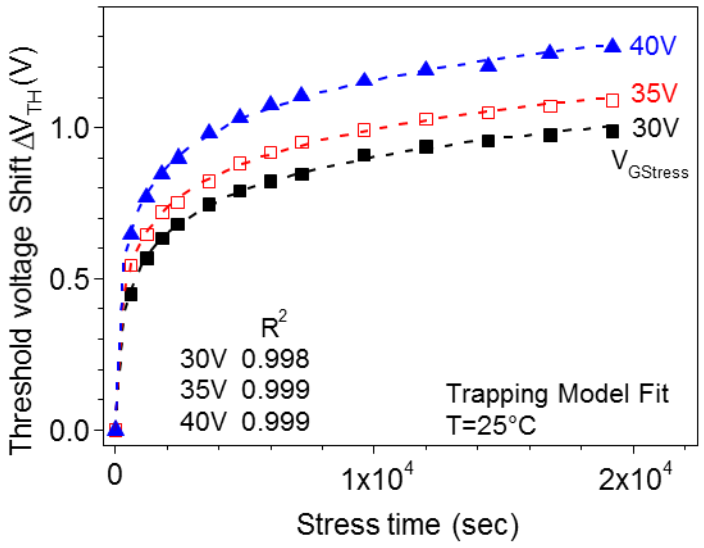

Figure 3.8: Threshold voltage shift during 30V, 40V, and 50V stress gate biases made at 25°C. The dashed curves are the fit with carrier trapping equation 3.3. The correlation factor R^2 of the fit is also given.

At constant stress time, the threshold voltage shift increases with the stress temperature (Figure 3. 19). Plotting shift as a function of the reverse temperature, we found that it is thermally activated with activation energy of 0.12 eV (Figure 3.10). Thermal activation of the threshold voltage shift means that the trapping of electrons inside silicon nitride is

followed by conduction inside the insulator [11]. The temperature behavior of the shift is mainly dominated by the charge conduction via hopping inside the insulator.

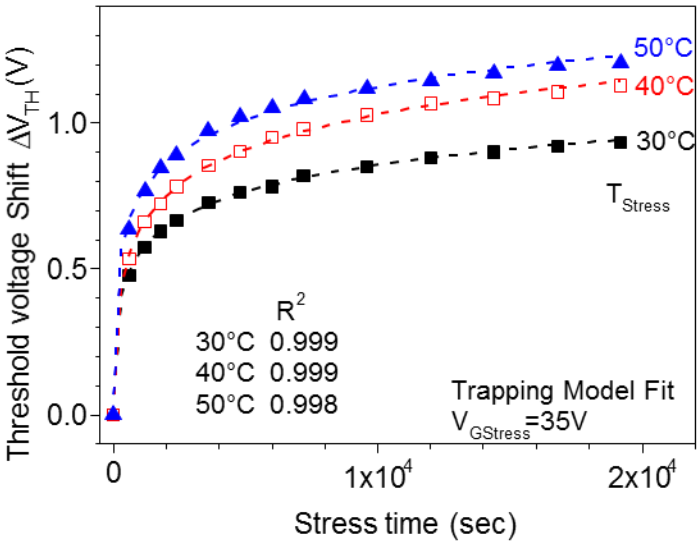

Figure 3.9: Threshold voltage shift during 35V stress gate bias made at 30°C, 40°C and 50°C. The dashed curves are the fit with carrier trapping equation 3.3. The correlation factor R^2 of the fit is also given.

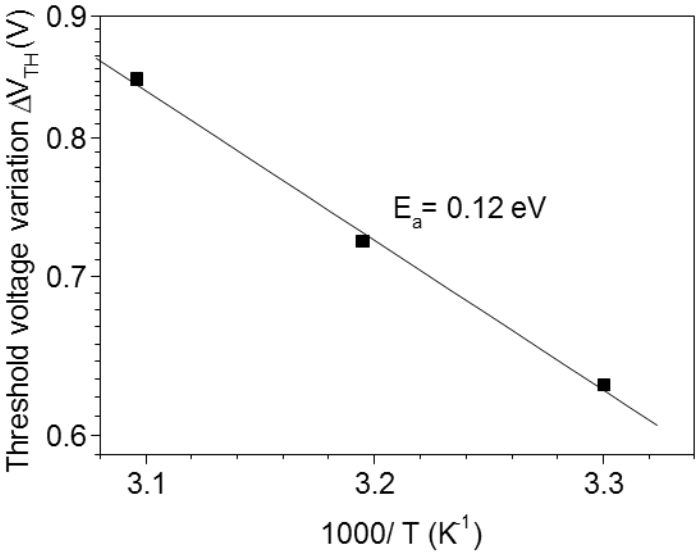

Figure 3.10: Thermal activation of the threshold voltage variation after 5.5 hours gate bias stress.

2.2.3 Conclusion on the electrical stability of microcrystalline silicon TFTs using silicon nitride as gate insulator

All these experimental and fitting stress results lead to attribute the shift of the threshold voltage of the present microcrystalline silicon TFTs to carrier trapping inside the silicon nitride gate insulator. The shift is thermally activated that suggests a shift behavior dominated by charge conduction inside silicon nitride. This conclusion is not surprising. Indeed firstly, microcrystalline silicon used here is very well crystallized as shown from the high crystalline fraction, 73%, deduced from Raman measurements. High crystalline fraction means low influence of the disordered regions and then high stability of the film. The second argument favoring the trapping model is the quality of silicon nitride deposited at low temperature 150°C. It is not surprising that this low temperature deposited film contains much more defects than usual silicon nitride deposited at 350°C favoring a hopping conduction inside the material.

However as the final purpose of the present work are to fabrication these microcrystalline TFTs on flexible low temperature plastic substrate, we have to continue to deposit silicon nitride at such low temperature. Moreover, even when using this low temperature deposited silicon nitride, the shift of the threshold voltage under extreme stress (high stress temperature 50°C and high stress bias $V_{GSstres}$-V_{TH}=35V-12V=23V) is only 1.2V. This low shift confirms the good stability of present TFTs. Moreover, if we take the usual definition of the lifetime that is the time needed for the drain current in saturation to decrease by 50%, we find more than 1014 years of functioning to reach this limit!

3. Microcrystalline silicon TFTs on flexible substrates

After checking the performance and the electrical stability of microcrystalline silicon TFTs fabricated at low temperature, it is now the time to fabricate these TFTs on flexible substrate. The purpose here is to reach the maximum flexibility when using such inorganic material as microcrystalline silicon.

Indeed, other materials as organic ones which have ideal elastic properties and Young modulus in the range of 0.1 – 10 GPa [14], are considered as ultra-flexible materials. Thus, organic TFTs (OTFTs) are nowadays a major research axis and have been widely reported with high flexibility and extreme curvature radii R until 1 – 0.1 mm [15]–[18]. However these materials are far from commercial availability. A lot of reproducibility and stability problems are still a drawback in the commercial use of OTFTs. This is why coming back to inorganic materials can be interesting. Inorganic materials are known to be much more stable and reproducible.

From these inorganic materials, silicon is the favor material. Silicon on any substrate is still the most reliable material to build efficient commercially available large area electronics. Silicon is vastly available; it is the second available element in the earth. It has no problem for recycling. It contains only one chemical element so that its chemistry is simple. Its forbidden band-gap is compatible with the mean temperature in the earth. Since first Silicon transistor on 1954 (60 years ago), the death of silicon is announced periodically. It overcame many issues as the working frequency (>4 Ghz now) and the low temperature process on glass and on plastics.

It is usually used in its amorphous structure or after laser crystallization to produce the most widely used active matrix for displays. It can be deposited at low temperature producing CMOS electronics on plastic substrate.

In IETR Laboratory (thesis of S. Janfaoui [19]), microcrystalline silicon TFTs have been successfully fabricated on 125 μm thick PEN substrate. The electrical performance, such as mobility, threshold voltage, substreshold slope, and electrical stability, of TFTs on PEN is comparable with that on glass substrate. However, the flexibility of these TFTs is poor. The

TFTs are destroyed by mechanical bending with R = 10 mm. The dysfunction is explained by the mechanical failure in the silicon nitride gate insulator.

The purpose of the present work is to go down in curvature radius leading to highly resilient silicon electronics.

3.1 Fabrication of microcrystalline silicon TFTs on PEN substrate.

Reaching highly resilient µc-Si TFTs needs to change some steps in previous TFT's process (thesis of S. Janfaoui [19]), in order to reduce the strain induced in the TFT's structure when bending it. To describe these changes, it is important to give first the mechanical model leading to the calculation of the strain.

3.1.1 Strain calculation

Figure 3.11 shows the structure of previous TFTs.

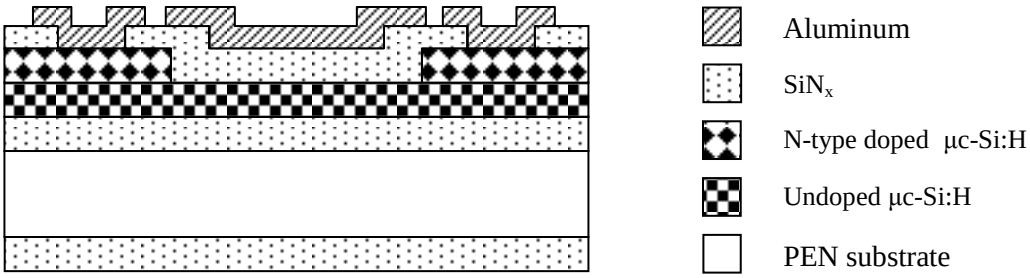

Figure 3.11: Structure of TFT fabricated on PEN substrate in the thesis of S. Janfaoui [19].

The 125 µm thick PEN substrate was embedded first between two 250 nm thick silicon nitride films. Then usual TFT process was made following the description given in chapter 2. On the center of the structure where the channel occurs, from mechanical point of view, the total structure is a stack of 6 layers: 250 nm thick silicon nitride, 125 µm thick PEN sheet, 250 nm thick silicon nitride, 100 nm thick undoped microcrystalline silicon, 300 nm thick silicon nitride and 250 nm thick Aluminum.

Calculation of the strain developed inside the structure when it is bent at some curvature radius is not easy. However, from mechanical point of view, the 6-films structure can be simplified taking into account the thickness and the Young modulus of the 6 films.

Considering the much higher Young modulus of silicon nitride (270 GPa) and the different thicknesses, the total bended structure is considered constituted by 3 layers only: bottom 250nm thick silicon nitride, 125 µm PEN substrate and a top 550 nm thick silicon nitride (Figure 3.12).

Figure 3.12: Mechanical model of the total TFT structure.

The strain developed in this simplified structure can be calculated using a model reported by the Princeton Group [20]. In this model, the strain ε in 3 films stack is given by equation (3.4).

$$\varepsilon = \left(\frac{1}{R} \pm \frac{1}{R_0}\right) \frac{d_S + d_{f1} + d_{f2}}{2} \frac{\chi(\eta_1^2 + \eta_2^2) + 2(\chi\eta_1 + \chi\eta_1\eta_2 + \eta_2 + 1)}{\chi(\eta_1 + \eta_2)^2 + (\eta_1 + \eta_2)(1+\chi) + 1} \qquad (3.4)$$

In this equation, d_S, d_{f1} and d_{f2} are the thicknesses of substrate, top and bottom silicon nitride films respectively. χ and η are defined by $\chi = \frac{Y_f}{Y_S}$; $\eta_1 = \frac{d_{f1}}{d_S}$; $\eta_2 = \frac{d_{f2}}{d_S}$ where Y_S and Y_f are the Young modulus of the substrate (6.45 GPa) and the silicon nitride film (270 GPa) respectively. R and R_0 are the present and the initial curvature radii.

Figure 3.13 presents the strain in the structure as a function of the curvature radius.

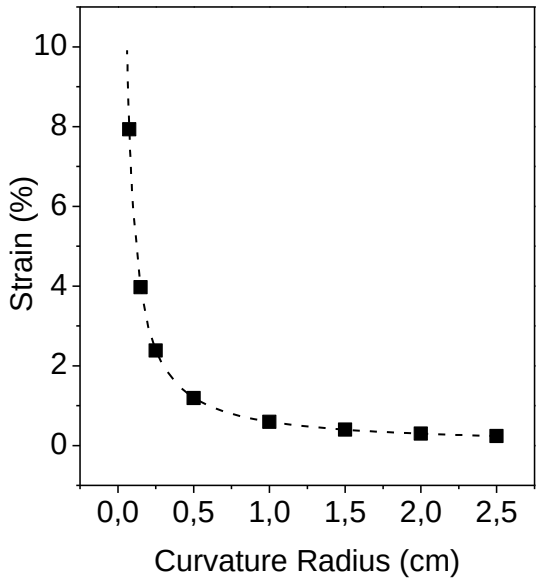

Figure 3.13: Strain developed in the structure as a function of the curvature radius.

As written before, this structure cannot hold a curvature radius lower than 10 mm. The purpose here is to simplify more the structure, reducing the thicknesses and removing some films.

First, the thickness 125µm of PEN substrate is too large, limiting the flexibility. Lastly, Dupont Teijin Films developed 25 µm thick of the same PEN substrate with one adhesive face (reference TEONEX Q831A). Indeed, 25 µm thick substrate cannot be handled freely as can be done with 125 µm thick sheet. 25 µm thick PEN sheet has to be stuck on rigid substrate during the TFT process. This sticking is an advantage as usual process on rigid substrate can be made. Only the stick has to do not change during the thermal and chemical treatments of the process.

The second possibility to reduce the strain is to remove the highest Young modulus films or to reduce their thickness. Silicon nitride has the highest Young modulus in the structure. We have 3 silicon nitride films in the previous structure. The behavior of PEN substrate, when submitted to the different chemical and thermal treatments, which are involved in the process, shows that it resists to these steps. The idea is then to remove both passivation silicon nitride films used in previous process. The other possibility is to reduce the thickness

of the silicon nitride gate insulator. Previously in IETR, 150 nm thick silicon nitride has been shown to act efficiently as gate insulator.

Following these observations, TFT process was simplified to keep TFTs more flexible. Before fabricating TFTs, the strain inside the new structure was calculated using the same model as previously.

The new structure is presented in Figure 3.14.

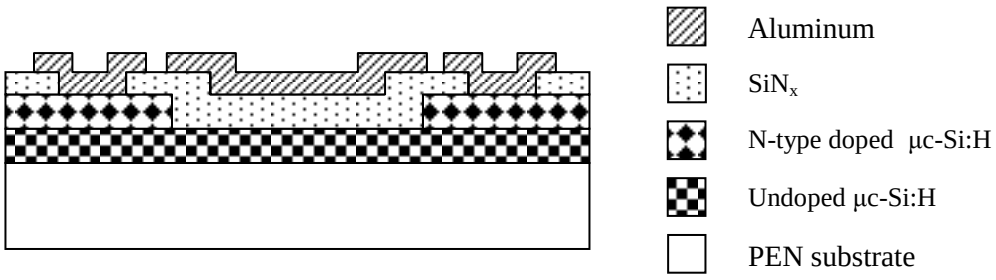

Figure 3.14: Structure of TFT fabricated on 25 µm thick PEN substrate.

From mechanical point of view, the total structure is a stack of 4 layers: 25 µm thick PEN sheet, 100 nm thick undoped microcrystalline silicon, 150 nm thick silicon nitride and 250 nm thick Aluminum. As previously, the structure can be simplified taking into account the thickness of each film and its Young modulus. The total bended structure can be considered constituted by 2 layers only: 25 µm PEN substrate and a top 150 nm thick silicon nitride (Figure 3.15).

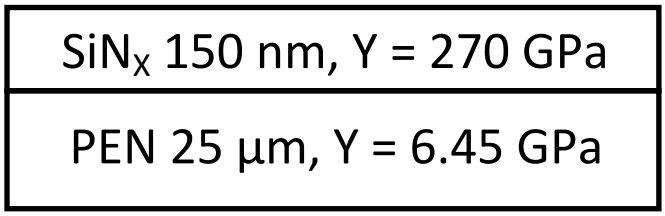

Figure 3.15: Mechanical model of TFT on 25µm PEN.

The strain developed in this simplified structure can be calculated using previous model reported by the Princeton Group [20]. For a stack of 2 layers, equation (3.4) can be simplified into equation (3.5).

$$\varepsilon = \left(\frac{1}{R} \pm \frac{1}{R_0}\right)\left(\frac{d_S + d_f}{2}\right)\frac{(1+2\chi\eta+\chi\eta^2)}{(1+\eta)(1+\chi\eta)} \qquad (3.5)$$

In this equation, d_S, d_f are the thicknesses of substrate and silicon nitride film respectively. χ and η are defined by $\chi = \frac{Y_f}{Y_S}$; $\eta = \frac{d_f}{d_S}$ where Y_S and Y_f are the Young modulus of the substrate (6.45 GPa) and the silicon nitride film (270 GPa) respectively. R and R_0 are the present and the initial curvature radii.

Figure 3.16 presents the strain in the structure as a function of the curvature radius. The strain in previous structure is also represented in this Figure. Obviously, the strain developed in the new structure is lower than the strain developed in previous structure for the same curvature radius.

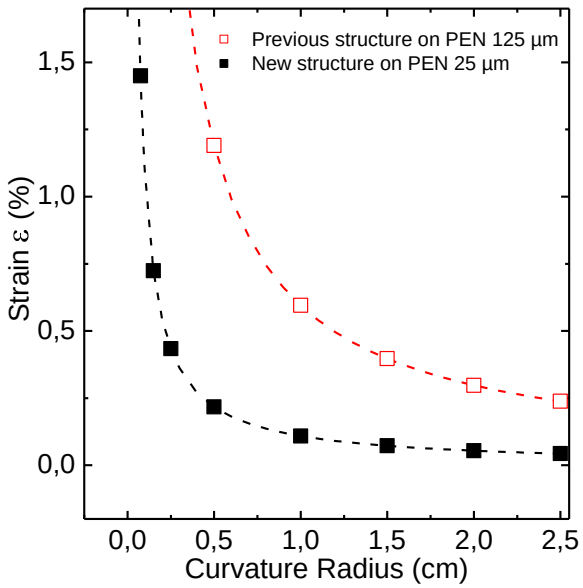

Figure 3.16: Strain developed in the new structure (black filled squares) and in previous structure (red open squares) as a function of the curvature radius.

Present calculation shows the possibility to bend TFTs at lower curvature radius by using the new structure. It is the time now to fabricate TFTs following this new structure and to check their mechanical behavior.

3.1.2 TFT's process

TFTs are fabricated directly on 25 µm thick PEN (Polyethylene Naphthalate) using same steps than that on glass substrate. The only difference is that here thinner (150 nm thick) silicon nitride is used as gate insulator. The difficulty to handle and process on very thin plastic substrates is well-known: 125 µm thick plastics can be handled freely but thinner ones (< 50 µm) require to be spin-coated (e.g. Polyimide) or reported on a rigid carrier. Here, the PEN sheet with an adhesive back face has been stuck on a glass carrier wafer before processing and released only at the end of the process.

Before starting the process, PEN sheet attached on glass is cleaned by acetone and alcohol for 10 minutes respectively. As presented in Chapter 2, the process involves:

- deposition of undoped and doped µc-Si layers, here 100 nm and 70 nm thick respectively,
- 2 photolithography steps to define the TFT geometry,
- a RCA cleaning process to remove the organic and metallic impurities in the undoped silicon layer,
- deposition of 150 nm thick silicon nitride layer, which will be the gate insulator of TFT, and then 2 hours annealing at 180°C under N_2 gas
- photolithography step to open windows onto source and drain
- deposition of aluminum and then patterning to from the drain, source and gate electrodes.
- Final 2 hours annealing of the TFT at 180°C under N_2.

After the process, the PEN sheet is removed from the holding glass and TFTs characterized.

3.1.3 TFT's electrical characterization

Figure 3.17 shows the transfer characteristics of the microcrystalline silicon TFT on 25 µm thick PEN with a W/L ratio of 40/20 µm. Even if the thickness of gate insulator is reduced to 150 nm for this new structure, the gate leakage current is only 4 pA at V_{GS} = 30V, indicating a good dielectric property of this gate insulator. The electrical parameters have been summarized in Table 3.2. We present here also the electrical parameters of microcrystalline silicon TFT fabricated on 125 µm thick PEN substrate using previous structure [19]. The electrical parameters, such as mobility and subthreshold slope, of both TFTs on 25 µm thick PEN using new structure and on 125 µm thick PEN using previous structure, are similar. Even if the thickness of silicon nitride gate insulator and device structure are different for both TFTs, the consistency of these electrical parameters indicates a good reproducibility of our microcrystalline silicon TFT process on PEN substrate.

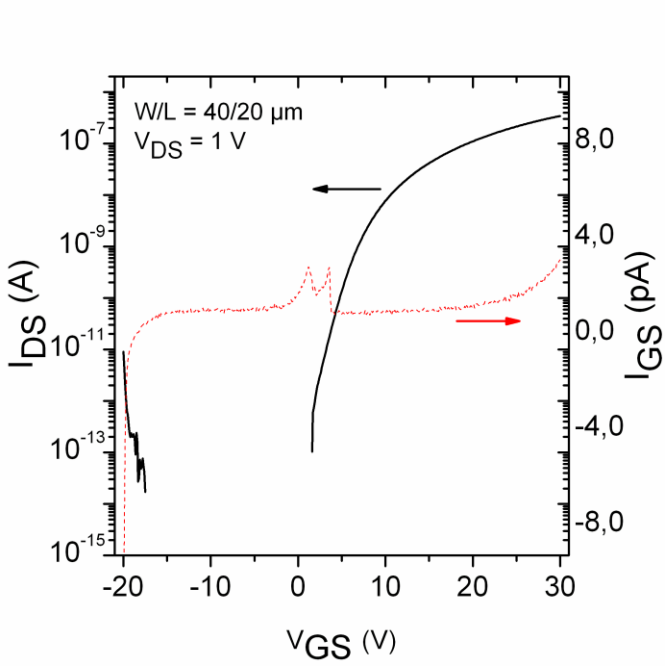

Figure 3.17: Transfer characteristic of microcrystalline TFT on 25 µm thick PEN. Leakage gate current I_{GS} is also given in the figure.

	Mobility (cm^2/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)
New structure on 25µm PEN	0.45	1.3	17
Previous structure on 125 µm PEN	0.46	1.35	12

Table 3.2: Electrical parameters of microcrystalline TFT fabricated on 25µm thick PEN (new structure) in comparison with previous structure fabricated on 125 µm thick PEN [19].

As the electrical stability is an important factor contributing in the validation of the process, gate bias stress has been applied on the present microcrystalline silicon TFTs fabricated on 25 µm thick PEN substrate. TFTs were submitted to +20V stress gate voltage during 6 hours at ambient temperature. Figure 3.18 shows the transfer characteristics plotted at different stress times. The behavior is similar to what we foud previously when studying the electrical stability of our usual µc-Si TFTs (paragraph 2.2 of Chapter 3). Positive shift of the characteristics is observed. The characteristics are parallel implying constant subthreshold slope and then probably dominant effect of carrier trapping inside the insulator.

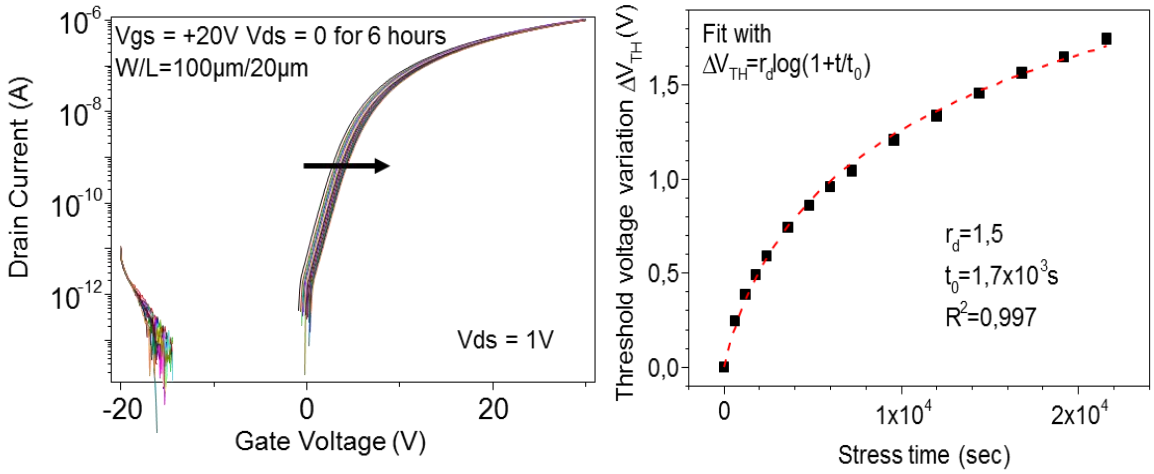

Figure 3.18: Transfer characteristics during 6 hours and +20V stress gate voltage and the resulting shift of the threshold voltage. This shift is fitted by carrier trapping equation.

The shift of the threshold voltage is presented in the same figure 3.18. It is well fitted with the carrier trapping equation 3.2 leading to the same conclusion as previously. However, we note slightly larger shift 1.6V than previously (<1V) where TFTs were fabricated on glass.

3.2 Mechanical behavior of microcrystalline silicon TFTs on PEN substrate.

TFTs fabricated on 25 µm thick PEN presents more or less similar electrical parameters and electrical stability than same TFTs fabricated on glass. The next step is to check these performances under mechanical (tensile and compressive stress) bending and particularly the lowest curvature radius they can hold.

3.2.1 Mechanical stress tools

The mechanical behavior to evaluate the flexibility is studied by bending TFTs to tensile and compressive stress with different curvature radii using static homemade tools (Figure 3.19). We focus here only on the longitudinal strain, which means a channel (i.e. the current flow) oriented in the same direction of the bending. Electrical characteristics are measured during and after bending tests.

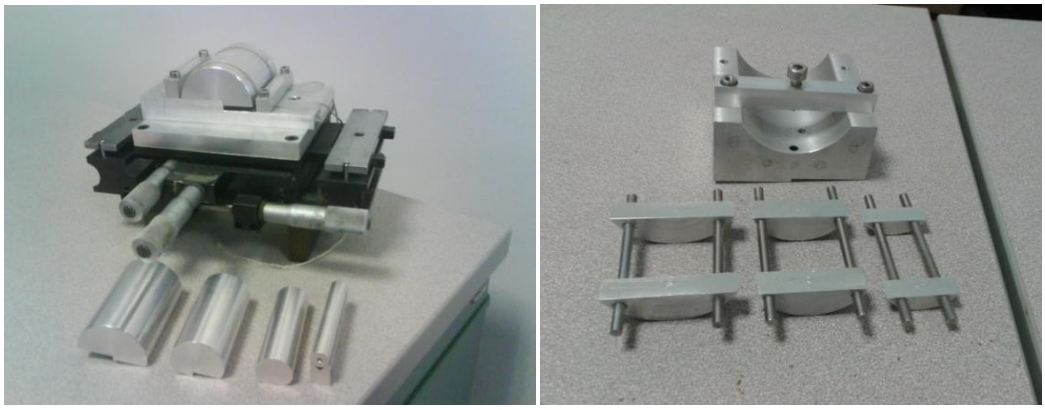

Figure 3.19: Homemade tools for tensile and compressive strain. TFTs are bended outward and inward in the same direction of the channel.

The procedure of the TFT's characterization under bending consists in sticking the substrate with TFTs on half cylinder tools with different radii. The channel of TFTs is oriented in the direction of the bending. Then TFTs are characterized under probes as usual. Figure 3.20 shows the PEN substrate-TFT structure stack mounted on half cylinder tool in the case of tensile stress.

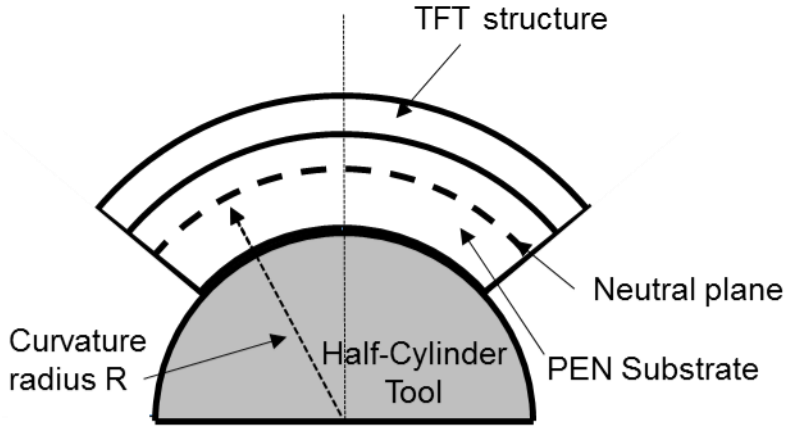

Figure 3.20: PEN substrate with TFTs mounted on half-cylinder tool. In this case TFT is submitted to tensile stress in the direction of its channel due to the curvature radius R.

3.2.2 TFTs behavior during bending tests

TFTs are bent for different radii R in tension (ranging from 25 mm to 5 mm). Figure 3.21 shows an example of transfer characteristics of TFTs in flat position and bent at these different tensile curvature radii.

The first important result is that present TFTs can hold 5 mm curvature radius without breaking. 5 mm is lower than the minimum curvature radius (10 mm) that can hold TFTs fabricated in previous structure. This experimental result confirms the calculation of the strain made before in paragraph 1.1 of Chapter 4. This calculation has shown that the strain developed is lower in the new structure for the same curvature radius, leading to functioning TFTs at lower curvature radius.

The on-current increases when the curvature radius decreases that means when the tensile stress increases. This figure 3.21 shows also the relative variation of the on-current with the strain. The strain is calculated using the model described before.

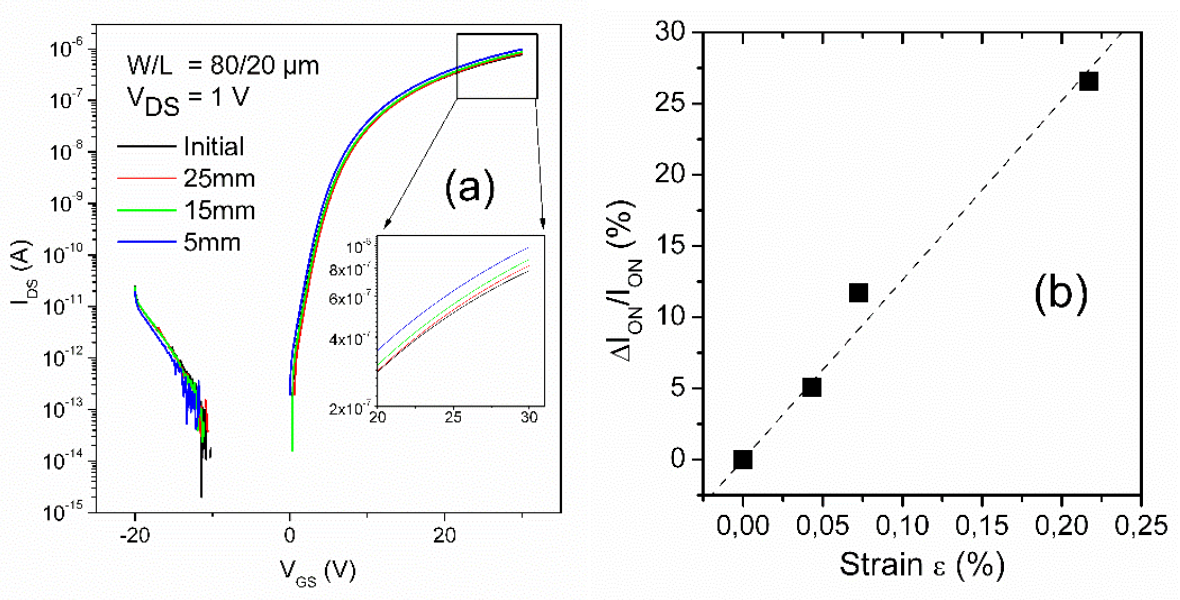

Figure 3.21: Transfer characteristics of TFTs bent under different tensile curvature radii and the relative increase of the on-current as a function of the developed tensile strain

The increase of on-current with tensile strain for N-type TFTs is known. It is common in silicon TFTs whatever the amorphous [21], micro(poly)-crystalline [22,23] or single crystalline structure [24]. The effect of tensile stress on µc-Si TFTs deposited on PEN was extensively studied in the thesis of S. Janfaoui [19]. The increase was attributed to a change in the energy bands due to the uniaxial stress, decreasing mainly the conductivity effective mass.

On-current increases nearly linearly with the strain with a slope of 93%. The on-current increases by 28% when TFT is bent until 5 mm curvature radius. The variation is too important to conclude that present TFTs cannot be used in functioning electronics submitted to dynamic variation of the mechanical stress. However presents TFTs can be operational under high static mechanical deformation.

3.2.3 TFTs critical radii under tension and compression

The homemade tools to study the TFT's characteristics under bending are limited to R = 5 mm under tensile stress. It is not possible to use probes when measuring TFTs characteristics at lower curvature radius.

However it is important to check the behavior of these TFTs under lower curvature radii, until their breaking. The solution to make this study is to bend mechanically the TFTs at very low curvature radius and to check their functioning when coming back in flat position. If any breaking occurred under mechanical deformation, TFTs cannot work after this breaking.

TFTs are then bent tensely and compressively until R = 2.5, 1.5 and 0.75 mm using steel cylinders and measured while re-flatten after every bending. Figure 3.22 shows the transfer characteristics together with the leakage gate current I_{GS} behavior of TFTs in flat position after each bending. Note that the sample was previously cut in two so that transistors from the same process were subjected to only tensile or compressive stress.

Remarkably, the transfer characteristics are exactly similar after either tensile or compressive bending until R = 1.5 mm. The gate current leakage increases a bit for R = 1.5 mm but stays very low (maximum of 50 pA for V_{GS} = 30 V). For lower radius, i.e. 0.75 mm, an obvious degradation of I_{ON} and I_{GS} is observed but TFTs remains functional in both tension and compression.

However, a slight difference can be observed between tension and compression. The degradation is more important under tension, as shown from the behavior of I_{GS} and can be impacted to a mechanical degradation of the films, such as cracks. Under compression it may be caused by a delamination of the films from the substrate. This phenomenon has indeed been suggested in [25].

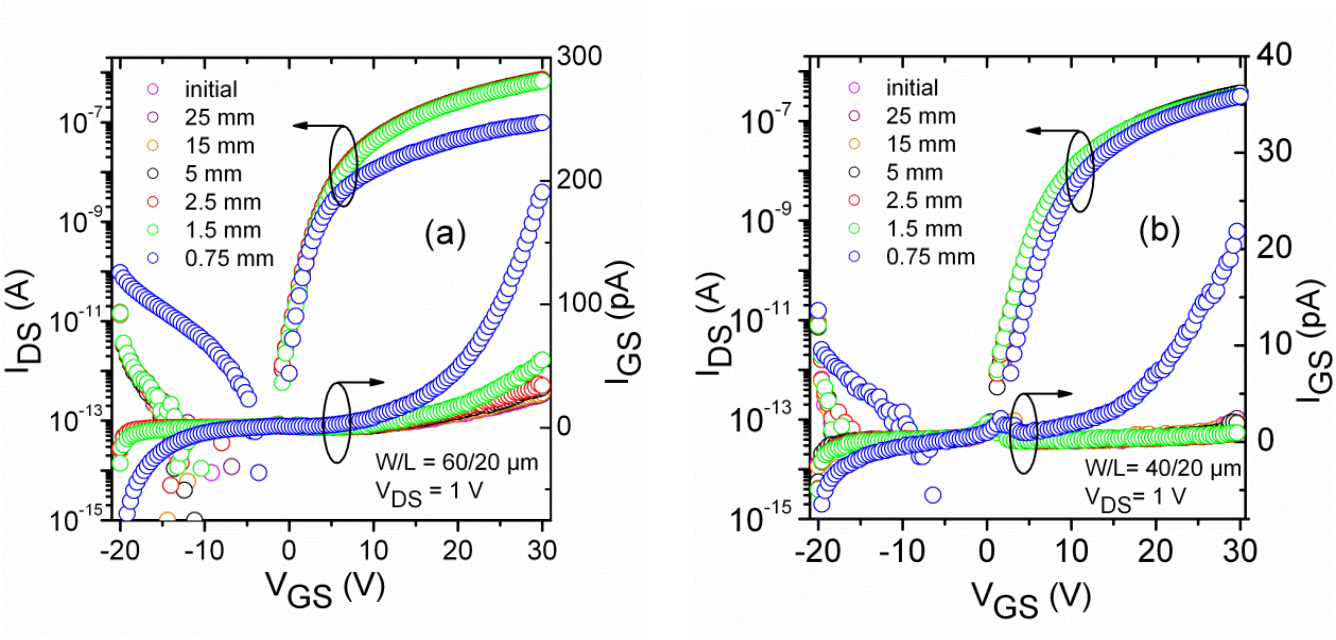

Figure 3.22: Transfer characteristics and gate current measured in flat position after bending for different curvature radii: a) tensile stress and b) compressive stress

Present results highlight the possibility to bend microcrystalline silicon TFTs in tension or compression without changing their electrical properties until R = 1.5 mm at least (since no tests have been performed between 1.5 and 0.75 mm). 1.5 mm radius means practically the possibility to bend TFT in 2 without losing their performance in flat position. This value is comparable with some organic TFTs, even all the layers of our TFTs are inorganic.

3.2.4 TFTs reliability under multiple bending

Previous result on the minimum curvature radius that can hold present TFTs is an important one. However, it may be useful to test this ability to hold such curvature radius by making multiple tensile bending tests, simulating a fatigue test. Figure 3.23 a) shows the transfer characteristics of 3 differently sized TFTs (W/L = 60/20, 40/20, 20/20 µm) measured in flat position, initially and after various bending cycles: 20, 50 and 100 times for R = 5 mm. Figure 3.23 b) focus on the transfer characteristic of the TFT with W/L = 40/20 µm in flat position also initially and after various bending cycles: 20, 50, 100 and 200 times for R = 2.5 mm.

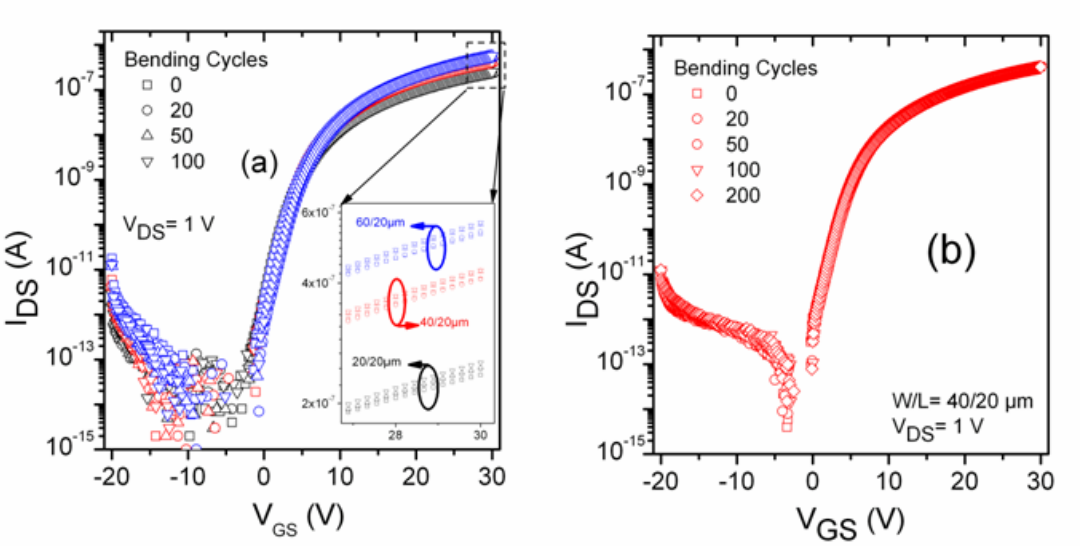

Figure 3.23: Transfer characteristics of TFTs measured flatten before and after tensile bending stress applied: a) 20, 50 and 100 times for 3 different W/L ratios at R = 5 mm, b) 20, 50, 100 and 200 times for W/L = 40/20 µm at R = 2.5 mm.

One can observe that transfer characteristics stay nearly unchanged after 100 cycles at R = 5 mm and even 200 cycles at R = 2.5 mm. An I_{ON} analysis of the 40/20 µm TFT at V_{GS} = 30V shows a nearly constant value with a relative variation of 1 % even after 200 cycles at R = 2.5 mm, as shown in Figure 3.24.

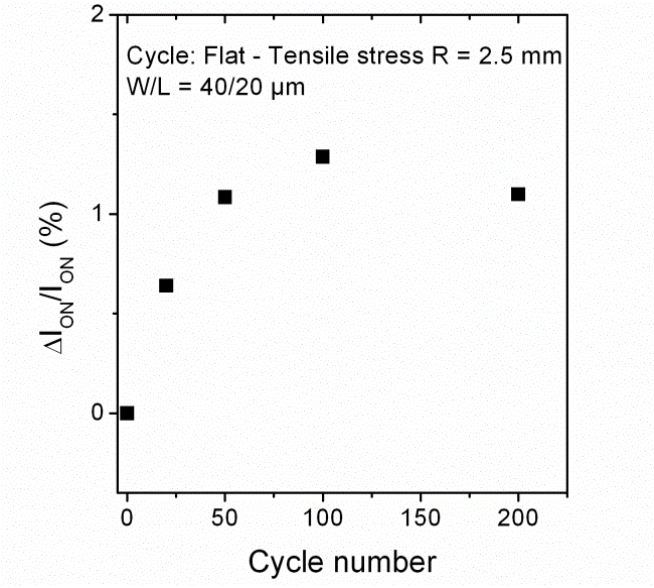

Figure 3.24: Relative variation of the on-current at V_{GS}=30 V of the 40/20µm TFT when submitted to Flat – Tensile cycles at R=2.5mm until 200 cycles.

3.2.5 Discussion of the high flexibility of microcrystalline silicon TFT on PEN substrate

These previous results demonstrate the possibility to bend TFTs made of inorganic materials (microcrystalline silicon, silicon nitride and aluminum) until R = 1.5 mm without losing electrical performances and support R = 0.75 mm but with lower electrical performances. It seems that the main effect limiting the radius is a high increase of I_{GS} at high V_{GS} as shown in Figure 3.22. The origin of I_{GS} degradation can be the mechanical behavior of the silicon nitride layer due to its highest Young modulus.

As expected from the discussion on the limiting factors in the mechanical behavior of the TFT structure developed before in IETR [19], and from the calculation of the strain developed in previous and present TFT structures, present TFT structure holds lower curvature radius than the previous one.

To understand more the origin of the mechanical limit, it may useful to reproduce here figure 3.25 showing the strain developed in both structures by curvature radius. This figure is renumbered 3.25 here.

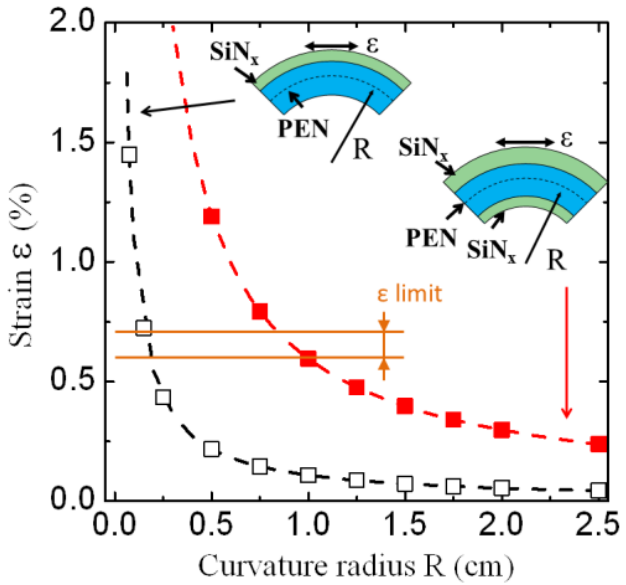

Figure 3.25: Strain developed in the new structure (black open squares) and in previous structure (red filled squares) as a function of the curvature radius.

We observe well that for an equal curvature radius, the new TFT structure is much less strained than the previous one. The previous structure holds 10 mm minimum curvature radius. At this curvature radius, the value of the strain developed inside the structure is about 0.6-0.7%. The 1.5 mm minimum curvature radius held by the new structure corresponds to similar strain of 0.6-0.7%. This means that both structures are limited by the same origin defined by the maximum strain (0.6-0.7%) than can hold silicon TFT using microcrystalline silicon as active layer and silicon nitride as gate insulator.

This value of strain limit is approximately the same reported by the Princeton Group [20] for amorphous silicon TFTs on polyimide using silicon nitride as gate insulator. This means that microcrystalline silicon and amorphous silicon TFTs are limited by the same strain value. The other possibility is that silicon can hold higher strain but silicon nitride cannot. Indeed, silicon nitride was used in both amorphous and microcrystalline silicon TFTs. Moreover, its Young modulus, 270 GPa, is higher than its value for silicon 160 GPa.

The conclusion is that the main limitation of silicon TFTs comes from the mechanical behavior of silicon nitride material.

4. Conclusion

Following the long way of IETR towards not only flexible but also reliable electronics, the results given in chapter constitute an important milestone. We demonstrated the possibility to build highly flexible electronics than can be bent many times nearly in two and that works after that.

This electronics is based on silicon that is the most used semiconductor and that is known for its reliability and reproducibility.

The reliability of microcrystalline silicon TFTs made at low temperature that is compatible with the use of transparent plastic substrate, as PEN, was studied and demonstrated. The study attributed the slight change of the TFT's parameters during functioning to carrier trapping in silicon nitride gate insulator.

These reliable TFTs present, however, low field effect mobility, slightly lower than 1 $cm^2/V.s$. Increasing this mobility while maintaining the high reliability is the new challenge we will try to reach in next chapter.

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Chapter 4: Increasing the mobility of microcrystalline silicon TFT

1. Introduction

As presented in the issues addressed in the present work, the other problem concerns the field effect mobility value and its link with the electrical stability. Indeed, when using silicon dioxide deposited by RF sputtering as gate insulator, TFTs present thigh mobility (from 20 to 150 $cm^2/V.s$ for electrons) but very poor electrical stability [1]. On the contrary, the mobility is very weak (on the order of 1 $cm^2/V.s$) and the electrical stability very excellent when using silicon nitride deposited by PECVD at 150°C as gate insulator. Silicon dioxide deposited on microcrystalline silicon produces high interface quality leading to high mobility but poor stability due to oxygen penetration in silicon during the Sputtering deposition [2].

The problem of simultaneous both high mobility and high stability is addressed here through the use of different gate insulators leading to channel - gate insulator interface change.

2. Microcrystalline silicon TFTs using different gate insulators

To check the only effect of changing the gate insulator, the process to fabricate all TFTs is keep exactly the same. Only the gate insulator is changed. The process was already described in chapter 2. After deposition of 100 nm thick un-doped and 70 nm thick doped µc-Si films always in the same conditions, doped µc-Si film is plasma etched to define source and drain regions. Then gate insulator is deposited and plasma etched to open the source and drain vias. After that, aluminum film is deposited and wet etched to define the source, gate and drain contacts.

2.1 RF sputtered silicon dioxide as gate insulator

Silicon dioxide was used as gate insulator in the first experiments due to its known properties and particularly to the electrical quality of its interface with silicon.

2.1.1 Reviews of previous TFTs using silicon oxide deposited at ambient temperature (without heating the substrate) by RF sputtering

K. Kandoussi [1] and K. Belarbi [2] used silicon dioxide deposited by RF sputtering without heating the substrate during their PhD works. The deposition conditions and the post-annealing process were optimized through the performance of Metal-Oxyde-Silicon wafer MOS capacitance. Table 4.1 gives the deposition conditions. The post-annealing was made under 20 sccm H_2 and 10 sccm O_2.

Power (W)	Pressure (mbar)	D_{A-K} (cm)	Mixture Ar-O_2
200	$5\ 10^{-3}$	8	30%(O_2)

Table 4.1: Deposition conditions of sputtering silicon oxide

An example [2] of transfer characteristics of TFTs when using this silicon dioxide as gate insulator is given in Figure 4.1. The electrical parameters calculated from this curve are presented in Table 4.2.

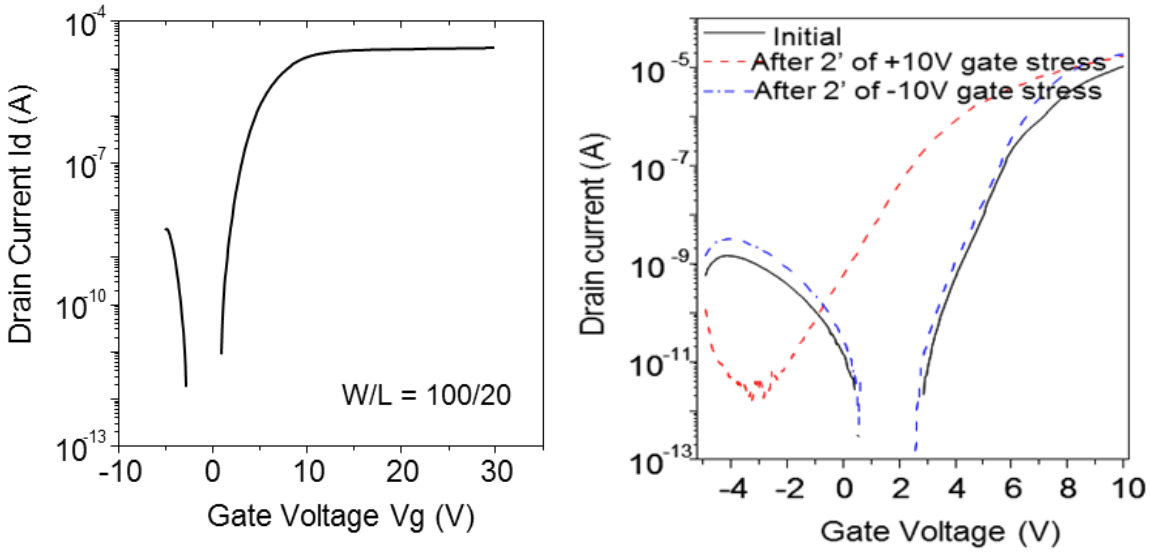

Figure 4.1: Transfer characteristics of microcrystalline silicon TFTs when using silicon dioxide deposited without heating the substrate and behavior of such characteristics under low stress gate voltage during shift time (2 minutes).

Mobility ($cm^2/V.s$)	Subthreshold slope (V/Dec)	Threshold voltage (V)
40	0.5	3.2

Table 4.2: Electrical parameters of N-type TFT extracted for transfer characteristic presented in Figure 4.1.

Interesting parameters were found with high mobility, low subthreshold slope and low threshold voltage. However, these TFTs were fully instable as shown in Figure 4.1 where the threshold voltage shifts by 5V under positive stress after 2 minutes only.

This non-stability was explained by the behavior of oxygen present in the first nanometers of the active layer and coming from the bombardment of silicon by oxygen during the sputtering.

2.1.2 Silicon dioxide deposited at fixed temperature RF sputtering

Previous silicon dioxide was deposited without heating the substrate in a RF sputtering reactor where it is not possible to make this heating. Heating the substrate is known to help in better quality of the deposited film. Then new silicon dioxide was deposited during the present thesis work in another reactor at 150°C. This temperature was chosen in order to be compatible with the use of PEN substrate.

2.1.2.1 MOS capacitance using SiO_2 deposited at 150°C

Before fabricating TFTs, the quality of SiO_2 film and its interface with silicon were checked through the characteristics of Aluminum-SiO_2-N type silicon wafer MOS structure. Figure 4.2 presents High frequency (1 MHz) and Quasi-static C-V characteristics of this structure, after post-annealing at 180°C and 250°C during 1 hour or 4 hours. SiO_2 films were deposited with a power of 75W and a gas mixture of 40 sccm Ar and 20 sccm O_2.

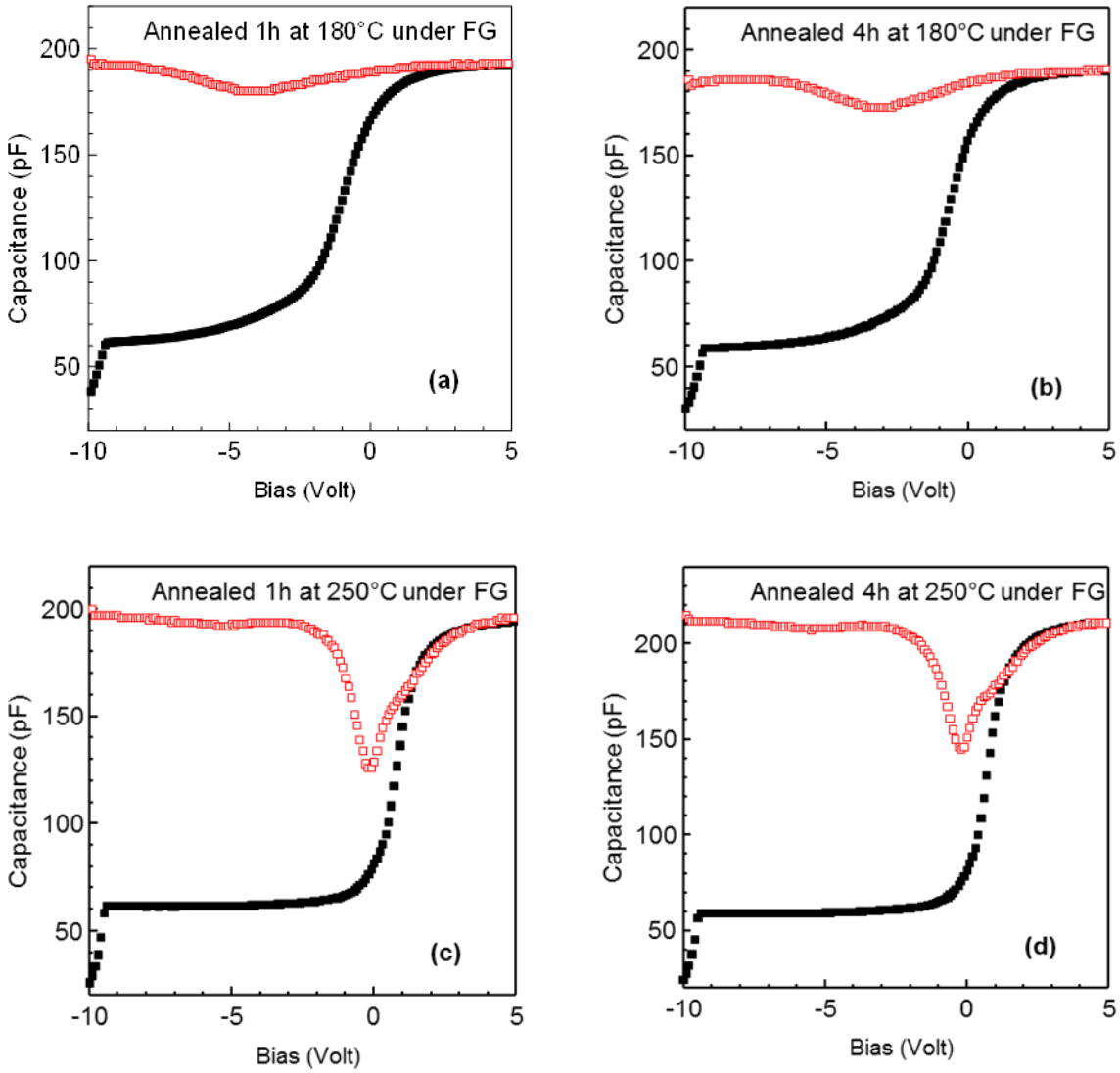

Figure 4.2: High frequency 1 MHz (black full square curves) and Quasi-static (red open square curves) C-V characteristics of Al-SiO_2-N type Si wafer MOS structures after 1h and 4h annealing at 180°C or 250°C.

To discuss on this figure 3.2, we need to remember that a modulation of the quasi-static characteristic means the surface voltage is not pinned by interface defects due mainly to the low content of such defects. Deeper is the modulation, lower is the defect content. After annealing at 180°C, weak modulation can be observed. The modulation is much deeper after the 250°C annealing. This means the interface is greatly improved after 250°C annealing.

The other observation is the near flat quasi-static (QS) curves in the accumulation and deep inversion regimes after 250°C annealing. This means very weak leakage current. After 180°C annealing, the quasi-static (QS) characteristic is also near flat but we can observe a very slight slope meaning higher leakage current after 180°C annealing than after 250°C.

After 250°C annealing, a shoulder appears in the QS characteristic in the weak inversion regime. This means an energetically localized interface defect appears. It slows down the decrease of the capacitance from accumulation to weak inversion regime. The shoulder is more important after 250°C annealing than after 180°C.

The improvement of the characteristics after these annealing can be quantified by the slope of the high frequency capacitance in the weak inversion regime and the value of the flat-band voltage FB. Table 3.3 summarizes these quantities after the annealing.

Annealing temperature (°C)	Annealing time (hour)	HF C-V slope (pF/V)	Flat-band voltage (V)
180	1	45	-4
	4	52	-3
250	1	92	-0.1
	4	114	-0.3

Table 4.3: Slope of the high frequency capacitance in the weak inversion regime and Flat- band voltage after annealing at 180°C and 250°C during 1h and 4h.

The C-V slope improves after each annealing. However and as expected, the temperature effect is higher than the time effect. The FB voltage shifts to lower negative voltage arriving at nearly 0 after 250°C annealing.

These CV experiments led us to determine what can be the best annealing conditions giving the highest quality SiO_2 film. It seems here that 250°C annealing during 1h are the optimum conditions in the low temperature domain of the TFT process. Even if 250°C is too high when using PEN substrate, it was chosen here only to check the improvement of the

TFT characteristic in terms of mobility value and stability. Moreover, 250°C is not too high temperature so that polyimide substrate can be used at this temperature.

2.1.2.2 TFTs using SiO_2 deposited at 150°C and then annealed at 250°C during 1h under forming gas.

As described before, present TFTs uses 100 nm thick undoped µc-Si film as active layer, 70 nm thick N-type doped µc-Si film as source and drain regions. After the µc-Si processing steps, 150 nm thick Silicon dioxide is deposited at 150°C and then annealed at 250°C during 1 hour under forming gas.

Transfer characteristics of these TFTs are presented in Figure 3.3. The channel width W and the channel length L are 100 µm and 20 µm respectively. Leakage gate current is also given in the same figure.

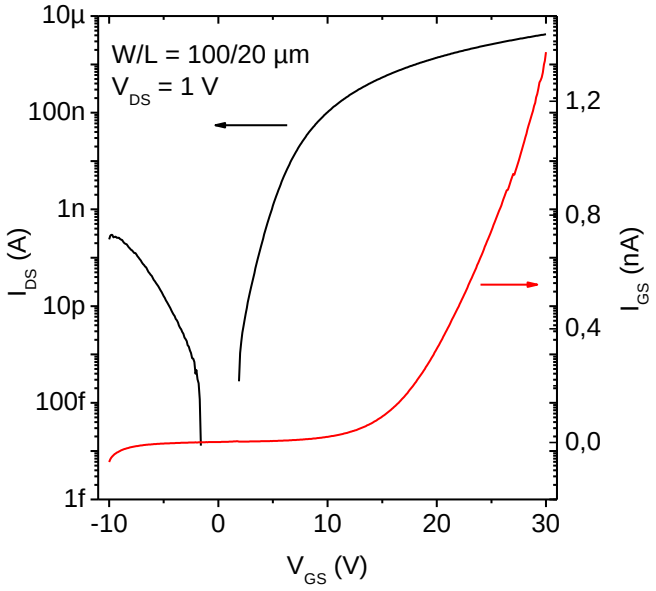

Figure 4.3: Transfer characteristic of microcrystalline silicon TFT (100/20 µm) with 150 nm thick sputtered silicon dioxide deposited at 150°C as gate insulator

Very low off-current at low gate voltage is shown. However, it increases nearly exponentially when the reverse gate voltage increases. The leakage gate current is very low

until a gate voltage value of +15V, from which it increases a lot. At a gate voltage of 30V, it reaches 1.2 nA.

The electrical parameters of this type of TFT are summarized in the Table 4.4.

Mobility (cm^2/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)	I_{ON}/I_{OFF}
2.5	1.25	17.2	$>10^7$

Table 4.4: Electrical parameters of TFT presented in Figure 4.3.

The off-current behavior is similar to what it was found when using silicon dioxide deposited without heating the substrate. The mobility value is lower than its previous value. However, it can be acceptable if high TFT electrical stability is obtained.

The TFT electrical stability was investigated by applying positive gate bias stress $V_{GSstress}$ = + 20V for 6 hours at room temperature. A negative shift of the threshold voltage and a nearly constant subthreshold slope are observed. The threshold voltage shift can be due to displacement of positive charge inside the insulator towards the insulator-channel interface. However, the most important observation is the weak value of the shift, 1.45 V, particularly if this behavior is compared to that of previous TFTs when using silicon dioxide deposited without heating the substrate during the deposition.

Depositing silicon dioxide in the present conditions can be one way to improve the stability of microcrystalline silicon TFTs. However, we have to check if an annealing at 180°C that is compatible with the use of PEN substrate can be enough to insure some stability.

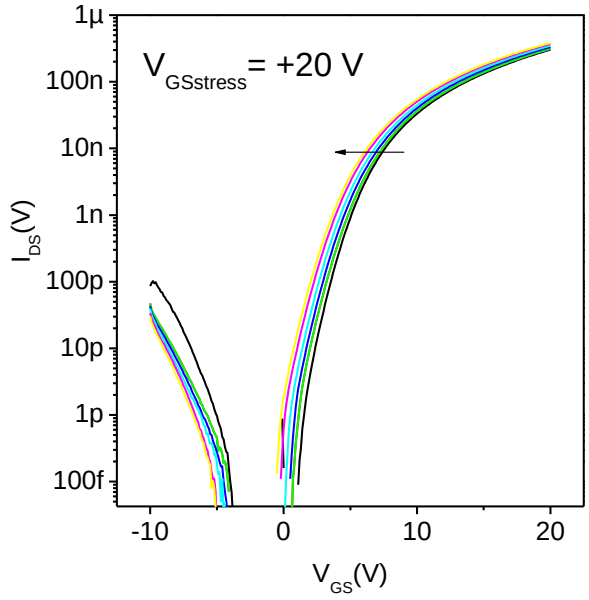

Figure 4.4 Microcrystalline silicon TFTs using sputtering silicon oxide as gate insulator after prolonged gate bias stress, $V_{GSstress}$= +20V, stress for 6 hours.

2.2 TFTs using ECR-CVD deposited SiO2 as gate insulator

Depositing SiO_2 by chemical vapor deposition techniques can present some advantages in comparison of sputtering techniques. The deposition is more "soft" leading to only slight bombardment of silicon by oxygen. TFTs can be more stable.

To check only the possibility to use such deposition techniques, some microcrystalline silicon TFTs were processed first in IETR, then SiO_2 films were deposited in the Institute for Microelectronics and Microsystems – CNR – Roma (Italy) using ECR-CVD reactor and finally TFT's process was finished in IETR.

SiO_2 deposited by ECR-CVD in IMM was previously optimized by the IMM team as gate insulator of polycrystalline silicon TFTs [3]. The best gate insulator was obtained after a post-annealing at 450°C.

In the present work, SiO_2 films were deposited as usual in IMM without heating the substrate. As usual also, the deposition was followed by a post annealing in IETR. However,

the annealing temperature was limited to 180°C following the goal of this work. Then final annealing was made at 180°C under forming gas.

Figure 4.5 shows the transfer characteristic of microcrystalline silicon TFT using 100 nm thick silicon oxide deposited by ECR-CVD as gate insulator. Table 4.5 concludes the electrical parameters of the TFT. The mobility value, 0.85 cm^2/Vs is, much weaker than that of previously fabricated TFT using sputtering silicon oxide as gate insulator. The leakage gate current increases from 15V gate voltage. However, it stays very low and its value at 25V is only 40 pA, much lower than its value with previous sputtered silicon dioxide.

Even if the mobility value is low, it has been useful to check the electrical stability of these transistors.

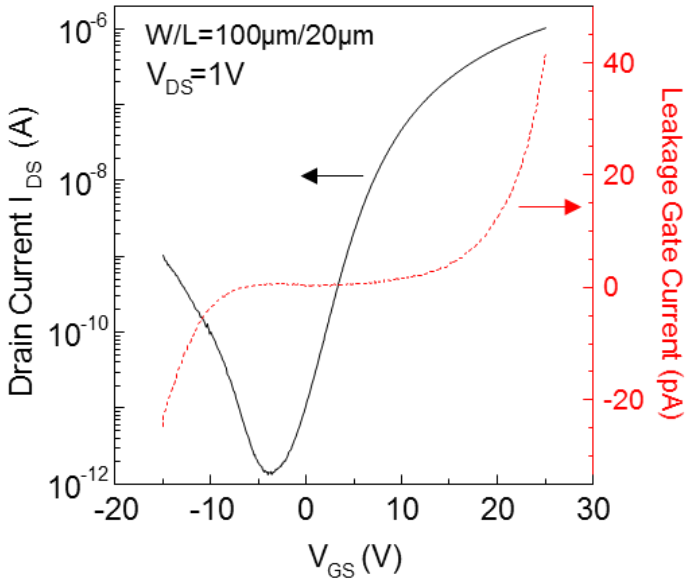

Figure 4.5: Transfer characteristic of microcrystalline silicon TFT (100/20 µm) with ECR-CVD deposited silicon oxide as gate insulator

Mobility (cm^2/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)	I_{ON}/I_{OFF}
0.85	2	14.5	10^7

Table 4.5: Electrical parameters of TFT using ECR-CVD deposited silicon oxide as gate insulator

Figure 4.6 shows the behavior of the transfer characteristics of such TFT during +20V gate bias stress. The shift is nearly parallel indicating constant subthreshold slope. This means that the shift is more probably due to charge trapping and/or displacement of charges inside the gate insulator. The shift is important, a little bit less than 4V after 40 minutes of stress.

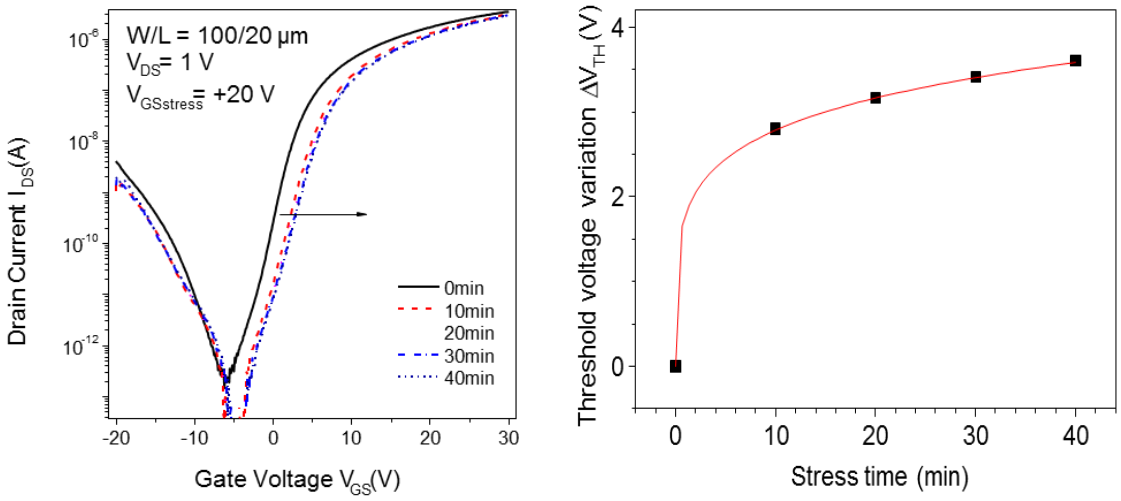

Figure 4.6: Shift of the characteristics of ECR-CVD SiO2 based TFTs during +20V gate bias stress.

Together with the first previous results obtained by the IMM group, present results seem indicate that present ECR-CVD SiO_2 not able to reach our goal if the maximum annealing temperature is limited to 180°C.

2.3 TFTs using ALD deposited Al_2O_3 as gate insulator

Other possibility to reach our goal was to check other insulators than silicon dioxide. Alumina can be the solution, particularly when deposited by Atomic Layer Deposition (ALD) technique. The very low deposition rate will insure a “smooth” deposition and then good interface with the active layer of TFTs.

Thermal ALD Technique was used by IMEC-Leuven (Belgium) team to deposit Al_2O_3 layer for us at 150°C using tri-methyl aluminum (TMA) and H_2O as precursors. The deposition conditions are summarized in Table 4.6.

Pulse time (s)				Chamber pressure (mbar)	Flow rate (sccm)
TMA	Purge	H_2O	Purge		
0.5	15	0.5	15	0.3	500

Table 4.6: Deposition conditions of Al_2O_3 by Thermal ALD in IMEC.

To check only the possibility to use this Al_2O_3 film as gate insulator for ours TFTs, some silicon TFTs were processed first in IETR, then Al_2O_3 films were deposited in IMEC Leuven using their ALD reactor and finally TFT's process was finished in IETR.

Before fabricating TFTs, the quality of Al_2O_3 film and its interface with silicon were checked through the characteristics of Aluminum-Al_2O_3-N type silicon wafer MOS structure. Figure 4.7 presents High frequency (1 MHz) and Quasi-static C-V characteristics of this structure, after post-annealing at 180°C during 1 hour. Important modulation of the quasi-static capacitance is observed; that means high electrical quality of the interface alumina-silicon. This result is not surprising as low interface defect density was previously found when using thermal ALD. TMA can provide hydrogen for the passivation role of silicon surface by hydrogen. Moreover, alumina was found as hydrogen reservoir providing hydrogen to silicon surface during post-annealing steps [4].

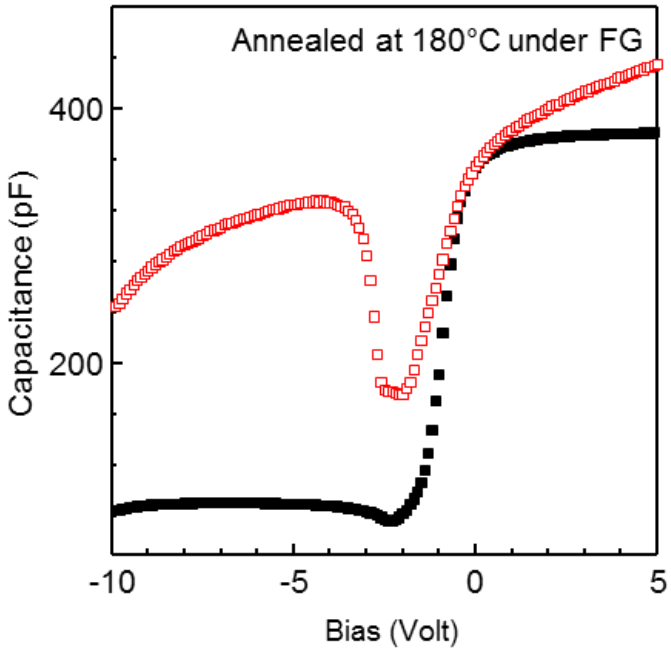

Figure 4.7: High frequency 1 MHz (black full square curves) and Quasi-static (red open square curves) C-V characteristics of Al-Al_2O_3-N type Si wafer MOS structures after 1h annealing at 180°C.

However and unfortunately, quasi static capacitance curve is not flat, meaning important leakage current in the structure. This leakage current can be reduced by annealing at higher temperature that is not the purpose of the present work.

Using the HF capacitance in accumulation regime, the relative dielectric constant of present alumina film was found to be 5.2.

As such alumina insulator film was not used before as gate insulator of silicon TFTs, we checked its use with Solid Phase Crystallized (SPC) Polycrystalline silicon based TFTs as well as with present microcrystalline silicon based TFTs. Indeed, SPC process is well established in IETR and it is used as reference process when testing new material.

The SPC process starts with a deposition of undoped and doped amorphous silicon layers by LPCVD at 550°C and then both layers are solid phase crystallized at 600°C under vacuum during 8 hours [5]. The following process steps are similar to the description of the µc-Si TFT's process.

Figure 4.8 presents the transfer characteristics of same size (W/L = 100/20µm) SPC TFTs, one using silicon dioxide deposited by sputtering as gate insulator [6] and the other using ALD-Al_2O_3 as gate insulator. Both TFTs were annealed under forming gas at 200°C at the end of the process. This temperature is the maximum temperature during both processes. Table 4.7 summarizes the electrical parameters of both TFTs.

Even if the mobility is lower when using alumina, the electrical parameters of alumina based SPC TFTs, subthreshold slope and threshold voltage can be considered as very interesting.

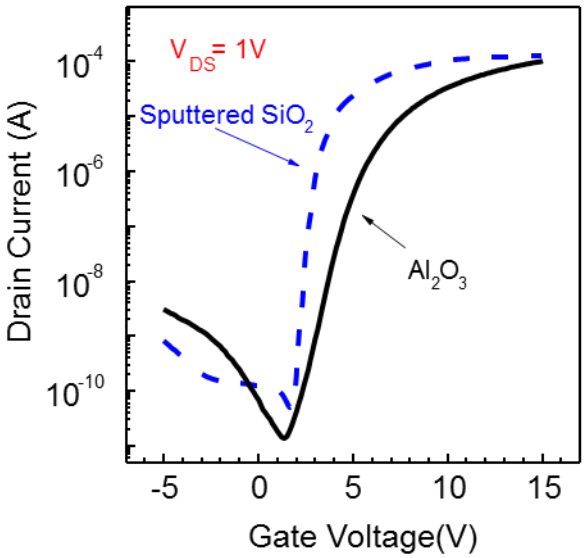

Figure 4.8: Transfer characteristics of W/L = 100/20 µm solid phase crystallized polycrystalline silicon TFTs, one using silicon dioxide deposited by sputtering as gate insulator [6] (dashed blue curve) and the other using ALD-Al_2O_3 as gate insulator (continuous black line).

Gate insulator	Mobility (cm^2/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)
ALD Al_2O_3	65	0.76	7.67
Sputtered SiO_2	120	0.24	5.2

Table 4.7: Electrical parameters of polycrystalline TFT using ALD Al_2O_3 and sputtering SiO_2 as gate insulator

After checking the quality of alumina-silicon interface through C-V measurements and the quality of alumina as gate insulator of silicon TFTs, the next step was to use it as gate insulator of microcrystalline silicon TFTs. Figure 4.9 shows a transfer characteristic of 100/20 µm µc-Si TFT using 100 nm thick Al_2O_3 as gate insulator. Leakage gate current is also represented in this figure. The electrical parameters of this TFT are shown in the Table 4.8.

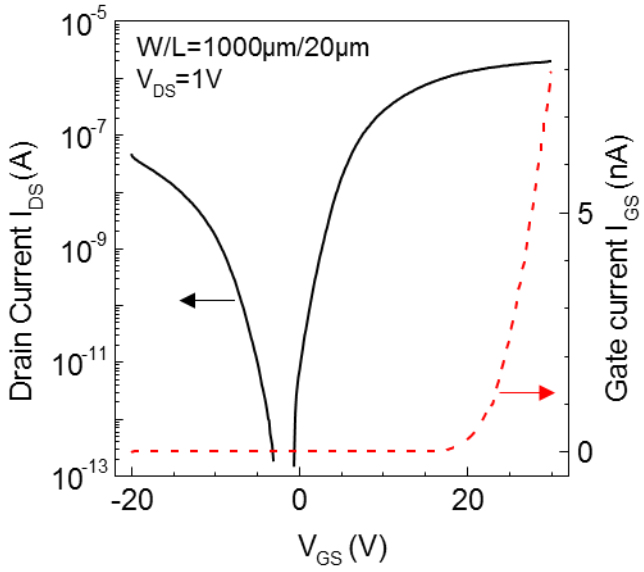

Figure 4.9: Transfer characteristic of microcrystalline silicon TFT using ALD deposited Al_2O_3 as gate insulator (continuous black line) and behavior of the leakage gate current (dashed red line)

Mobility (cm²/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)
0.5	1.3	7.51

Table 4.8: Electrical parameters of microcrystalline TFT using ALD deposited Al2O3 as gate insulator

The gate current stays very low until +20V gate voltage. It increases at higher gate votage but stays low, reaching 8 nA at 30V. The threshold voltage and subthreshold slope are not

too large. However, the mobility is lower than 1 $cm^2/V.s$ and the off-current increases highly when reverse gate voltage increases.

2.4 TFTs using PECVD deposited Si_3N_4 as gate insulator

As the stability of silicon nitride based TFTs was shown to be very important, it may useful to keep silicon nitride as gate insulator, changing only the deposition parameters and then trying to improve the interface between silicon nitride and microcrystalline silicon. The purpose is always to increase the mobility. The final goal is to reach at least a mobility of 5 $cm^2/V.s.$, needed for the use of these TFTs in high resolution Displays.

We present here first tentative to change this interface. The idea of this study is to create more efficient Si/SiN interface using multilayer silicon nitride. By this idea, the deposition of silicon nitride is divided into 2 runs. During the first run of silicon nitride deposition, we remove the NH_3 gas injection in order to ameliorate the interface quality. During the second run, the NH_3 is added in the reaction gases for complete the whole silicon nitride layer.

The deposition conditions of these 2 runs are summarized in Table 4.9. In this study, the deposition times for the 1^{st} run and the 2^{nd} run are 7.5 minutes and 22.5 minutes, respectively. The thickness of the whole silicon nitride layer is 300 nm. After the deposition, the silicon nitride is annealed at 180 °C during 2 hours under N_2.

Run	Power (W)	Pressure (mbar)	D_{A-K} (cm)	Temperature (°C)	SiH_4 (sccm)	N_2 (sccm)	NH_3 (sccm)
1^{st}	30	0.6	4.5	150	2	80	-
2^{nd}	30	0.6	4.5	150	2	80	40

Table 4.9: Deposition conditions of multilayer silicon nitride by PECVD

2.4.1 Transfer characteristic of TFTs using multilayer silicon nitride as gate insulator

Figure 4.10 presents transfer characteristic of µc-Si TFT using multilayer silicon nitride as gate insulator. The channel size of measured TFT is W/L = 100/20 µm. The drain voltage is V_{DS} = 1V. The TFT is measured for 2 times successively in order to investigate its stability. Table 4.10 summarizes the electrical parameters of this TFT for each measurement.

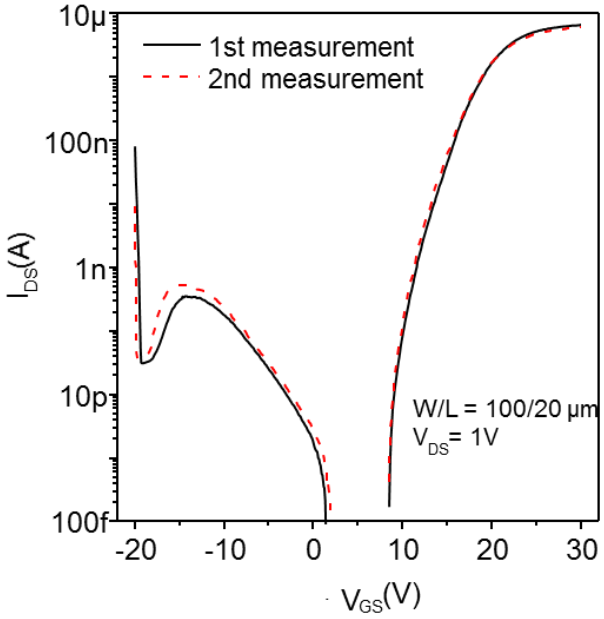

Figure 4.10: 2 successive measurements of transfer characteristics of µc-Si TFT using multilayer silicon nitride as gate insulator.

Measurement	Mobility (cm²/Vs)	Subthreshold slope (V/Dec)	Threshold voltage (V)
1st	8.6	1.03	17.92
2nd	7.6	0.95	17.88

Table 4.10: Electrical parameters of µc-Si TFT using multilayer silicon nitride as gate insulator for 2 successive measurements.

Obviously, the mobility of this TFT with multilayer silicon nitride as gate insulator has been largely increased comparing to the TFT using monolayer silicon nitride, which is presented in the Chapter 3. From the transfer characteristic of first measurement, we extract a mobility of 8.6 cm^2/Vs, while the TFT using monolayer silicon nitride demonstrated in Chapter 3 has only a mobility of 0.77 cm^2/Vs which is very similar to that of amorphous silicon TFT. Indeed, the mobility of the TFTs using monolayer silicon nitride is insufficient for some applications such as the high resolution AMLCD and especially the AMOLED. Normally, the mobility needed for AMOLED or high resolution AMLCD should be at least in the range of 2 – 5 cm^2/Vs [7]. Therefore, the mobility obtained from this study might be useful for some applications that need high mobility.

Additionally, these 2 types of TFT use exactly same material, microcrystalline silicon, as active layer. The thickness of the active layer is 100 nm for both TFTs. The improvement of mobility can be attributed to the insertion of a silicon nitride layer, which is deposited without NH_3 gas, between microcrystalline silicon and the silicon nitride presented in Chapter 3. This study indicates the possibility to increase the mobility of TFT by the amelioration of the usually used silicon nitride.

2.4.2 TFTs using multilayer silicon nitride as gate insulator under prolonged gate bias stress

Figure 4.11 shows the transfer characteristics of microcrystalline silicon TFT using multilayer silicon nitride as gate insulator after a prolonged gate bias stress. The stress gate voltage is fixed at $V_{GSstress}$ = +20 V.

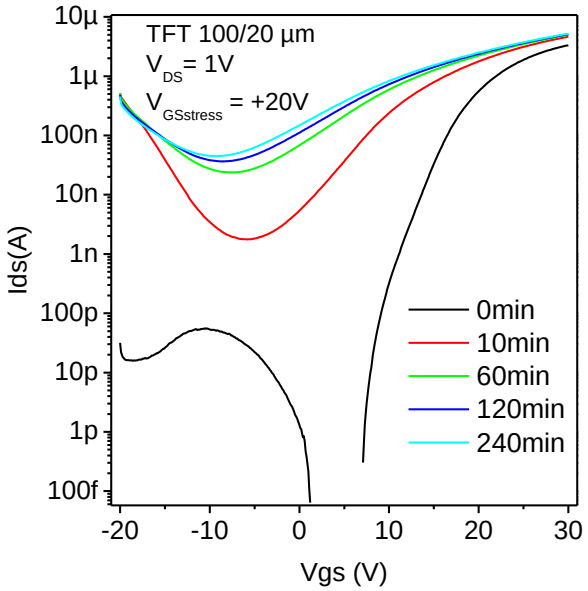

Figure 4.11: Microcrystalline silicon TFT using multilayer silicon nitride as gate insulator under prolonged gate bias stress

The prolonged gate bias stress is highly detrimental for the transfer characteristic of TFT. The off-current is significantly increased and the subthreshold slope is largely degraded to 10 V/dec after 10 minutes stress. After 4 hours stress, the degradation became more significant in terms of inverse current and subthreshold slope. These degradations are shown in Table 4.11

Stress time (s)	Off-current @ V_{GS} = -15V	Subthreshold slope (V/Dec)
0	26 pA	1.16
600	38 nA	5.68
14400	85 nA	12.96

Table 4.11: Off-current at V_{GS}=-15V and subthreshold slope of TFT using multilayer silicon nitride as gate insulator under gate bias stress

It is well-know that the subthreshold slope of TFT is closely relative to the quality of the interface between active layer and gate insulator. Here, the subthreshold slope of microcrystalline silicon TFT using multilayer silicon nitride as gate insulator is largely deteriorated after prolonged gate bias stress. Indeed, the subthreshold slope of TFT can be expressed as follow:

$$S = \frac{k_B T ln(10)}{q}\left[1 + \frac{\sqrt{q^2 \varepsilon_0 \varepsilon_{Si} N_{ep}}}{C_{INS}} + \frac{q^2 N_{SS}}{C_{INS}}\right] \quad (4.1)$$

where, C_{INS} is the capacity per unit area of the gate insulator. N_{ep} and N_{SS} are the densities of deep states in the channel and at the insulator/channel interface, respectively.

This expression indicates that the increase of subthreshold slope might be due to the creation of deep states in the channel or at the interface. It seems that the accumulation of electrons, which is caused by positive gate bias stress, results on defects in the channel or at the insulator/channel interface. Considering that the microcrystalline silicon material is stable, as shown in Chapter 3, the defect creation seems to be located at the interface or even inside the silicon nitride layer deposited by 1st run.

3. Conclusion

Envisaging the low mobility of TFT presented in Chapter 3, in this chapter, µc-Si TFTs have been fabricated using different gate insulators in order to improve the mobility.

The gate insulators used here include RF sputtered and ECR-CVD deposited SiO_2, thermal ALD deposited Al_2O_3, and PECVD deposited multilayer Si_3N_4. It is found that the electrical performance of µc-Si TFTs, which have same active layer, is impacted by different gate insulators and deposition conditions used. Unfortunately, all these gate insulators used couldn't improve mobility without sacrificing electrical stability of TFT.

However, silicon dioxide deposited by RF sputtering at fixed temperature seems one of the best ways to reach both acceptable mobility and stability. Silicon nitride can be the other way if working on the deposition conditions.

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Conclusion

The goal of this thesis was to fabricate microcrystalline silicon TFT, with high electrical stability and good mechanical flexibility, on flexible and transparent substrate.

Firstly we have fabricated N-type microcrystalline silicon TFT on glass substrate using silicon nitride as gate insulator. This type of TFT benefits from a weak off-current, 1.6 pA at V_{GS} = -20 V and 23 pA at V_{GS} = -30V. In addition, the subthreshold slope (1.1 V/Dec) and the threshold voltage (10.12 V) are acceptable. Inspite of the relative lower mobility (0.77 $cm^2/V.s$), it can be acceptable for some sensor applications.

We have studied the electrical stability of this TFT by applying gate bias stress. The results of this experiment manifested the electrically stable property. The shift of the threshold voltage is only 1.2 V under extreme stress conditions (high stress temperature 50°C and high stress bias 35V). It was also investigated to research the origin of instability as follow. These threshold voltage shifts followed a logarithmic law, indicating that the shifts are mainly caused by carrier trapping mechanism in the gate insulator.

Secondly we have transferred the same microcrystalline silicon technology on PEN substrate. We have chosen a 25 µm thick PEN (Provided by Dupont Teijin Films, reference TEONEX Q831A) as substrate. This type of PEN is transparent and has a maximum process temperature of 180 °C. The TFT fabricated on this PEN has a mobility of 0.45 cm^2/Vs, a subthreshold slope of 1.3 V/Dec and a threshold voltage of 17 V. A prolonged gate bias stress has also been performed for the TFT on PEN, where threshold voltage shift is 1.6 V after 6 hours gate bias stress under V_{GS} = +20V at room temperature.

We have measured the transfer characteristics of this TFT during mechanical tensile bending with different curvature radius. The minimum curvature radius in this measurement is R = 5 mm. It was observed that the on-current of TFT increases when the curvature radius decreases, which means the mechanical strain on TFT surface increases. On-current increase featured an approximate linear growth under the strain with a slope of 93, indicating a high sensitivity of TFT's parameter to mechanical strain.

After the PEN substrate was re-flattened from tensile and compressive bending (with different curvature radii), the transfer characteristics of TFT were also measured. The

minimum curvature radius in this measurement for both tension and compression is R = 0.75 mm. The transfer characteristics of TFTs were kept exactly similar after either tensile or compressive bending until 1.5 mm, except a slight increase of gate current leakage for R = 1.5 mm withstood to tensile bending. For R = 0.75 mm, obvious degradations of on-current and gate leakage current have been observed. Here, the degradation after tensile stress was more important than compressive stress. All the results above illustrated that the possibility to bend microcrystalline silicon TFT, for both tension and compression, even subjected to a low curvature radius, which is comparable with organic TFTs.

We have calculated the mechanical strain on the TFT using a model developed by Princeton Group. At minimum curvature radius, 1.5 mm, for both tension and compression, the TFT holds a mechanical strain about 0.6 – 0.7 %. This value is consistent with the previous result found in IETR. This means that both types of TFTs are limited by the same strain value even if lower curvature radius was reached in this thesis. We have assumed that the main limitation of silicon TFTs comes from the mechanical behavior of silicon nitride material. In order to reach smaller curvature radius, the best solution is to reduce even more substrate thickness.

Finally, we have tried to improve mobility of microcrystalline silicon TFT without sacrificing electrical stability by fabricating TFTs using different gate insulators. The active layers of all the TFTs are the same microcrystalline silicon film deposited at low temperature. The gate insulators used include RF sputtered and ECR-CVD deposited SiO_2, thermal ALD deposited Al_2O_3 and PECVD deposited multilayer Si_3N_4. However, all these gate insulators used couldn’t improve mobility without sacrificing electrical stability of TFT.

Publications

International publications:

M. L. Samb, H. Dong, E. Jacques, G. Sissoko, A. Seidou-Maiga, T. Mohammed-Brahim, "Thinning the active layer of TFTs", ECS Transactions, 64, 10, (2014), pp. 9-16

H. Dong, Y. Kervran, N. Coulon, O. De Sagazan, E. Jacques, T. Mohammed-Brahim, "Highly flexible microcrystalline silicon N-type TFT on PEN bent to a curvature radius of 0.75 mm", IEEE Transaction on Electron Devices. (Accepted)

International conferences:

H. Dong, E. Jacques, K. Kandoussi, C. Simon, N. Coulon, T. Mohammed-Brahim, "As-deposited crystallized silicon TFTs for active display addressing", Proceeding Active Matrix Flat Panel Displays 2012, Kyoto, Japan, July 4-6, (2012), pp. 107-110

T. Nogushi, K. Sugihara, K. Shimoda, T. Gushiken, T. Okada, E. Jacques, H. Dong, T. Mohammed-Brahim, "Poly Si TFTs formed by low temperature process using blue laser diode annealing", The 14th International Meeting on Information Display (IMID 2014), Daegu, Korea, August 26-29, (2014)

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M. L. Samb, H. Dong, E. Jacques, G. Sissoko, A. Seidou-Maiga, T. Mohammed-Brahim, "The use of very thin active layer to improve the characteristics of TFTs based on not single crystalline semiconductors", 11th International Conference on Thin Film Transistors ITC 2015, Rennes, France, February 25-28, (2015)

H. Dong, Y. Kervra, N. Coulon, O. De Sagazan, E. Jacques, T. Mohammed-Brahim, "Thin film transistors on polyimide substrate under high deformations", 11th International Conference on Thin Film Transistors ITC 2015, Rennes, France, February 25-28, (2015)