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Simulations Monte-Carlo et leur contribution à la compréhension des mécanismes d'aléas logiques (SEU) dans les technologies CMOS 65/32/20nm

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Résumé

L’augmentation de la densité et la réduction de la tension d’alimentation des circuits intégrés rend la contribution des effets singuliers induits par les radiations majoritaire dans la diminution de la fiabilité des composants électroniques aussi bien dans l’environnement radiatif spatial que terrestre. Cette étude porte sur la modélisation des mécanismes physiques qui conduisent à ces aléas logiques (en anglais "Soft Errors"). Ces modèles sont utilisés dans une plateforme de simulation, appelée TIARA (Tool sulte for rAdiation Reliability Assessment), qui a été développée dans le cadre de cette thèse. Cet outil est capable de prédire la sensibilité de nombreuses architectures de circuits (SRAM, Flip-Flop, etc.) dans différents environnements radiatifs et sous différentes conditions de test (alimentation, altitude, etc.) Cette plateforme a été amplement validée grâce à la comparaison avec des mesures expérimentales effectuées sur différents circuits de test fabriqués par STMicroelectronics. La plateforme TIARA a ensuite été utilisée pour la conception de circuits durcis aux radiations et a permis de participer à la compréhension des mécanismes des aléas logiques jusqu’au noeud technologique 20nm.

Abstract

Aggressive integrated circuit density increase and power supply scaling have propelled Single Event Effects to the forefront of reliability concerns in ground-based and space-bound electronic systems. This study focuses on modeling of Single Event physical phenomena. To enable performing reliability assessment, a complete simulation platform named Tool suIte for rAdiation Reliability Assessment (TIARA) has been developed that allows performing sensitivity prediction of different digital circuits (SRAM, Flip-Flops, etc.) in different radiation environments and at different operating conditions (power supply voltage, altitude, etc.) TIARA has been extensively validated with experimental data for space and terrestrial radiation environments using different test vehicles manufactured by STMicroelectronics. Finally, the platform has been used during rad-hard digital circuits design and to provide insights into radiation-induced upset mechanisms down to CMOS 20nm technological node.

Résumé en français

Introduction générale

La fiabilité d'un système ou d'un circuit électronique représente la probabilité de fonctionnement sans défaillance pendant une période de temps déterminée et dans les conditions spécifiées [1]. Il existe plusieurs phénomènes de dégradation de fiabilité des composants électroniques : électro-migration, rupture de grille, dégradation par porteurs chauds, décharges électrostatiques, verrouillage d'un composant (latch-up), stress électromagnétique et effets des radiations.

Avec la réduction des dimensions des transistors, les effets singuliers induits par la radiation sont devenus un enjeu majeur pour les technologies déca-nanométriques en environnement spatial et terrestre. Cela est causé par la baisse de la tension d'alimentation et la capacité des ndu circuit qui finalement conduisent à la diminution de la charge électrique utilisée pour établir un état logique.

Pour qualifier un composant électronique pour une application donnée, différentes méthodes de test sont utilisées : à la fois les méthodes expérimentales qui permettent de statuer sur la sensibilité des technologies et les modélisations qui permettent les analyses des mécanismes physiques au niveau des transistors.

L'objectif de cette thèse est de participer à la compréhension des mécanismes d'aléas logiques (SEU) dans les circuits numériques en technologies CMOS déca-nanométriques dans les environnements radiatifs (irradiations ions lourds, alpha, neutron et proton) en utilisant la simulation Monte-Carlo. Ce travail présente le développement de la plateforme de simulation complète permettant la simulation des SEU et l'évaluation précise des sections efficaces du taux des SEU. Ensuite, cette plateforme est utilisée pour adresser les problèmes récents qui sont discutés par la communauté. La plateforme est développée chez un fabriquant de circuits intégrés (STMicroelectronics), ce qui permet de bénéficier directement des données technologiques, des modèles des transistors calibrés avec les mesures sur silicium, des bibliothèques de cellules industrielles ainsi que d'une intégration avec l'environnement

CAD en place (Computer-Aided Design). La structure innovante de la plateforme et le couplage avec les outils industriels sont proposés pour rendre possible la simulation des différentes architectures de circuits allant de simples mémoires statiques SRAM aux solutions durcies aux radiations très complexes. Grâce à l'intégration avec les outils standards, la plateforme peut estimer la sensibilité de n'importe quel circuit tant que la géométrie et le schéma électronique sont disponibles.

Chapitre I L'état de l'art

Introduction

Les circuits électroniques sont soumis aux rayonnements ionisants naturels dans l'environnement spatial, atmosphérique et terrestre. Les effets induits par ces radiations se traduisent par trois types de phénomènes :

- Les effets singuliers
- Les effets cumulatifs de la dose
- Les défauts de déplacement

Ce travail de recherche est focalisé sur la famille des événements singuliers et plus précisément sur les aléas logiques qui sont les phénomènes observés majoritairement.

Ce chapitre présente dans un premier temps l'origine, les caractéristiques et les effets des particules qui sont présentes dans les environnements spatial et terrestre. Les standards de caractérisation de la sensibilité des circuits microélectroniques sont décrits avec une brève description des facilités de tests, suivis par une analyse approfondie de l'état de l'art des méthodes de simulation présentes dans la littérature. Cette analyse permet de définir les objectifs de ce travail de recherche.

Les environnements radiatifs

Dans cette partie, les environnements radiatifs spatial et terrestre sont décrits. La description de l'environnement spatial traite le cas du rayonnement cosmique (Galactic Cosmic Rays ou GCR) à origine extragalactique, du Soleil qui est la plus grande source de radiation dans notre système solaire et des ceintures de radiation composées des particules piégées par le champ magnétique de la Terre. Dans l'environnement terrestre les sources majeures de radiation sont les neutrons atmosphériques produits dans les parties hautes de l'atmosphère par les rayons cosmiques, et les particules alpha provenant de la contamination des circuits intégrés.

Mécanismes d'événements singuliers

Les particules énergétiques présentes dans les environnements radiatifs interagissent avec la structure semi-conductrice par les mécanismes d'ionisation directe et indirecte. Cette interaction conduit à la déposition de la charge électrique. Ensuite, cette charge est collectée par les transistors du circuit en créant des impulsions de courant parasites qui peuvent conduire aux aléas logiques sous certaines conditions décrites dans cette partie du manuscrit.

Caractérisations de la sensibilité des circuits

La Figure 1.20 présente la méthodologie de développement et de qualification de la technologie utilisée à STMicroelectronics en illustrant la modélisation, les tests et méthodes de durcissement. Pour standardiser les caractérisations de la sensibilité des circuits, des normes spécifiques ont été introduites. Les normes JEDEC JESD89A pour l'environnement terrestre [12] et JESD57 pour l'environnement spatial [13] sont décrites.

Caractérisations expérimentales

Les méthodes expérimentales de caractérisation des circuits sont présentées : dans un premier temps les caractérisations temps réel et les caractérisations accélérées.

Méthodes de modélisation

Cette partie discute des outils de simulations utilisés pour la modélisation des effets singuliers : les solutions basées sur la simulation TCAD (Technology Computer-Aided Design) sont analysés suivies par les simulateurs Monte-Carlo développées par l'industrie (IBM, ONERA) et les laboratoires de recherche (Université Vanderbilt, CEM-2).

Les objectifs de recherche de cette thèse

L'analyse de l'état de l'art a montrée la capacité des outils à simuler les effets singuliers, mais a démontrée également les limitations communes qui limitent l'intérêt de leur utilisation par un fabriquant de circuits intégrés. Cette étude porte sur le développement et l'intégration industrielle de la plateforme de simulation qui bénéficie des données disponibles chez le fondeur. De plus, les contraintes suivantes doivent être satisfaites :

- Possibilité de simuler différentes architectures de circuits
- Possibilité de simuler différents ntechnologiques

- Possibilité de simuler différents environnements radiatifs
- Possibilité d'effectuer la simulation pendant la phase de conception du circuit avant la fabrication du composant
- Possibilité d'évaluer et valider l'efficacité des différentes méthodes de durcissement.

Annexes

Deux annexes présentent les différents types d'événements singuliers, les formules de calculs de la section efficace SEU et le taux d'erreurs (Soft Error Rate SER).

Chapitre II La plateforme TIARA (Tool Suite for Radiation Reliability Assessment)

Introduction

Le chapitre II présente la plateforme de simulation baptisée TIARA (Tool Suite for Radiation Reliability Assessment). Les objectifs de la plateforme ont été définis dans la section 1.7.

Flot de simulation

La Figure 2.1 présente le schéma bloc de la plateforme TIARA : les entrées, le cde simulation (avec les modules majeurs) et les sorties. Il existe 3 types d'entrées qui doivent être fournies à TIARA pour la simulation de la sensibilité du circuit :

- La géométrie en format GDS, le schéma électrique du circuit et les modèles des transistors du PDK
- Les modèles d'environnements
- Les informations technologiques telles que la géométrie de la couche de métallisation et les paramètres pour les modèles de transport.

Le cde simulation crée dans un premier temps la structure équivalente en 3D en utilisant les données géométriques GDS, puis les événements radiatifs sont générés. Toutes les particules ionisantes sont ensuite transportées par les couches de la métallisation et du volume actif du silicium. La simulation électrique complète (SPICE) est utilisée pour déterminer s'il y a un impact de la particule sur le fonctionnement du circuit.

Les sorties de TIARA peuvent être représentées sous forme de taux d'erreur (pour les neutrons ou particules alpha), de sections efficaces

utilisées (dans le cas des ions lourds), de taux d'aléas multiples (MCU) et de cartographies d'erreurs.

Création de la structure

La création de la structure équivalente est basée sur l'information géométrique fournie lors de la phase de design au format GDS. Ce format constitue un standard industriel utilisé par tous les outils de conception du lay-out de la cellule et a été choisi pour répondre aux objectifs définis dans la section 1.6. La structure simulée modélise tous les drains des transistors qui sont polarisés en inverse et qui peuvent collecter la charge induit par un ion.

Les modèles d'environnements

Les modèles d'environnements tiennent compte d'environnements terrestre (les interactions entre neutron et Silicium et les particules alpha) et spatial (simulation des ions lourds ou des protons). La structure détaillée du module est présentée sur la figure 2.2. Transport de la particule à travers la métallisation Pour modéliser le transport de la particule à travers la métallisation, il est considéré que cette métallisation est composée de la couche de dioxyde de silicium (SiO2). Cette hypothèse a été vérifiée dans la référence [40]. Pour extraire l'information de la perte d'énergie dans la passivation, les tableaux de Ziegler ont été implémentés directement dans TIARA.

Transport de la particule à travers le substrat

Ce module, qui permet de modéliser la génération, le transport et la collection des charges par les transistors de la structure semi-conductrice, est le module le plus critique pour l'estimation de taux d'erreur. TIARA classifie les impacts des particules en deux types : les impacts directs dans la jonction de la structure polarisée en inverse (modèle de courant de dérive) et les impacts en dehors de la jonction polarisée en inverse (modèle de diffusion-collection).

Le modèle de courant de diffusion-collection est calculé à partir des équations suivantes 2.2-2.5 et 2.11-2.12.

Les critères de basculement

TIARA utilise plusieurs critères de basculement développés dans le cadre de ce travail de recherche. Le critère le plus précis est l'utilisation de la simulation électrique complète de la cellule simulée dans laquelle les impulsions des courants parasites sont injectées. Ce critère peut-être utilisé pour tous les circuits supportés par TIARA. Pour les mémoires

SRAM, il est possible d'utiliser les critères simplifiés qui diminuent le temps de simulation : le critère Imax=f(Tmax) pour les impacts hors drain (section 7.2) et le critère LET seuil pour les impacts dans le drain (section 7.3).

Les résultats de simulation

Les résultats de simulation peuvent être présentés sous différentes formes selon l'environnement simulé. Dans le cas des ions lourds, les valeurs de la section efficace sont calculées par default pour chaque valeur de LET à partir de l'équation 2.15. Dans les cas des neutrons/alphas, les valeurs de SER sont calculées. De plus, TIARA calcule le taux des événements multiples pour toutes les mémoires simulées. Les figures 2.10 et 2.11 présentent les visualisations générées par TIARA : les cartographies d'erreurs et la visualisation des impacts des particules dans la structure 3D.

Intégration de TIARA avec l'environnement CAD

TIARA est couplée avec plusieurs outils CAD pour permettre l'utilisation industrielle de la simulation pendant la phase de conception des circuits intégrés. La section 8.1 décrit le parseur GDS et le couplage de TIARA avec SPICE et les sections 8.2/8.3 montrent les parallélisassions de TIARA sur le système distribué et l'implémentation dans le GPU.

La précision et les incertitudes

La précision de la simulation TIARA dépend du nombre de particules simulés. Grâce à l'utilisation des parallélisassions massives la précision augmente significativement (les erreurs bars sont inférieurs à 1Il existe 3 sources majeures d'incertitudes dans TIARA : 1) dues à la modélisation TCAD, 2) dues à la modélisation SPICE, et 3) dues à la prédiction du taux d'erreur. La description détaillée de toutes ces incertitudes peuvent être trouvés dans les tableaux 2.1-2.3.

Chapitre III Validation et capacités de la méthodologie TIARA

Introduction

Le chapitre présente la validation des estimations de la plateforme TIARA par la comparaison avec les tests expérimentaux dans les accélérateurs des particules.

Validation de TIARA dans les différents environnements radiatifs

La validation des résultats des simulations TIARA pour les différents environnements radiatifs a été effectuée en utilisant la mémoire conçue en technologie 65nm CMOS. Les figures 3.1, 3.2 et 3.3 présentent les simulations TIARA comparées avec les mesures expérimentales pour les ions lourds (effectuées à RADEF en Finlande et à UCL en Belgique), les particules alpha (effectuées à STMicroelectronics à Crolles en France) et les neutrons (effectuées à TRIUMF au Canada). Un bon accord a été trouvé pour tous les types d'environnements.

Estimation du taux d'aléas multiples (MCU)

Cette section présente les méthodes d'estimation du taux d'aléas multiples (MCU). Les valeurs des MCU simulées et expérimentales sont comparées sur la figure 3.6. Les cartographies des événements multiples sont également confrontées avec les résultats TCAD publiées dans la littérature. Le modèle de l'effet bipolaire parasite est proposé pour pouvoir étendre l'approche de simulation aux structures fabriquées avec la couche enterrée (deep N-well ou DNW).

Capacités additionnelles de TIARA

Les analyses supplémentaires de TIARA sont possibles grâce à l'intégration de TIARA avec les outils CAD commerciaux. Ces analyses sont démontrées en étudiant l'effet de la température, de la tension d'alimentation et des procédés de fabrication. De plus, TIARA permet de simuler plusieurs types de circuits. Ces simulations, comparées avec l'expérience, sont présentées pour les mémoires Dual-Port et les bascules logiques.

Chapitre IV Utilisation de TIARA pour les analyses avancées des mécanismes d'aléas logiques dans les circuits standards et durcis

Introduction

Le dernier chapitre de ce manuscrit présente les simulations les plus avancées de circuits très complexes : bascules logiques basées sur l'architecture DICE. De plus, les mécanismes physiques d'aléas logiques sont analysés et les sujets majeurs discutés par la communauté de radiations sont adressés : l'effet de Â« charge sharing Â» dans les structures robustes aux radiations basées sur le concept DICE et l'influence de spectre de la sensibilité sur la valeur de SER.

Expériences et simulations des bascules durcies en technologie 65nm

Une bascule logique basée sur l'architecture DICE a été conçue en technologie 65nm CMOS. La sensibilité de cette bascule aux ions lourds a été mesurée à RADEF en fonction de la valeur du LET de la particule et pour toutes les configurations statiques. L'expérience a été répétée pour les neutrons à TRIUMF et à STMicroelectronics pour les alphas. Les simulations ont été effectuées également pour tous ces environnements radiatifs : ions lourds, particules alphas et neutrons atmosphériques. La section 2.3 compare ces résultats :

- La figure 4.2 présente les sections efficaces des ions lourds en fonction de la valeur effective du pouvoir ionisant (LET) pour les quatre configurations statiques de la bascule,
- Le tableau 4.2 présente les résultats expérimentaux et les estimations de TIARA pour les ions lourds en fonction de l'angle de rotation du faisceau,
- Le tableau 4.3 présente les résultats des simulations et de l'expérience avec la source radioactive alpha.
- La section 2.4 analyse en détail le SER dÃ» aux neutrons. Les simulations TIARA présentées sur la figure 4.5 ont montré que la contribution des réactions élastiques neutron-silicium est beaucoup moins importante pour la bascule durcies que pour les implémentations standards.

Etude Monte-Carlo du "charge sharing"

Le mécanisme de "Charge sharing" est le problème majeur pour les bascules logiques utilisant le concept DICE. Ce mécanisme augmente avec l'intégration technologique parce que les distances entre les transistors sensibles de la structure diminuent et en conséquence la collection simultanée des charges par plusieurs transistors augmente. Pour pouvoir prendre en compte ce phénomène les modèles analytiques de transport des charges ont été d'abord calibrés avec les simulations TCAD. Les structures 3D TCAD utilisées pour cette étude sont présentées sur les figures 4.8 et 4.9. L'accord entre les impulsions parasites de courants estimés à partir des modèles analytiques et les simulations numériques TCAD est présenté sur la figure 4.10. La figure 4.13 donne les résultats simulés du mécanisme de Â« charge sharing Â» dans un seul well (collection simultanée par deux transistors NMOS ou deux transistors PMOS) et dans des wells séparés (collection simultanée par NMOS et PMOS). Il a été trouvé que la probabilité du Â« charge sharing Â» dans un seul well est 5 fois plus importante que dans les wells séparés. En se basant sur cette conclusion, différents placements de transistors ont été proposés afin de durcir la bascule logique (augmentation du LET seuil de la cellule de 50%).

Etude de l'influence des spectres de neutrons atmosphériques sur le SER

Pour analyser le SER dÃ» aux neutrons atmosphériques, les bases de données des réactions neutrons-siliciums ont été créées en utilisant une application GEANT4. Différents spectres des neutrons ont été choisis pour la compilation de ces bases des données : les spectres continus JEDEC, LANSCE et TRIUMF, et les spectres mono énergétiques 14, 50, 100, 150 MeV. La simulation GEANT4 utilise la dernière version GEANT4 4.9.4p01, et le module GPS pour générer le flux des neutrons. Les modèles physiques utilisés sont listés dans le tableau 4.5. Les figures de 4.18 à 4.21 présentent une analyse de la composition des bases de données pour chaque spectre en considération (les proportions des particules secondaires, le nombre de particules secondaires par réaction, le type de réaction et les histogrammes d'énergies des particules secondaires). La simulation TIARA a été couplée avec les bases de données pour estimer les SER des bascules logiques. Les figures 4.23 et 4.24 présentent les résultats des simulations et les résultats expérimentaux pour les sources mono énergétiques et les spectres continus. La différence entre le SER référence JEDEC et les spectres mono énergétiques est limitée à 25%, et 15% pour les spectres continus.

Projections sur les technologies d'avenir

Finalement, TIARA a été utilisée pour réaliser des projections de la sensibilité des circuits dans les technologies futures. Le circuit de test a été fabriqué par STMicroelectronics en technologie 32nm CMOS. Ce circuit embarque différentes architectures de mémoires SRAM. Les données expérimentales pour les ions lourds ont été collectées à RADEF en Finlande. TIARA a montré un bon accord avec l'expérience (voir figure 4.26). Dans un deuxième temps, les prédictions TIARA ont été réalisées pour la technologie 20nm CMOS en basant la simulation sur la géométrie réelle de la cellule, sur les premières modèles électriques SPICE des transistors et sur l'extrapolation des paramètres de transport à partir des données des technologies précédentes. Cette estimation a montré une diminution de la section efficace des ions lourds de 11-17% selon la valeur de LET de la particule. Les prédictions de l'efficacité du concept de DICE ont également été faites pour la technologie 32nm CMOS. Contrairement aux données de la littérature, TIARA a démontré que le concept DICE restera valable pour ce ntechnologique si les techniques de durcissement sont appliquées pendant la phase de conception du lay-out.

Conclusion générale

Cette thèse contribue à la réalisation et à l'intégration industrielle

de la plateforme de simulation Monte-Carlo baptisée TIARA (Tool Suite for Radiation Reliability Assessment). Cette plateforme a été conçue pour pouvoir être utilisée dès les premières étapes du développement de la technologie sans avoir besoin de la calibration avec les données expérimentales. De plus, TIARA bénéficie de la disponibilité des données technologiques du fabriquant des semi-conducteurs : les profiles des dopages, les modèles électriques des transistors calibrés avec les mesures sur silicium et les différentes conceptions industrielles. Les exigences définies au départ du développement de cette plateforme incluent la possibilité de simuler différents circuits numériques de différentes technologies CMOS dans les différents environnements radiatifs ainsi que l'évaluation et la validation des méthodes de durcissement.

L'architecture innovante décrit en détail dans ce manuscrit a satisfait toutes ces exigences. La structure modulaire du code est adaptée pour les nouveaux développements. Les modèles d'environnement ont été développés pour simuler les différents environnements radiatifs naturels : ions lourds, particules alpha et neutron atmosphériques. Les modèles de transport incluent des équations de diffusion-collection raffinées et un nouveau modèle de courant pour les impacts des particules dans le drain. Des nouveaux critères de basculement ont été proposés ainsi que des solutions novatrices de couplage entre TIARA et les outils CAD. De plus, TIARA a été implémentée pour permettra l' utilisation d'un système distribué et de GPUs (Graphics Processing Units) pour la parallélisassions massive, ce qui diminue drastiquement le temps de simulation.

TIARA a été validé par la comparaison avec les résultats des mesures expérimentales pour tous les types de radiation et un très bon accord a été observé pour toutes les valeurs de LET. Cette validation a été faite sur plusieurs ntechnologiques, en utilisant plusieurs circuits de test fabriqués par STMicroelectronics et sur plusieurs architectures de circuits numériques. Les capacités additionnelles du code ont également été démontrées (l'analyse d'influence de la température, de la tension d'alimentation et des procédés de fabrication sur la sensibilité du circuit).

TIARA a été utilisé pour expliquer les mécanismes des effets singuliers dans les architectures durcies aux radiations très complexes. Le Â« charge sharing Â» a été étudié et des solutions de robustisation ont été proposées. Finalement, des projections sur les futures technologies ont été faites et ont montré les sections efficaces des ions lourds des mémoires SRAM jusqu'au ntechnologique 20nm, et des bascules logiques durcies jusqu' au ntechnologique 32nm. La plateforme est toujours utilisée pour assister la conception des futures librairies (radhard et rad-tolérant) à STMicroelectronics. La majorité des solutions

de durcissement étudiées dans le cadre de cette thèse n'ont pas été présentées et reste confidentielles à STMicroelectronics.

Les prochains développements de TIARA sont prévus et envisage l'implémentation et la validation du modèle d'amplification bipolaire pour élargir l'utilisation de TIARA aux circuits fabriqués avec la couche enterrée. De plus, les simulations des circuits analogiques et mixtes (analogique-numérique) peuvent être effectuées après la validation des modèles de transport sur la plage complète de tension d'alimentation. Le troisième axe des futurs développements consiste à prendre en compte les différents matériaux présents dans la métallisation.

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Glossary

AF	Acceleration Factor, 29
ASTEP	Altitude SEE Test European Platform, Plateau de Bure, France, 29
BEOL	Back-End-Of-Line, 38, 45, 51
CAD	Computer-Aided Design, 2
CCD	Charge-Coupled Devices, 1, 5
CME	Coronal Mass Ejection, 7
CMOS	Complementary Metal-Oxide-Semiconductor, 2
DD	Displacement Damage, 5
DHC	Double-Height Cell, 103
DICE	Dual-Interlocked Storage Cell, 3
DRAM	Dynamic Random Access Memories, 1, 15
DUT	Device Under Test, 33
ECC	Error Correction Code, 139
EIA	Electronic Industries Alliance, 28
ESA	European Space Agency, 6
FEOL	Front-End-Of-Line, 45
FF	Flip-Flop, 3
GCR	Galactic Cosmic Rays, 6, 7
GPS	General Purpose Particle Source, 50
IC	Integrated Circuit, 2, 5
LBNL	Lawrence Berkeley National Laboratory, 30
LET	Linear Energy Transfer, 18
LSF	, 66

LSM Laboratoire Souterrain de Modane, Underground Laboratory of Modane, Fréjus, France, 30

MBU Multiple Bit Upset, 41
MCDASIE Monte Carlo Detailed Analysis of Secondary Ions Effects, 38
MCU Multiple Cell Upset, 41
MRED Monte-Carlo Radiative Energy Deposition, 38

NASA National Aeronautics and Space Administration, 6

PDK Process Design Kit, 46
PHISco Prediction of Heavy Ion Sensitivity code, 38

RHBD Radiation-Hardened-By-Design, 2, 60, 66
RPP Rectangular Parrallel Piped, 38
RT Real Time, 28

SAA South Atlantic Anomaly, 10
SBU Single-Bit Upset, 41
SCR Space Charge Region, 22
SEB Single Event Burnout, 41
SEE Single Event Effects, 1, 5, 6
SEFI Single Event Functional Interrupt, 41
SEGR Single Event Gate Rupture, 41
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SEMM Soft-Error Monte-Carlo Model 2, 38
SER Soft Error Rate, 2, 13, 47
SESB Single-Event Snap-back, 41
SET Single Event Transient, 5, 41
SEU Single Event Upset, 2, 5, 41
SOHO Solar & Heliospheric Observatory, 7
SPREG Single-Port Register, 75
SRAM Static Random Access Memory, 2
SRIM Stopping and Range of Ions in Matter, 15
STEREO Solar TErrestrial RElations Observatory, 7
STI Shallow Trench Isolation, 48

TCAD	Technology Computer-Aided Design, 24
TIARA	Tool sulte for rAdiation Raliability Assessment, 2, 45
TID	Total Ionizing Dose, 5

Introduction

Reliability is the probability that a device or a component will perform its intended function during a specified period of time under stated conditions [1]. Successful functioning is usually defined by the user's specification and belongs to the highest priorities for semiconductor companies because of the necessity of a product to satisfy client requirements. There exist numerous phenomena leading to the decrease of integrated circuit reliability: electromigration, gate rupture, hot carrier degradation, electrostatic discharge, latch-up, electromagnetic stress and radiation effects.

Historically, the presence of Single Event Effects (SEE) in electronic devices was predicted by Wallmark back in 1962 [2] but for the first time these effects were experimentally observed by Binder at al. [3] in 1975 and were attributed to the influence of Galactic Cosmic Rays. First soft errors at sea-level were observed by May and Woods from Intel [4] on Dynamic Random Access Memories (DRAM) and Charge-Coupled Devices (CCD) four years later. It was proven experimentally that alpha particles from natural package materials surrounding the device induce Soft Errors.

Together with technology feature size downscaling [5], SEE have become one of the major reliability issues in modern digital devices [6; 7]. This is mainly attributed to the constant reduction of supply voltage and node capacitance resulting in a decrease of the electrical charge used to store a logical value. Additionally, the continuous reduction in nodal capacitance makes it easier to cause an error [8], the reduced gate length increases the parasitic bipolar effect [9], and the decrease in the nodal separation and desire for higher packing density increases the probability of charge sharing after an ion-strike [10; 11].

In order to qualify a semiconductor component for a given application and quantify its failure rate in a radiation environment, dedicated norms have been developed, ex. JESD89A for Soft Error measurements induced by alpha particles and cosmic-rays [12] or JESD57 [13] / [14] to measure SEE from heavy-ion irradiation. These norms define the standard procedures to be followed during the experimental measurements in radiation facilities or with radiation sources. Experimental character-

izations can be classified in two major groups: real-time testings with a nominal particle flux and accelerated measurements exposing the die to intense radiation exceeding the natural radiation levels by many orders of magnitude.

Additionally, since the late 60's, computer simulations are extensively used for better understanding of SEE and to give an insight in underlying physical phenomena on a device level. Simulation models are developed based on the physical theory and prior experience from the radiation tests and can be applied during the design phase to optimize the circuit for its particular operating conditions and environment.

The objective of this dissertation is to participate in the understanding of physical mechanisms leading to Single Event Upset (SEU) in digital circuits in deca-nanometric Complementary Metal-Oxide-Semiconductor (CMOS) technologies in different radiation environments (i.e. heavy ion, alpha, neutron and proton irradiations) using the Monte-Carlo simulation approach. This work consists of developing a complete simulation platform allowing to simulate single event upsets and evaluate precisely the SEU cross-sections or Soft Error Rates. In addition, this platform will be used to address recent issues discussed by the radiation effects community. Moreover, the platform is developed at a semiconductor company (STMicroelectronics), thus all inputs benefit maximally from the availability of technological data, calibrated with silicon measurements transistor models, industrial designs and additionally it is integrated with an Integrated Circuit (IC) Computer-Aided Design (CAD) flow. The innovative platform structural design and coupling with CAD tools described in this work will be proposed to allow to perform simulations of different circuit architectures, ranging from simple Static Random Access Memory (SRAM) to very complex Radiation-Hardened-By-Design (RHBD) circuits, and can be used to assess the sensitivity of any digital circuit as long as its layout and electrical schematic are available.

Chapter I of this thesis presents necessary background information concerning space and terrestrial radiation environments that influence the functioning of integrated circuits followed by the explanation of interaction between radiation and semiconductor that is at the origin of the circuit malfunction. The experimental characterization methods are briefly discussed and state-of-the-art modeling approaches presented in the literature are investigated. Finally, a detailed analysis of their architectures and implemented physical models allows for selecting the most appropriate for industrial use and for proposing further developments in the frame of this thesis.

Chapter II describes the architecture of the simulation platform named Tool suIte for rAdiation Reliability Assessment (TIARA). Its flow is pre-

sented and accompanied by the description of TIARA inputs (as data from digital circuit design phase, dedicated environmental models and all technological information) and outputs (to which belong the estimation of upset cross-sections or Soft Error Rate (SER), multiple fail rates and error bit-maps). The physical models chosen in this framework are described in detail together with input parameter variation influence on radiation sensitivity assessment. TIARA's internal structure is exhaustively analyzed with the main implementation solutions and simulation uncertainties.

Chapter III conducts a validation of model choices implemented in TIARA by comparison of simulation results with experimental measurements. All test vehicles presented in this work were manufactured by STMicroelectronics in CMOS technologies ranging from 65nm down to 32nm node. Tests were performed at various radiation facilities and in different operating conditions. This validation is performed for all studied radiation environments (alphas, neutrons and heavy ions), on different circuit architectures (single- and dual-port standard- and high-density SRAM, standard and RHBD Flip-Flop (FF)). After the extensive validation, TIARA simulation capabilities accounting for temperature, power supply and process corner effects on sensitivity are demonstrated.

Chapter IV presents TIARA ability to perform complex Monte-Carlo analyses of SEE effects and insights in the latest topics being raised by the radiation effects community. At the beginning, the complete analysis of a Radiation-Hardened-By-Design FF based on Dual-Interlocked Storage Cell (DICE) concept is carried out with different radiations. In addition, several hardening techniques are evaluated by the Monte-Carlo simulation. Dedicated simulations are performed to address different Single-Event Upset mechanisms such as neutron-induced errors due to elastic and inelastic scattering and ever increasing with technology shrinking charge sharing. The effect of different neutron energy spectra on the neutron SER is studied and compared to experimental data obtained from experiments with continuous and mono-energetic sources. The final part shows TIARA's ability to anticipate radiation sensitivity for future technological nodes down to CMOS Bulk 20nm.

Chapter 1

Background of Single Event Effects in Electronic Devices

1 Introduction

As humankind, microelectronic devices are continuously exposed to natural radiations in space, high- and low-altitude terrestrial environments causing malfunctions that can be classified in three major types of radiation-induced phenomena:

- Single Event Effects (SEE) provoked by a single, energetic particle and being able to introduce both temporary as well as permanent device/circuit errors such as Single Event Transient (SET), , SEU, etc... The exhaustive classification is given in Appendix 1.
- Total Ionizing Dose (TID) causing slow and generally irreversible gradual degradation of the electrical device's performance.
- Displacement Damage (DD) creating defects by colliding with atoms of the crystal and influencing particularly opto-electronic components, CCD and bipolar technologies.

This work focuses on SEE and more particularly on the most often occurring SEE type - the SEU. TID and DD phenomena are out of the scope of this study. The detailed reference material for the TID can be found for example in the [15; 16; 17; 18; 19; 20; 21] and for DD in [22; 23; 24; 25; 26; 27].

The objective of this chapter is to present the necessary background information about the radiation environments and also about the main mechanisms encompassed in this thesis.

The chapter starts with a description of major space and terrestrial radiation environments to which electronic devices are exposed in normal operating conditions. The second part explains interactions be-

tween these environment and a semiconductor structure; it also introduces all Single Event physical phenomena leading to a circuit malfunction. In the third part, the experimental IC characterization standards are described followed by a brief presentation of several radiation test facilities. Then, the most common modeling approaches existing in the literature are analyzed in order to put the advantages and drawbacks of the-state-of-the-art simulations into perspective and finally, define the objectives of this research work.

2 Radiation environments

This section presents space and terrestrial natural radiation environments whose impact on microelectronic devices is characterized in this study. Origins of space radiation are continuously studied and still not completely identified. Nevertheless, the environments in the vicinity of the Earth are well characterized thanks to National Aeronautics and Space Administration (NASA) and European Space Agency (ESA) programs that allowed development of environment models. Particles coming from space produce additionally particle showers in Earth's atmosphere thus influencing the electronics on avionic altitudes and even at sea-level.

2.1 Space Environment

There are three main contributors to high-energy particle radiation environments in space. The first is comparatively a low-level flux of ions called Galactic Cosmic Rays (GCR) coming from outside of our solar system. The second is the radiation emitted by the Sun, characterized by high fluxes of protons and heavier ions. The third are particles trapped by Earth's magnetic field such as Van Allen belts.

Galactic Cosmic Rays

Galactic Cosmic Rays were discovered by Victor Hess in 1912 (co-awarded a Nobel Prize in Physics 1936) who first measured levels of atmosphere ionization and observed its increase as a function of altitude, thus proving the extra-terrestrial origin of this radiation. The measurements were done both during the day and night excluding the influence of the Sun.

GCR are high-energy charged particles that originate outside of our solar system and are attributed to be remnants from supernova explosions. They are mainly composed of protons (87%), alpha particles (12%) and heavier ions (1%) with energies up to 10^{11} GeV and fluxes ranging from 1 to 10 $cm^{-2} \cdot s^{-1}$ outside Earth's atmosphere. Although

the GCR fluxes are relatively low, they are a major threat for space-borne electronics causing SEE because of their extremely high energies and ability of penetration through all space regions as well as space-craft shielding.

Figure 1.1(a) presents a GCR composition as a function of atomic number on top of the atmosphere [29]. Typical energy spectra for few of the major elements during solar maximum and solar minimum conditions [28] are shown in Figure 1.1(b). As seen, they peak around 1 GeV per nucleon. The ion fluence for energies inferior to 10 GeV per nucleon is modulated by the Sun's magnetic field and solar wind. This influence is discussed in the following paragraph.

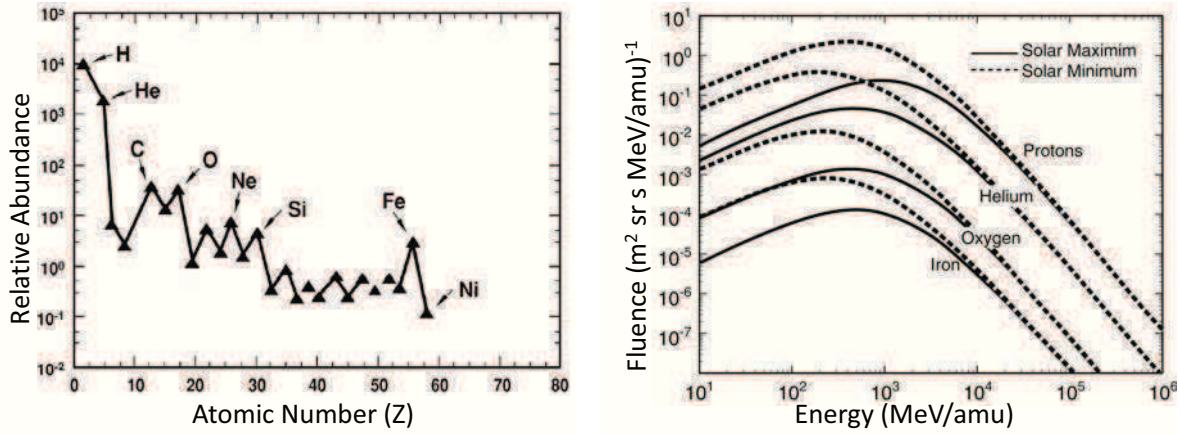

Figure 1.1: Galactic Cosmic Rays (a) composition as a function of atomic number and (b) energy spectra for protons, helium, oxygen and iron during solar maximum and solar minimum conditions (inspired from [28]).

Solar radiation

The Sun is both a source of radiation as well as a modulator of GCR flux, thus the understanding of the Sun's physics is extremely important. Numerous space programs have been launched in the last decades, like Solar & Heliospheric Observatory (SOHO) [30; 31] and Solar TErrestrial RElations Observatory (STEREO) [32], to explain and to measure solar space weather projects. Both were designed to study the internal structure of the Sun, its extensive outer atmosphere and the origin of the solar wind and Coronal Mass Ejection (CME). Currently, they are used as the main source of near-real time solar data for space weather prediction provided by NASA as web-based applications [33].

The Sun's activity is cyclic with a 11 year period: 7 year long period of solar maximum (high solar activity) and 4 years during solar minimum (low solar activity). Figure 1.2 illustrates the solar activity during

the last 50 years. By superposition of solar flux on GCR intensity, the Sun's influence is clearly evidenced: for a solar maximum, GCR fluxes are at minimum and for a minimum, GCR fluxes are at maximum [28]. This is caused by the above mentioned Sun's magnetic field and solar wind which during the solar maximum activity, significantly attenuate GCR flux resulting in the spectral shapes show in Figure 1.1(b) and GCR intensity in Figure 1.2. Solar wind is composed of protons with energies inferior to 100 keV, electrons with energies inferior to several keV and alpha particles [34].

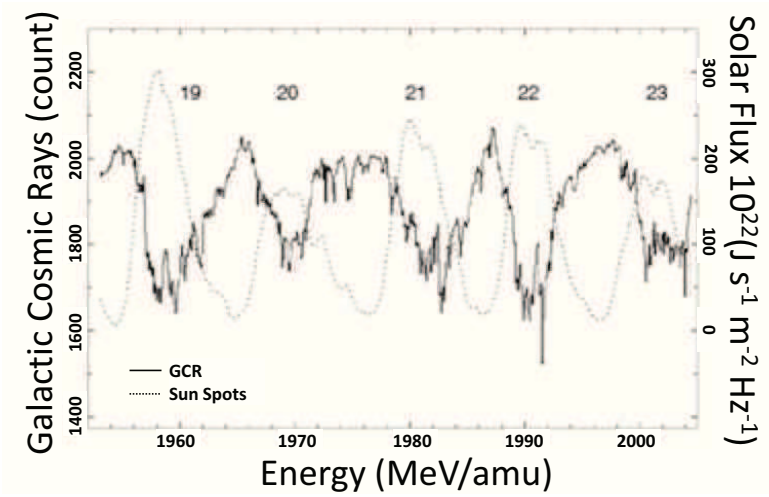

Figure 1.2: The observed record of yearly averaged solar activity indicator (dotted) compared to the GCR intensity (solid) between 1950 and 2005 - during the solar maximum, there is a minimum of GCR flux (inspired from [40]).

Besides the solar wind, there are two main types of solar particle events: solar flares and CME. The first ones are created when the localized energy storage in the coronal magnetic field becomes too important and is released ejecting mostly electrons. On the other hand, CME, is a large eruption of plasma and is composed of about 96% of protons 3.5% of alphas and about 0.1% of heavier ions with energies up to 1GeV [35]. CME can last from 12 hours to several days. Solar particle events are known to occur more frequently and with higher intensity during the declining phase of solar maximum [36]. Figure 1.3 presents very recent data obtained from the SOHO laboratory showing the largest solar flare ever recorded that was observed on the 7th of June 2011 [37].

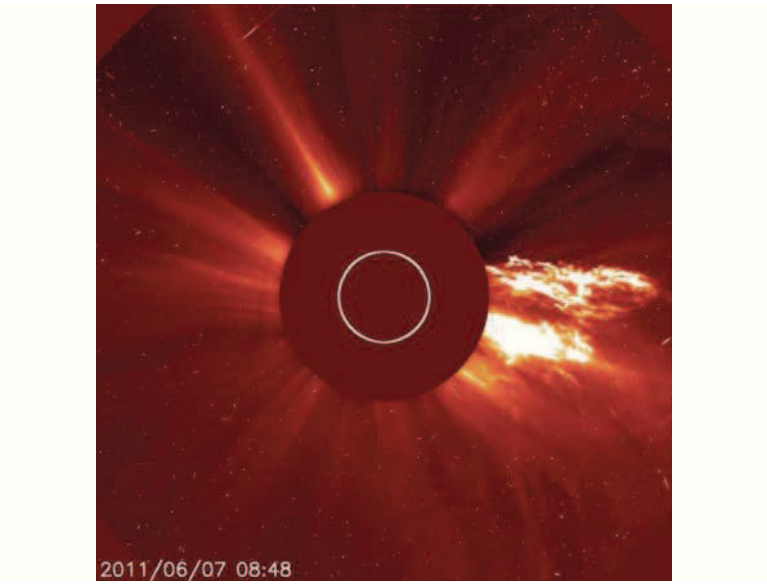

Figure 1.3: The largest solar flare ever recorded unleashed as observed by the SOHO satellite, on the June 7, 2011 (with authorization of NASA [37]).

Charged particles trapped in magnetosphere: Van Allen Belts, South Atlantic Anomaly

Earth's magnetosphere is capable of trapping certain types of charged particles with specific masses and energies and it can constrain their movement. As presented in Figure 1.4, the motion of a charged particle in this field is spiral following the magnetic lines. While approaching polar regions, the magnetic field strength increases, causes the spiral to tighten and eventually the field becomes sufficient to reflect the particle movement in the opposite direction. Additionally, there is a slower longitudinal drift of the path around the Earth that is westward for protons and eastward for electrons. The trapped particles form the inner and outer zone of Earth's Van Allen belts are shown in Figure 1.5.

Both intensity and extent of the outer zone are variable and changes as a function of time due to solar weather and interplanetary magnetic fields. The Earh's field is weaker for outer zone than for inner one leading to the shorter lifetimes of trapped particles. The outer zone extending to sin10 Earth radii is mostly composed of electrons (99%) with energies up to 10 MeV and average electron fluxes (>1 MeV) equal to $3 \cdot 10^6 cm^{-2} s^{-1}$, however the peak electron fluxes can vary by factor > 100x with geomagnetic and solar activity.

While flux variability characterizes the outer zone, the inner radiation belt composition and flux are very stable. The most important source of charged particles in the inner zone are the collisions between

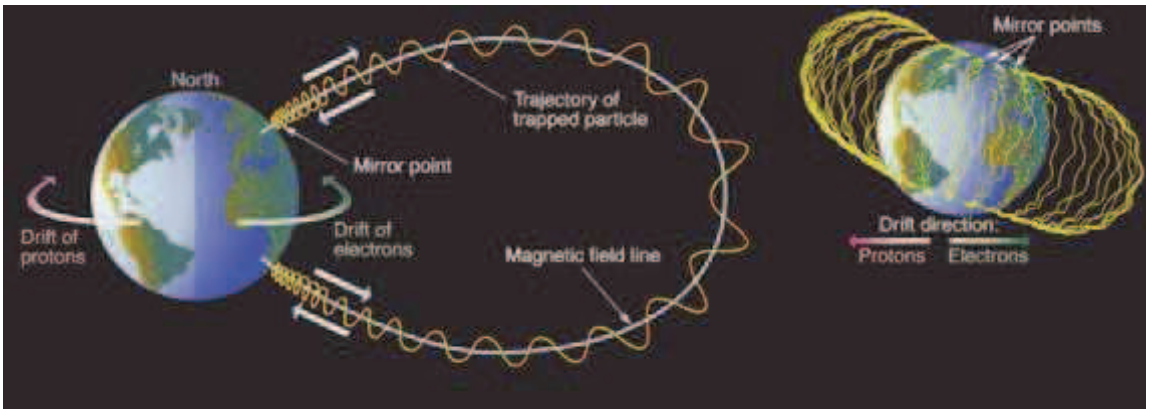

Figure 1.4: Trajectories of charged particles trapped by the Earth's magnetic field (with authorization of [42]).

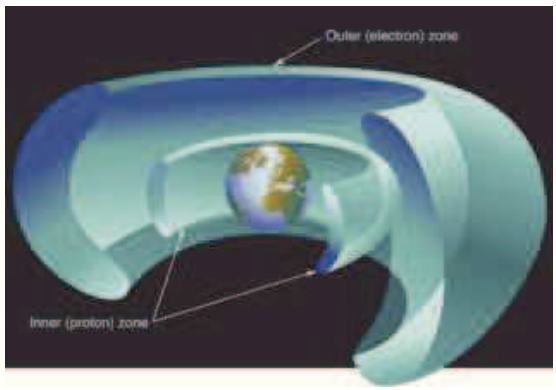

Figure 1.5: Diagram of the Earth's inner and outer Van Allen Belts (trapped particles by the Earth's magnetic field) (with authorization of [42]).

GCR and atoms of the atmosphere. This mechanism produces particle showers from which some of these produced particles are backscattered and are confined by the magnetic field explaining the composition which is mostly protons. The proton belts extend to sin3.5 Earth radii, energies of trapped protons range up to 100's of MeV with fluxes (>10MeV) up to about 10^5 cm^{-2} s^{-1}.

South Atlantic Anomaly

The Earth's magnetic dipole is offset from the geomagnetic center of the planet by about 11 degrees with respect to the North-South axis; this results in its displacement of more than 500km from the Earth's geographic center. This offset of the magnetic field and geometrical Earth poles causes weaker field in the region of South Atlantic Anomaly (SAA) and stronger field over northern part of Asia. As a result, it influences the movement of charged particles trapped in the inner zone of the Van Allen proton radiation belt. In the weaker magnetic field ar-

eas, the radiation belt penetrates deeper in the atmosphere going to lower altitudes (Figure 1.6 left) resulting in high proton fluxes even for altitudes far below 500km. Figure 1.6 right shows the collected data by SAMPEX satellite (NASA) orbiting on LEO for protons of energies superior to 0.7 MeV and electrons of energies superior to 0.5 MeV. The SAA is a potential threat for electronics embedded in satellites orbiting in altitudes between 100 and 1500 km in the region of south-est Brazil and South Atlantic ocean.

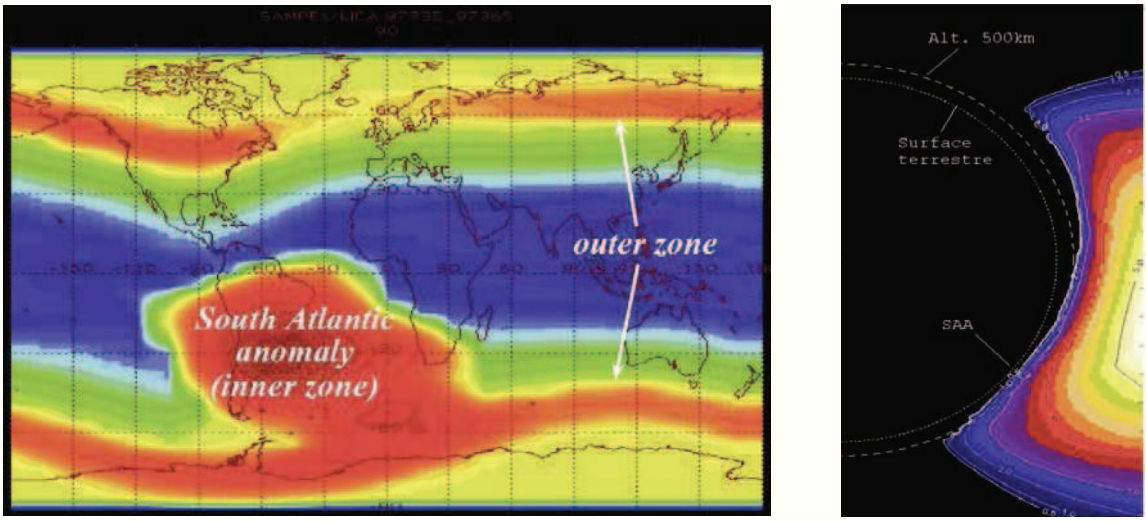

Figure 1.6: Left: Count rate (arbitrary units) of proton (>0.7 MeV) and electron (>0.5 MeV) fluxes as a function of latitude and longitude collected by the NASA SAMPEX satellite orbiting in LEO (inspired from [43]). Right: Proton fluxes from inner Van Allen radiation belt as a function of altitude .

Conclusions on space environment

This section describes different space radiation environments. Particle fluxes are compared in Figure 1.7 as a function of energy, flux and origin of the particles. To the most energetic ones belong GCR with relatively low fluxes of particles containing heavy ions, alpha particles and protons. Other highly energetic particles come from CME and inner radiation belts (trapped protons). The less energetic but with the highest fluxes are protons from solar flares and solar wind protons.

These particles influence behavior of electronics used in spacecraft or in satellites on different orbits. Typical satellite orbit trajectories and radiation Van Allen belts are shown in Figure 1.8: LEO stands for Low Earth Orbit, HEO for Highly Elliptical Orbit, GEO for Geostationary Orbit and MEO for Medium Earth Orbit. Table 1.1 summarizes all presented radiation sources, major orbits that are affected and the radiation effects that are induced.

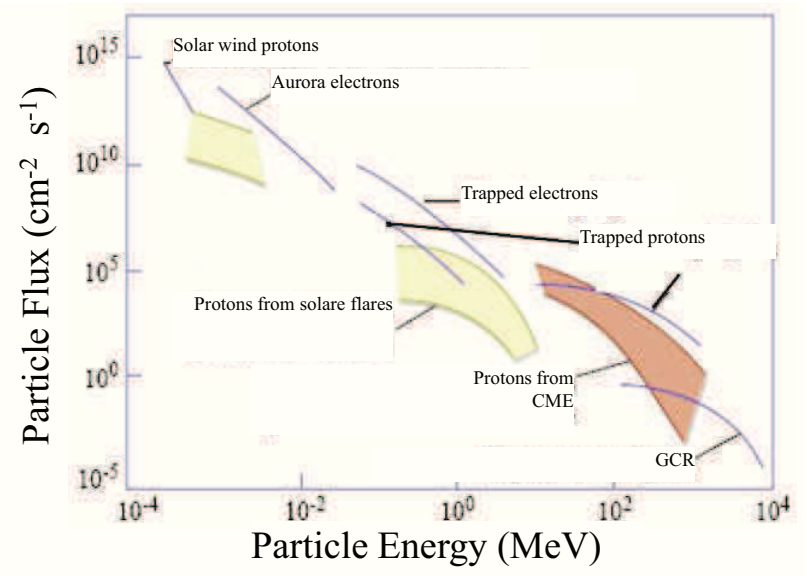

Figure 1.7: The summary of the particle fluxes present in space as a function of their energy and their origin (inspired from [40]).

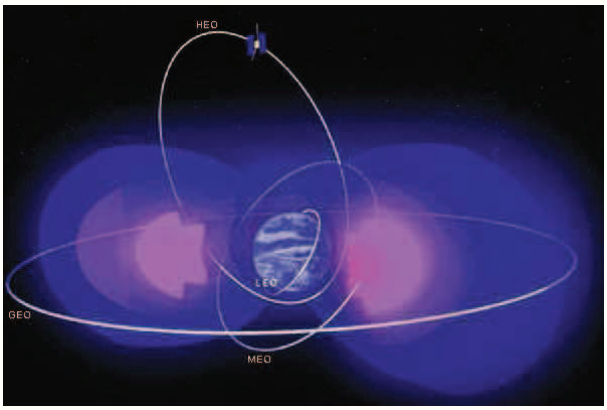

Figure 1.8: Typical satellite orbits and Van Allen belts (with authorization of [42]): Low Earth Orbit (LEO), Highly Elliptical Orbit (HEO), Geostationary Orbit (GEO), Medium Earth Orbit (MEO).

Radiation source	Types of orbit affected	Radiation Effects
GCR	LEO, GEO, HEO, Interplanetary	SEE
CME & Solar flares	LEO, GEO, HEO, Interplanetary	SEE, TID, DD
Trapped protons	LEO, HEO	SEE, TID, DD
Trapped electrons	LEO, GEO, HEO	TID, DD

Table 1.1: Summary of radiation sources, types of affected orbits and major radiation effects they provoke. Derived from [41; 44].

2.2 Terrestrial Environment

There are two primary radiation sources causing soft errors at ground level: atmospheric particles (mostly neutrons) that originate from GCR colliding with atmosphere atoms and alpha particles due to telluric radioactivity [38; 39].

Atmospheric environment due to cosmic rays

The energetic particles coming from outer-space can be deflected by Earth's magnetic field but a certain fraction, as it was shown previously, can be trapped by magnetic field in radiation belts and the most energetic ones (>1 GeV) coming especially from GCR traverse the magnetic field lines and can penetrate deeply in the atmosphere. Such incident particles lose their energy by colliding with the molecules of the atmosphere at altitudes below 50km and as a result of these collisions nuclear reactions can occur creating secondary particle showers containing protons, muons, pions, electrons, neutrons and different ions (Figure 1.9) with energies ranging up to 100 GeV. All these particles can potentially interact with matter.

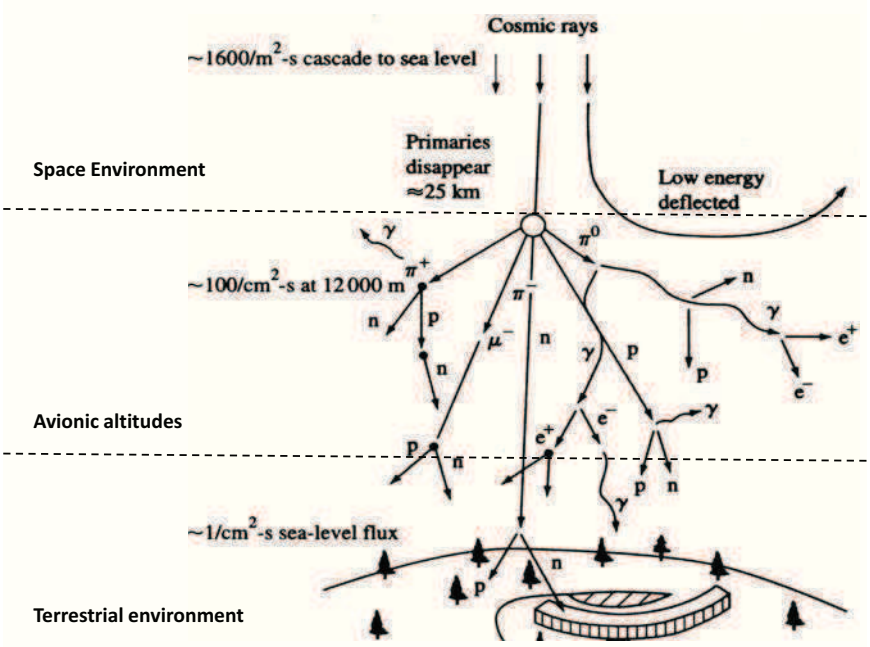

Figure 1.9: Illustration of the interactions between galactic cosmic rays and the atmosphere creating cascade of atmospheric particle showers (inspired from [45]).

The total flux of the major particles in the atmosphere as a function of altitude is presented in Figure 1.10 [46; 47]. Muons, whose flux at sea-level is the highest, weakly interact with matter and thus weakly

influence SER. However, the last publications show the increasing interest in muon-induced effects [48]. The flux of strongly interacting pions on the other hand is too small to be taken into account. From all types of particles, the most significant contribution to single event effects is that of the secondary neutrons that can penetrate easily the atmosphere and all possible matters because of the lack of electrical charge. Thus any shielding techniques become ineffective as far as neutron radiation as concerned. Moreover, while traversing the semiconductor, neutrons can interact with the crystalline structure causing the nuclear reactions and as a result, secondary particles which via ionization processes create the electron-hole pairs.

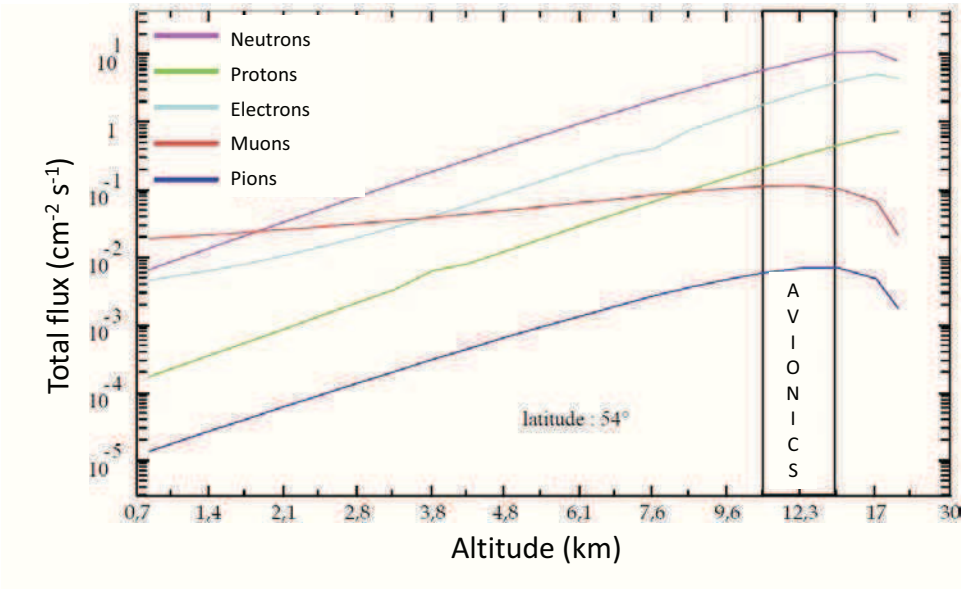

Figure 1.10: Particle fluxes in the Earth's atmosphere as a function of altitude (inspired from [47]).

The most commonly used metric for quantifying the neutron flux is the integral flux. For New York City, the neutron flux for an energy range between 1 MeV and 10 MeV is equal to $14.6 \cdot n \cdot cm^{-2} \cdot s^{-1}$ and $13 \cdot n \cdot cm^{-2} \cdot s^{-1}$ for energies above 10 MeV [12]. Because of the offset of Earth's magnetic dipole, the neutron flux varies for different latitudes and longitudes. The highest neutron fluxes are observed in the region of SAA, and the lowest in Asia. Table 1.2 summarizes relative cosmic-ray neutron fluxes at selected places relative to the reference flux measured at New York City.

Alpha particles due to radioactive decay of nuclei

The source of alpha particles are naturally occurring unstable atoms. An alpha particle is composed of four nucleons: two protons and two

City (Country)	Location: Latitude (°) / Longitude (°E) / Elevation (m)	Avg. Relative Neutron Flux (α h-1 cm-2)
New York (USA)	40.7N / 286.0 / 0	1.00
Los Angles (USA)	34.0N / 241.7 / 100	0.94
Paris (France)	48.9N / 2.3 / 50	0.98
La Paz (Bolivia)	16.5S / 291.9 / 4070	8.99
Bankok (Thailand)	13.4N / 100.3 / 20	0.52
Tokyo (Japan)	35.7N / 139.8 / 20	0.64
Pic de Bure (France)	44N / 5.9 / 2252	6.3

Table 1.2: Average relative neutron fluxes as a function of location for a few major cities and a Pic de Bure facility used in this study for experimental measurements (latitude, longitude, altitude)[12].

Atom	Half-life	Main alpha emissions
^{237}Np	2.1×10^{6} years	4.96 MeV
^{238}U	4.4×10^{9} years	4.196 MeV (77%), 4.147 MeV (23%)
^{235}U	7.0×10^{8} years	4.77 MeV (72%), 4.72 MeV (27%)
^{232}Th	1.4×10^{10} years	4.27 MeV

Table 1.3: Summary of the main alpha decay families characteristics.

neutrons, thus there are four families of alpha decay series: Neptunium (^{237}N), Thorium (^{234}Th), two Uranium isotopes (^{235}U and ^{238}U). The neptunium is extremely rare because of its short half-life time that is much shorter than the age of Earth. Table 1.3 summarizes the main characteristic of four alpha decay families.

Although all semiconductor materials are highly purified, the presence of alpha-particle emitter isotopes has been established in materials used in the chip package (such as solder balls or mold compounds) or directly integrated at circuit-level (silicon, metal interconnects, more recently hafnium in new high-k gate dielectrics or platinum in silicide layers [50; 51; 52]). Historically, alpha particles emitted by trace uranium and thorium impurities in packaging materials were identified as a cause of soft errors in DRAM devices in the late 1970s [49].

Alpha particle emission is independent of temperature, time, etc. Figure 1.11 presents the Uranium ^{238}U decay chain with alpha and beta emissions [54].The alpha emission energy is a discrete decay energy,

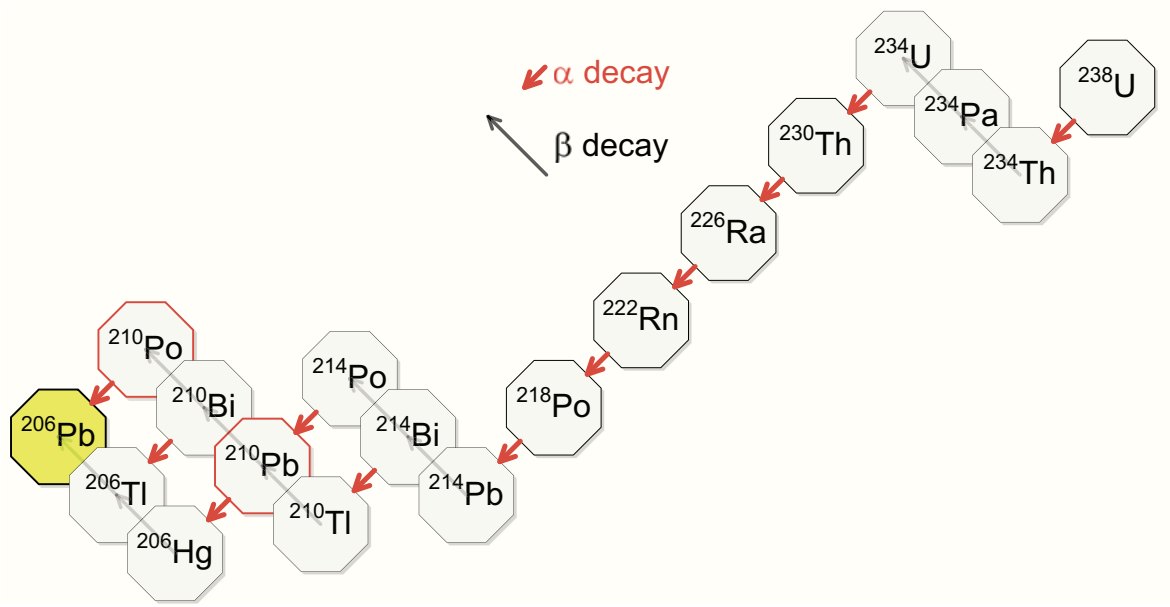

Figure 1.11: Schematic representation of the Uranium 238 decay chain showing the alpha (red arrows) and beta (black arrows) possible emissions (inspired from [54]).

unique to the emitting nucleus. The minimal and maximal alpha energy emitted from all radioactive isotopes are equal to 3.9 and 8.8 MeV that corresponds to the penetration range in silicon of 17.15 and 57.02 μm. Values have been calculated using Stopping and Range of Ions in Matter (SRIM) software [53]. Figure 1.12 presents the dominant alpha particle sources from the Uranium-238 and Thorium-232 decay series [55]. The dark blue lines represent the actual emission energies while the light blue regions represent the alpha particle spectrum emitted from a "thick" material such as the package (thick here is defined as a source material which is thicker than the maximum range of an alpha particle at the maximum emission energy).

In packaged semiconductor product, the sources of alpha emitting impurities can be found in packaging materials, silicon wafer materials and bounding structures. Table 1.4 reports alpha emissivities of major materials used for packaging and manufacturing of the silicon wafer [12].

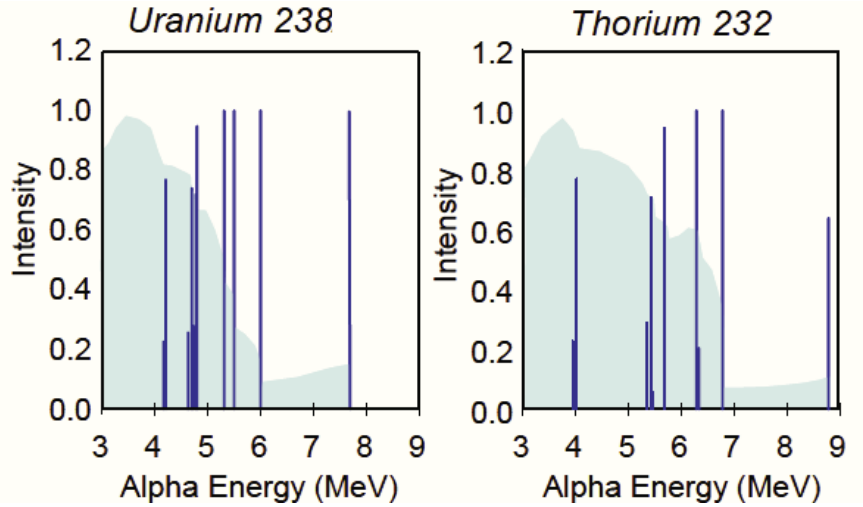

Figure 1.12: Dominant alpha particle emissions from the Uranium and Thorium decay series (inspired from [55]). The discrete lines show the actual alpha emission energies and the light blue regions show the alpha spectrum emitted from a thick material.

Material	AER ($\alpha\ h^{-1}\ cm^{-2}$)
Fully Processed Wafers (bulk)	$< 4 \times 10^{-4}$
30 µm thick Cu Metallization	$< 3 \times 10^{-4}$
20 µm thick AlCu Metallization	$< 3 \times 10^{-4}$
Mold compound	$5 \times 10^{-4} - 2.4 \times 10^{-2}$
Flip Chip Underfill	$7 \times 10^{-4} - 4 \times 10^{-3}$
Pb-based Solder Bumps	$9 \times 10^{-4} - 7.2 \times 10^{-0}$
Packaging	10^{-3}

Table 1.4: Emissivities of alpha particles for various materials used during the chip manufacturing and packaging (after [12]).

3 Single Event Mechanisms

3.1 Interaction of radiation in matter and charge generation

As discussed in the previous section, the primary particles of interest when studying Single Event Effects are neutrons, protons, alphas and heavy-ions. All radiation-induced errors are the result of ionization i.e. the interaction of incident ion with the target material atoms causing the generation of electron-hole pairs. Two ionization mechanisms can be distinguished: direct ionization produced by the primary charged particles or indirect ionization from secondary particles produced by reactions between the primary atom and the target nuclei (nuclear re-

Particle source	Particle type	Type of Interaction
GCR	p , α, HI	p – direct/indirect α, HI – direct
CME & Solar Flares	p, α, HI	p – direct/indirect α, HI – direct
Trapped protons	p	direct/indirect
Atmospheric neutrons	n	indirect
Telluric radioactivity	α	direct

Table 1.5: Summary of the particle types present in different radiation environments and the types of interactions while penetrating the solids.

actions).

Table 1.5 synthesizes all particles present for the different radiation environments described in the first section of this chapter with the interactions they cause when penetrating a semiconductor lattice. In the most general case heavy ions and alpha particles are directly ionizing and neutrons deposit charge by indirect ionization. Protons can deposit charge in both ways: by direct ionization especially for low energy protons around 1-2 MeV [56; 57; 58; 59] and by indirect ionization for higher proton energies.

Direct Ionization

Direct ionization is produced due to penetration of an electrically charged particle in matter. The incident ion's trajectory remains unchanged from its original direction with essentially no momentum transfer to atomic nuclei. As an ion passes through matter, it loses energy during each Coulomb interaction with the target crystalline structure. The effect of all interactions is to transfer the energy to the target matter creating electron-hole pairs (the energy needed to create a electron-hole pair in silicon is equal to 3.6eV) and to slow the ion down and, if the target is thick enough, eventually stop the particle within the target.

One key parameter used to characterize the penetration of charged particles is the average energy loss per unit path length (dE/dx), i.e., stopping power or stopping force. The radiation effect community commonly uses mass stopping force, called Linear Energy Transfer (LET), as the metric for average deposited energy per unit path length defined by the Equation 1.1:

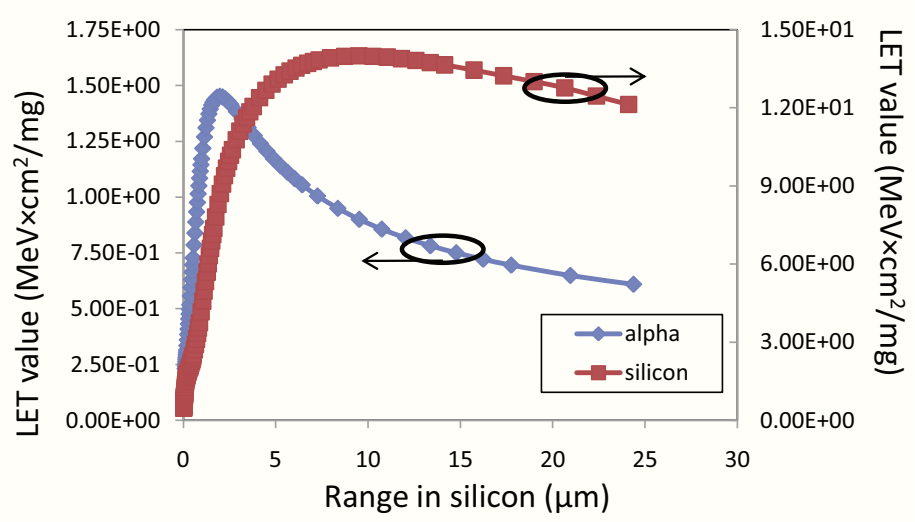

Table 1.6: LET value as a function of range in silicon for two particles: an alpha and a silicon atom simulated with SRIM software [53].

$$LET = -\frac{1}{\rho} \cdot \frac{dE}{dx} \tag{1.1}$$

where ρ is the density of the target material and the LET unit is typically expressed in $MeV \cdot cm^2 \cdot mg^{-1}$. When taking into account that silicon density is equal to $2.32g \cdot cm^3$ and energy needed to create an electron-hole pair we obtain the following relation:

$$1MeV \cdot cm^2 \cdot mg^{-1} = 10.3fC \cdot \mu m^{-1} = 0.23MeV \cdot \mu m^{-1} \tag{1.2}$$

Ion transport through matter is a complex mechanism and can be simulated using advanced codes employing Monte-Carlo techniques and detailed physical models like SRIM [53]. The particle LET depends on its atomic number but also on its energy. For all ions with a high initial kinetic energy and for all materials, while ion penetrates in the target, its energy decreases and its LET increases to maximum near the end of its range, then LET starts decreasing very rapidly. Figure 1.6 shows the SRIM simulation of alpha particle and silicon atom as a function of range in silicon. The peak in the stopping LET curve is known as the Bragg's peak. As it is illustrated in figure, the Bragg's peak is especially important for ions with low atomic mass (alpha, protons) since most of their energy is transferred while they stop and less visible for heavier particles.

Indirect Ionization

Energy may also be transferred into nuclear reactions for which the ion interacts with a single target nucleus. In this case nuclear forces

dominate the energy-loss process. From a radiation point of view, there are three nuclear reaction types: elastic collision, inellastic collision and fission.

- Elastic collision provokes the target atom movement by transferring the incident ion momentum that results in the target ejection from the crystalline structure and the reflection of the incident particle. This ejected atom movement causes the direct ionization of the lattice. Figure 1.13(a) illustrates an elastic reaction between a neutron and silicon atom.

- Inelastic collision or fission leads to the partial transfer of the incident particle kinetic energy and to the excitation and/or the break-up of the target nucleus. In contrast to an elastic collision, for inelastic collision and fission the kinetic energy is not conserved. The incident ion penetrates the target nucleus, a variety of particles are emitted including nucleons (protons and neutrons), photons, alpha particles (helium ions), and other heavier fragments (known as recoil nuclei). Excited states may later decay by gamma ray or other forms of radiative emission, or further break-ups. The recoiling nuclei and other fragments transport through the semiconductor, losing energy along the way via ionization.

  Figure 1.13(b) shows an example of a fission reaction from GEANT4 simulation. The initial neutron energy before the collision is equal to 132 MeV, the hit silicon atom recoils in sodium, helium and proton with energies ranging from 1.7 MeV for sodium to 76 MeV for proton.

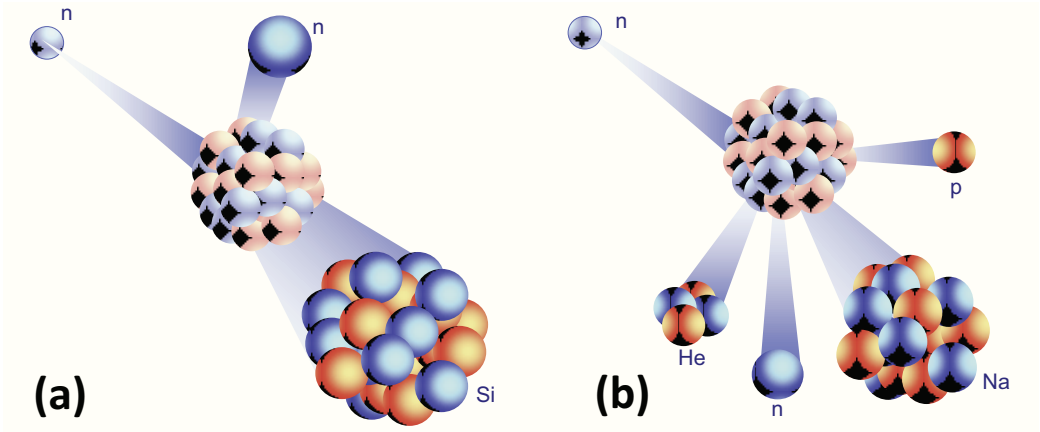

Figure 1.13: Examples of elastic (a) and inelasic nuclear reactions between a single incident neutron and a silicon atom (b) (artistic view). The presented reactions correspond to the reactions produced by GEANT4 simulation [61].

The secondary products from all above mentioned collisions become the energetic ions that while displacing in silicon will generate charge by direct ionization.

Ion Track Structure

In the past, the ion track structure has been considered as a second order effect [60]. For older technologies (> 250 nm CMOS), the generated spatial electron-hole pair distribution after an ion strike was small enough to cause only very local disturbance affecting one transistor. When CMOS technology is scaling down, one ion strike influences more and more transistors at the same time and the spatial distribution of charge is becoming an area of interest [63]. Figure 1.14 presents 3D TCAD simulations showing the heavy ion generated charge density impacting only one cell in a 130 nm technology while already 6 cells are impacted in 45 nm. The 3D e-h cloud size can be described by the variation of the carrier density radially from the track of the ion track and at a specific location along the track. This distribution will depend on the ion's stopping power, i.e., ion's energy and atomic number. It changes as the ion loses energy, that is, as the ion energy changes the radial distribution will change accordingly.

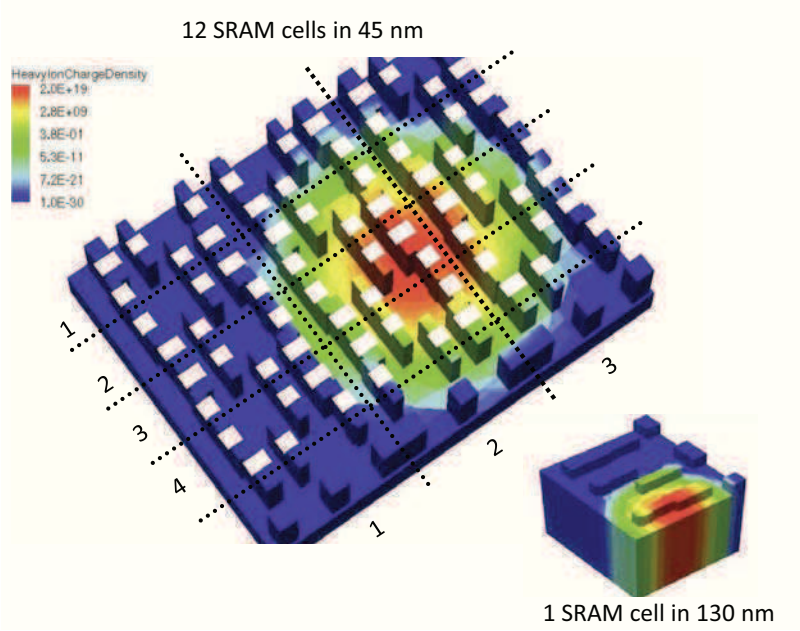

Figure 1.14: 3D TCAD simulations illustrating the impact of an ion with the same LET value in two different SRAM technologies (130 nm and 45 nm) (inspired from [62]).

Dedicated nuclear codes can be used to estimate the ion track structure. Figure 1.15 shows predictions from a computer code developed at STMicroelectronics for two ions with the same LET (11 $MeV \cdot cm^{-2} \cdot mg$)

but different charge distributions. The higher energy ion (Kr at 60 $MeV \cdot nuc^{-1}$) produces the wider spatial distribution of charge. The simulation platform developed in this study can be coupled with this code to take into account the real ion spatial charge distributions.

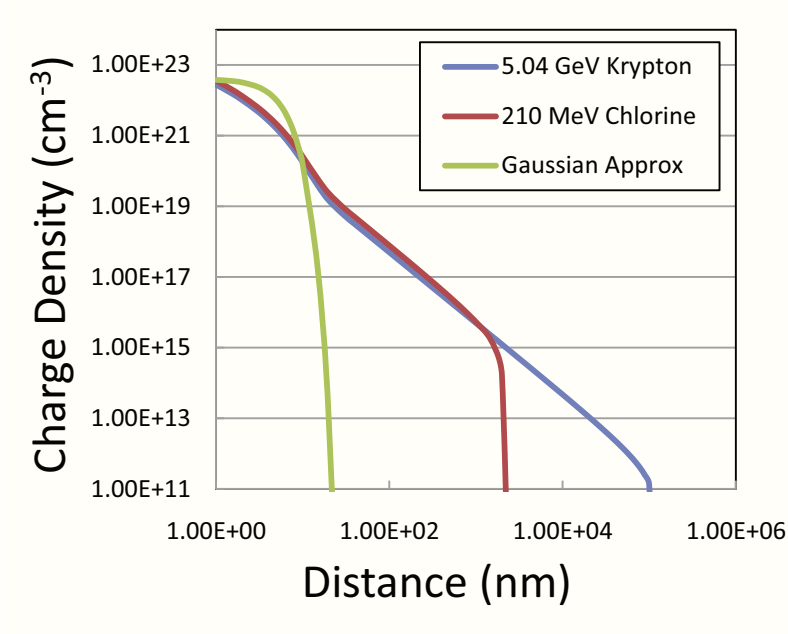

Figure 1.15: Average radial distribution of charge density for two ions with the same LET.

3.2 Charge transport and collection

An ionizing particle generates electron-hole pairs along its path as it passes through a semiconductor lattice, resulting in a charge distribution around the ion trajectory. This ion-induced charge can be collected by circuit junctions, especially reverse-biased transistor drain junctions that collect effectively this charge because of their high electric field. The collected charge by the junction induces a parasitic current on the contact of the junction and then in the circuit node connected to this junction.

TCAD simulation of an ion strike in a n+/p junction with the main charge transport mechanisms is shown in Figure 1.16 whereas typical current transient pulse created on the junction electrodes is shown in Figure 1.17. Its shape (i.e. magnitude and duration) is directly controlled by three main transport mechanisms:

- Charge drift occurring in the presence of the electric field in a semiconductor structure. This electric field is especially high in the Space Charge Region (SCR) of the reverse-biased junctions which

have deep depletion region widths and are the most susceptible areas to collect particle-induced charge. Due to the electric field of SCR, promptly after generation carriers (electrons and holes) are separated and are accelerated to high velocities resulting in extremely fast transient currents at the p-n junction electrodes.

- Field assisted funnelling mechanism was discovered by Hsieh et al. in 1981 [64; 65] and was attributed to the generation of high carrier concentration within or near the junction depletion region. This generation modulates the potential gradients and creates a field funnel. The electric field that was localized initially in the depletion region is distributed along the ion-track and is extended in the substrate, thus collecting promptly carriers deposited by an ion below space charge region of the junction.

  This fast collection of carriers due to electric field in the SCR and funnelling is shown in Figure 1.16(b) anc (c). The duration of the funnel creation and collection is approximately equal to several tens of picoseconds as shown in Figure 1.17

- Charge that is generated outside of the SCR and funnelling is subjected to ambipolar diffusion governed by charge concentration gradient. The diffusing carriers, that reach the depletion region of a junction, are collected by the underlying electric field. Diffusion is a slow transport mechanism that takes from hundreds of picoseconds to nanoseconds delaying the diffusion component of ion-induced current compared to drift component.

  On a longer time scale, collection is dominated by diffusion of excess carriers coming from deeper in the substrate (Figure 1.16(d)) that create the tail of the parasitic current pulse (Figure 1.17).

Concurrently, the recombination takes place which is an antagonist mechanism to charge collection. All diffusing excess carriers that do not reach the electric field will recombine after a certain period of time.

3.3 Circuit response - Single Event Upsets

The ion-induced parasitic currents in the circuit node influence circuit behaviour. The circuit responses can be very different depending on this parasitic current magnitude, duration and shape, circuit design and impacted node. In general, the responses can be destructive (hard error) or non-destructive (soft error). The classification of the SEE is presented in Appendix 1.

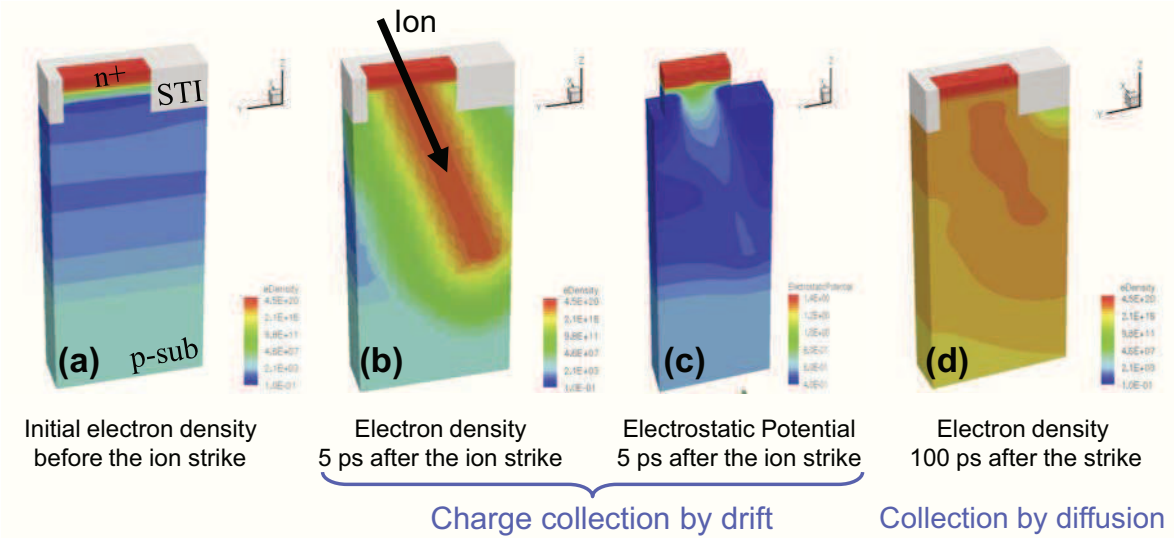

Figure 1.16: Simulation of an ion strike in a n+/p reverse-biased junction: initial electron charge density before ion strike in an off-state drain junction (a), electron density 5 ps after the ion strike (b), electrostatic potential 5 ps after the ion strike showing the junction space charge region and a funnelling phenomenon (c), electron density 100 ps after the ion strike.

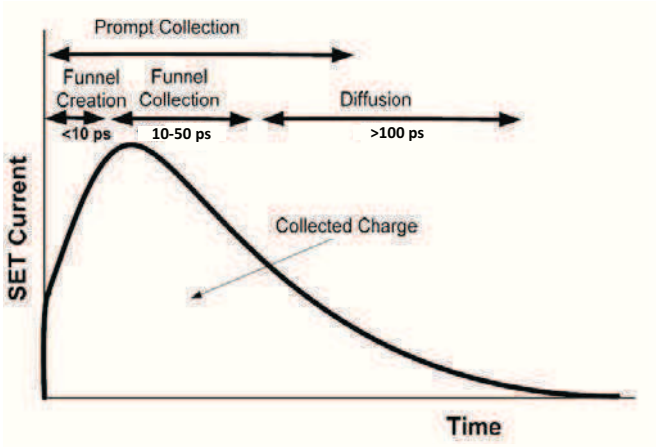

Figure 1.17: A typical ion-induced parasitic current in a reverse-biased transistor drain junction induced by ion strike (inspired from [66]).

A SRAM memory cell is used as an example of an SEU-sensitive component, however SEUs in both SRAMs and FFs are created through the same mechanisms. Figure 1.19(a) shows a schematic of an SRAM cell which is composed of cross-coupled inverters that store the logic state and act to provide stability to the logic state under noise or other perturbations and two access transistors allowing reading and writing mode. The SEU creation mechanisms due to a particle strike at one of the off-state transistor drains (called also sensitive nodes) are explained hereafter by Technology Computer-Aided Design (TCAD) simulation.

Figure 1.18 presents a 3D model of an SRAM cell created in a 65 nm CMOS technology calibrated with the STMicroelectronics low power manufacturing process using the Synopsys Sentaurus TCAD package. The top left picture shows 6 SRAM transistors (two pull-up PMOS transistors, two pull-down and two access NMOS transistors connected to one another by common drains) and well-ties biasing the silicon substrate and Nwell. The ion-strike simulation in the off-state NMOS transistor of the cell transient is carried out. Top right picture presents the heavy ion induced charge generated during ion impact. Two bottom pictures present electron densities 10ps and 500ps after the ion impact, respectively. For the first time instance (10ps after the ion-strike), the field-assisted charge collection occurs and the funnel is formed. For the second time instance (500ps after the ion-strike), the ion-induced excess carriers are present in the whole substrate, they diffuse and after reaching the space charge region of the reverse-biased junction, they are collected by the electrode.

The ion-induced parasitic current pulse (that was simulated by TCAD) is created on the same drain of the "off" NMOS transistor of the inverter whose input is in the ’1’ state and whose output is in the ’0’ state (Figure 1.19). The "on" PMOS transistor sources current in an attempt to balance this parasitic current. However, the restoring transistor has only a limited amount of current drive and a finite channel conductance. The current flow, therefore, induces a voltage transient at the drain of the restoring transistor and finally of the BLF node. This voltage transient is actually the mechanism that can cause an upset in an SRAM cell.

SEU occurrence depend on the magnitude and duration of the parasitic current. On one hand, for prompt ion currents, the nodal capacitance limits its magnitude and the SEU occurence. However, if this magnitude is high enough, the PMOS transistor is not capable of responding quickly enough and a bit-flip may occur. On the other hand, for long ion currents, if the PMOS transistor’s drive current is not sufficient to balance the ion current a bit-flip may occur.

Figure 1.19(b) shows a SRAM cell response to the ion-induced current and the impact of this current on the stored voltage at that node. As seen, the particle LET exceeds LET threshold, both inverters switch, resulting in a reversal of the stored information in the bit. This provokes a single-event upset. The minimum charge associated with the integrated single-event current at a critical node that can cause an upset is referred to as the critical charge.

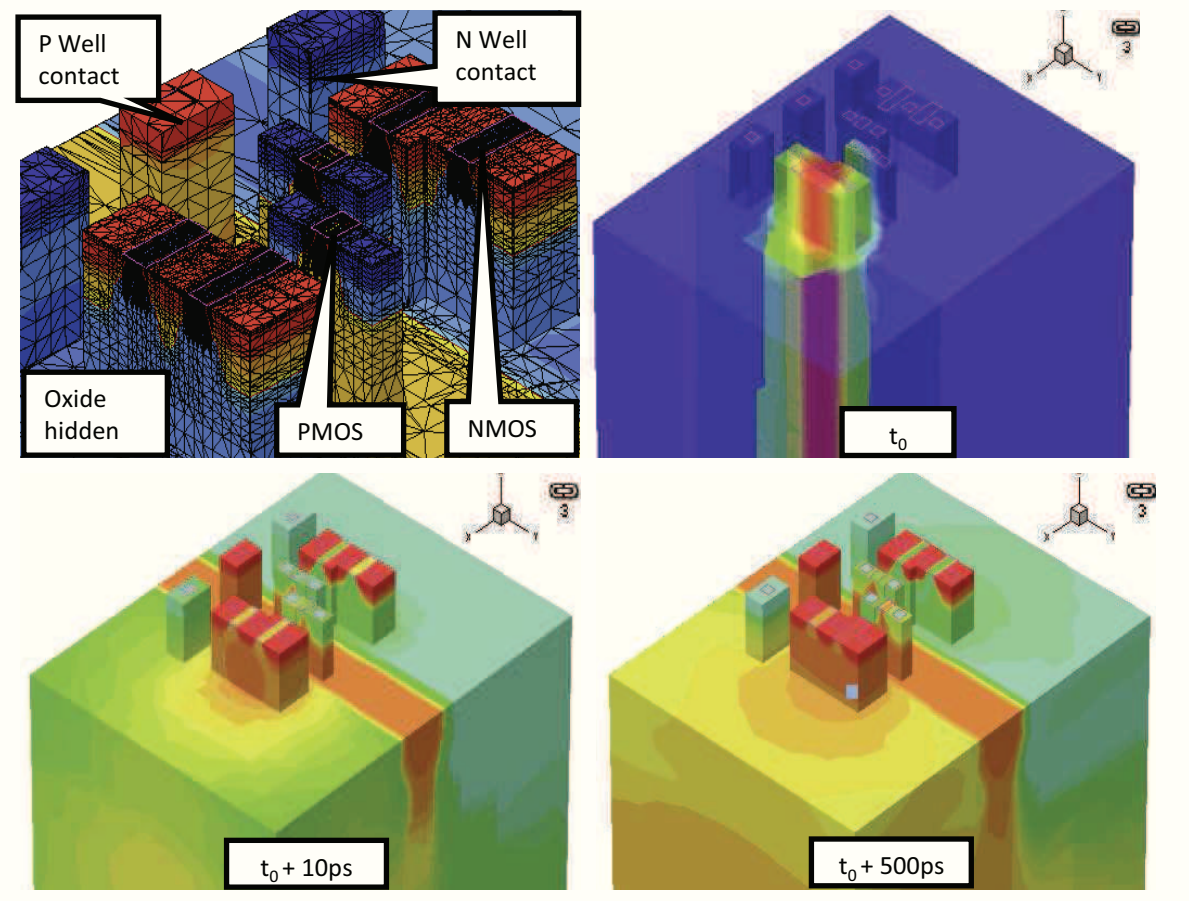

Figure 1.18: 3D TCAD model of a SRAM cell and ion-strike transient simulation: (top left) shows the doping profiles and mesh structure, (top rgiht) shows the generation of charge by penetrating ion, bottom figures show the electron density and main collection mechanisms 10ps and 500ps after the ion strike.

4 Radiation characterization of circuit sensitivity

Circuit reliability is the ability to perform the required function under stated conditions for a specified period of time. The reliability with respect to radiation is the capacity of a circuit to not exceed specified error rate in its given environment (temperature, altitude, supply voltage, etc.) It is necessary to quantify this failure rate to assure the device functionality requirement thus different testing and modeling strategies are developed. Figure 1.20 illustrates the SEU/SER characterization approach used by STMicroelectronics that is taken into account from the technology development phase through prototyping to qualification of a final product. All characterization methods commonly used in semiconductor industry for technology qualification are depicted.

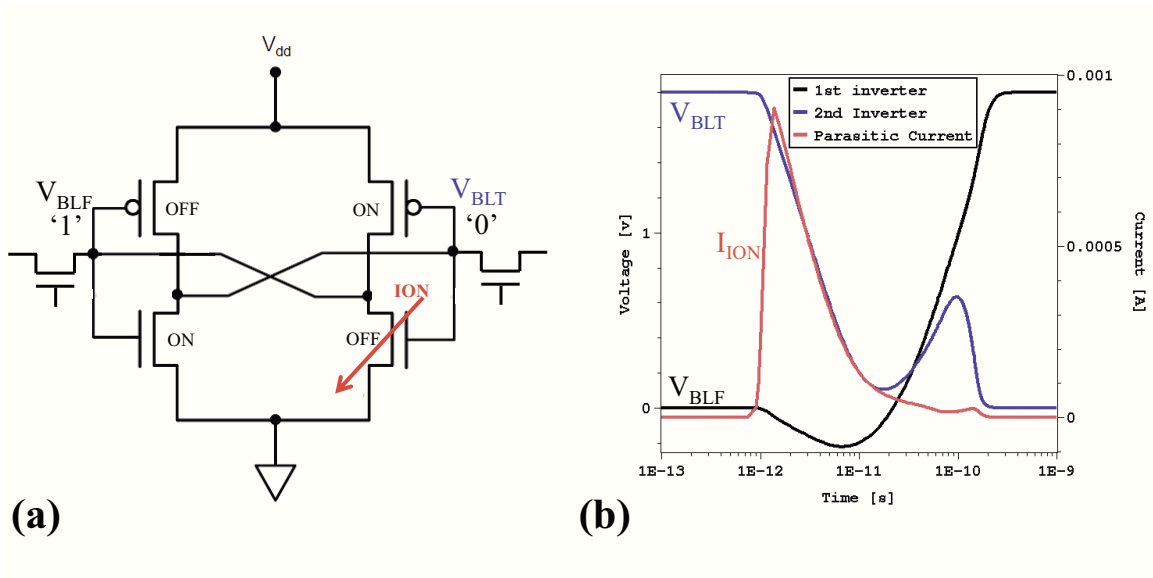

Figure 1.19: (a) Schematic diagram of cross-coupled inverters in a 6-transistor CMOS SRAM. A particle strike at one storage node can cause a change in the node's stored voltage state, which can propagate to the other node, upsetting the cell. (b) Diagram of simulated node voltage in a CMOS SRAM cell after a particle strike. If the incident particle LET exceeds the cell's LET threshold, the cell changes state.

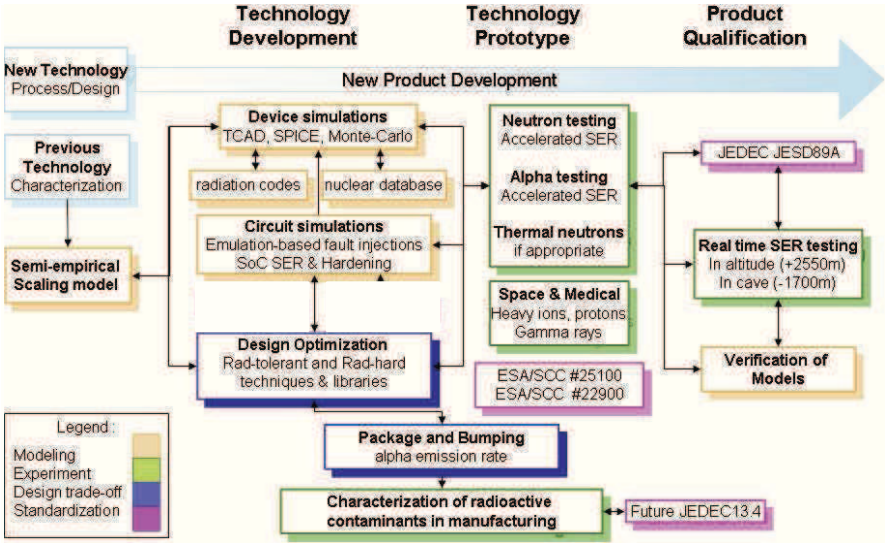

Figure 1.20: The ST flow used for radiation technology qualification illustrating modeling, testing, hardening and standardization methods [67].

- From the characterization of previous technologies, semi-empirical analytical models are extracted and allow the early SER assessment. Models are based on scaling of technological parameters (as doping profiles and transport of carriers in a semiconductor lattice). This information enables first order qualitative radiation assessments when compared to previous technological nodes. At

the same time, use of new materials during the manufacturing process is evaluated radiation-wise in order to anticipate new failure modes or sudden decrease in reliability.

- With technology development, more precise data are available (technology doping profiles, transistor SPICE models, silicon electrical measurements, etc.) that are used in the existing simulation tools. Additionally, during the design stage, the simulation tools are used to emulate device in real environment in order to find design weaknesses, propose the best-adapted hardening solutions to optimize design for a given application.

- Small samples availability (characteristic to prototyping phase) allows performing the accelerated radiation tests. Test vehicles are manufactured and packaged and tested with alphas, neutrons, heavy ions, protons or gammas as a function of the technology requirements. The experimental measurement results are then compared with simulation estimations for the purpose of adjusting the prediction models.

- Large samples availability (characteristic to qualification phase) leads to Real Time (RT) SER experiments. The purpose of real time tests is to compare the accelerated measurements on the same test circuits and confirm the validity of all accelerated testings.

The different standardizations are shown in Figure 1.20 to which belong ESA and JEDEC norms. The JEDEC Solid State Technology Association, formerly known as the Joint Electron Devices Engineering Council, is an independent semiconductor trade organization sponsored by Electronic Industries Alliance (EIA) regrouping the majority of semiconductor manufacturers. It was founded to develop standards for semiconductor devices. The JEDEC JESD89A [12] and JESD57 [13] norms focus on the measurement and reporting of alpha particle and terrestrial comsmic-ray-induced soft errors in semiconductor devices and test procedures for the measurement of single event effects in semiconductor devices from heavy ion irradiation respectively and are widely used permitting all foundries to manufacture in compliance with adopted standards and to compare products between each other.

The following two sections of this chapter focus on the real time and accelerated experimental characterizations that are performed strict compliance with presented norms. Then, the extensive analysis of major the-state-of-the-art modeling tools developed by different companies and research centres are presented.

5 Experimental characterizations

This part briefly presents the experimental radiation characterizations where test results reported in this thesis were collected. First, the real time and second, the accelerated experiments are presented.

5.1 Real Time Experimental characterizations

The real time (or unaccelerated) SER measurements consist in testing the large sample of devices for a certain period of time until enough soft errors have been accumulated to give a confident estimate of the SER. The particle acceleration is not used and has to be compensated by large number of tested devices and/or long exposure. The advantage of RT tests is direct measurement of actual SER requiring no intense radiation sources and extrapolation of measurement results to real conditions.

There are two types of real time SER tests that can be performed

- Atmospheric neutrons experiments at high altitudes where the neutron flux is higher.
- The alpha real time experiments are carried out in caves where the rock shields atmospheric neutrons and errors are only induced by silicon wafer and packaging contaminations.

In order to perform real-time characterizations of circuit in natural environments, STMicroelectronics uses two installed complementary test platforms, the first one at high altitude on the Plateau de Bure (French south Alps) and the second one inside the underground laboratory of Modane. In the following, these two test platforms are briefly presented together with their background radiation environments. The extensive long duration real time tests in both facilities have been performed on 130nm and 65nm ST SRAM memories.

Altitude laboratory - example of the Plateau de Bure facility

Altitude SEE Test European Platform (ASTEP) is a permanent installation and a dual academic research/R&D platform founded by STMicroelectronics, JB R&D and L2MP-CNRS in 2004 [68]. The platform is referenced as a research location in the international JEDEC standard JESD89A [12] and is currently operated by IM2NP and has been fully operational since March 2006. ASTEP is located in the French Alps on the desert Plateau de Bure (Devoluy Mountains) at 2552m (Latitude North 44° 38’ 02”, Longitude East 5° 54’ 26”), in a low electromagnetic noise environment. From a geomagnetic point-of-view, the ASTEP site is characterized by

the natural neutron flux approximately 6 times higher that the reference flux measured at New-York City. This value (called "acceleration factor" with respect to the gain that can be expected on the duration of real-time experiments performed in altitude instead of at sea-level) has been precisely measured in 2008 [69]. The platform hosts a neutron monitor that during the installation was used to experimentally determine the Acceleration Factor (AF) of the ASTEP location with respect to sea-level. With strictly the same setup, two series of data were thus recorded in Marseille and on the Plateau de Bure: the difference between the counting rates and barometric coefficients for the two locations allowed us to directly evaluate the acceleration factor of ASTEP with respect to Marseille location, here estimated to 6.7 [70]. Taking into account latitude, longitude and altitude corrections for Marseille location with respect to New-York City (the reference place in the world for standardization purposes), the final value of the acceleration factor is AF = 6.7·0.94 ≈ 6.3. Real-time measurements have been performed on bulk SRAMs fabricated by STMicroelectronics using commercial CMOS processes in 130 nm (200 mm wafers) and 65 nm (300 mm wafers) technologies.

Underground test laboratory - example of Modane facility

The test platform in the Laboratoire Souterrain de Modane / Underground Laboratory of Modane (LSM) was developed in order to obtain complementary measurements for separating the contribution to SER of atmospheric particles from the one due to natural alpha-particle emitters [**?**]. This laboratory is located about 1700m under the top of the Fréjus mountain (4800 meters water equivalent), near the middle of the Fréjus highway tunnel connecting France and Italy [71]. It was created in 1983 in order to conduct particle physics and astrophysics experiments in a strongly reduced cosmic ray background environment. Due to the depth of the LSM, the average particle flux inside the laboratory is extremely reduced [72]: about 4 $muons \cdot m^{-2} \cdot day^{-1}$; a few 10^3 fast $neutrons \cdot m^{-2} \cdot day^{-1}$ (depending on the neutron energy and the measurement location in the laboratory) emitted by natural radioactivity from the rock, the neutron component of cosmic rays being totally eliminated at this depth. In addition, the Radon in the laboratory is maintained at a very low rate of ≈ 20 $Bq \cdot m^{-3}$ owing to an air purification system which totally renews the volume of the air inside the laboratory twice an hour. With a very high confidence level, all events detected at LSM during the SER real time experiments are induced by internal chip radioactivity (alpha-particle emitters) and not by the external neutron background.

5.2 Accelerated tests

The ground-based accelerated experiments involve tests at different radiation facilities, i.e. for neutron, heavy-ions and proton, or tests with radioactive sources, i.e. alpha tests. These experiments are highly accelerated from flux point of view which provides an obvious advantage of quickly gathering information to predict the error rate over the life of an IC operating in a radiation environment. The acceleration is possible because the ageing/circuit characteristics change is negligible and radiation events are time independent. On the other hand, despite short test run times, such a method required the data extrapolation in order to predict component sensitivity in a real environment. The characterization of a component for terrestrial environment [12] lists the neutron sources that allows reproducing atmospheric neutron spectrum (LANSCE [74], TRIUMF [75], ANITA [76], etc.) and standardizes alpha experiments using Americium and Thorium radioactive sources. The qualification of a component for space application necessitates additional tests with heavy-ions that can be performed at RADEF [79], HIF [73], Lawrence Berkeley National Laboratory (LBNL) [78], etc.

Neutron Particle Accelerators

Terrestrial neutron at a highly accelerated rate can be performed with the mono-energetic neutron, mono-energetic proton or spallation neutron sources. The most common approach is to use spallation sources providing neutrons over a wide range of energies with a spectrum similar to the terrestrial neutron environment. Figure 4.17 shows the natural terrestrial neutron flux as a function of energy compared to the neutron spectra produced in both LANSCE and TRIUMF radiation facilities. The beam flux is many orders higher that the flux at ground level, ex. 1h in the LANSCE beam corresponds to the $1.5 \cdot 10^4$ years at sea-level. Figure 1.22 presents a sketch of a neutron irradiation facility (TRIUMF). The neutron beam is produced from primary proton beam via spallation reactions on aluminium target [75].

The error cross-section is computed by dividing the number of observed upsets by the particle fluence during the experiment and by number of tested devices according to formula Equation 2.15. Then, the SER (New York City) can be derived by multiplication of the cross-section by integral neutron flux (13 $neutron \cdot cm^{-2} \cdot s^{-1}$ for neutron energies between above 10 MeV).

Radioactive Alpha Source Experiments

The alpha irradiations are performed at STMicroelectronics in Crolles using the americium alpha source and a special industrial tester de-

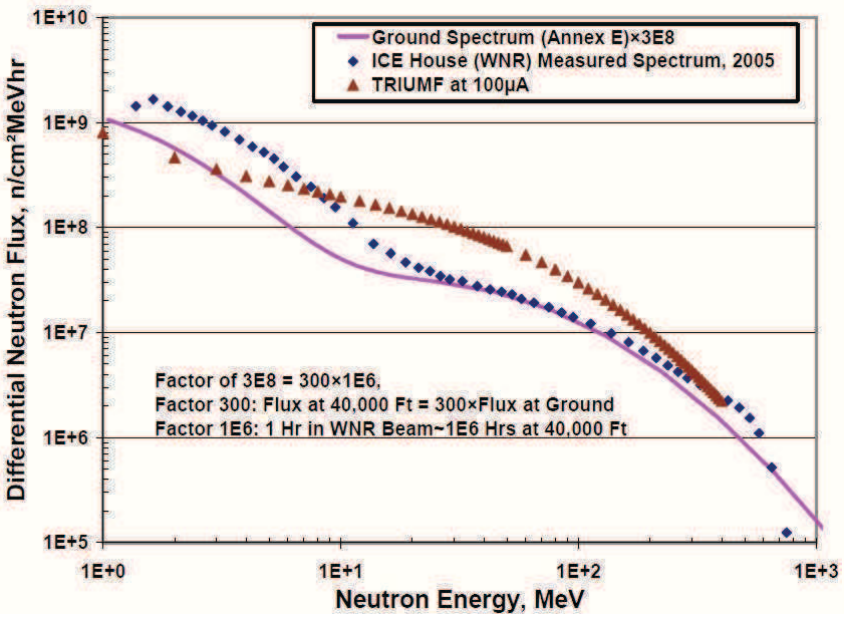

Figure 1.21: Terrestrial neutron spectrum measured in New York City compared to LANSCE and TRIUMF neutron spectra used fo experimental characterizations of IC.

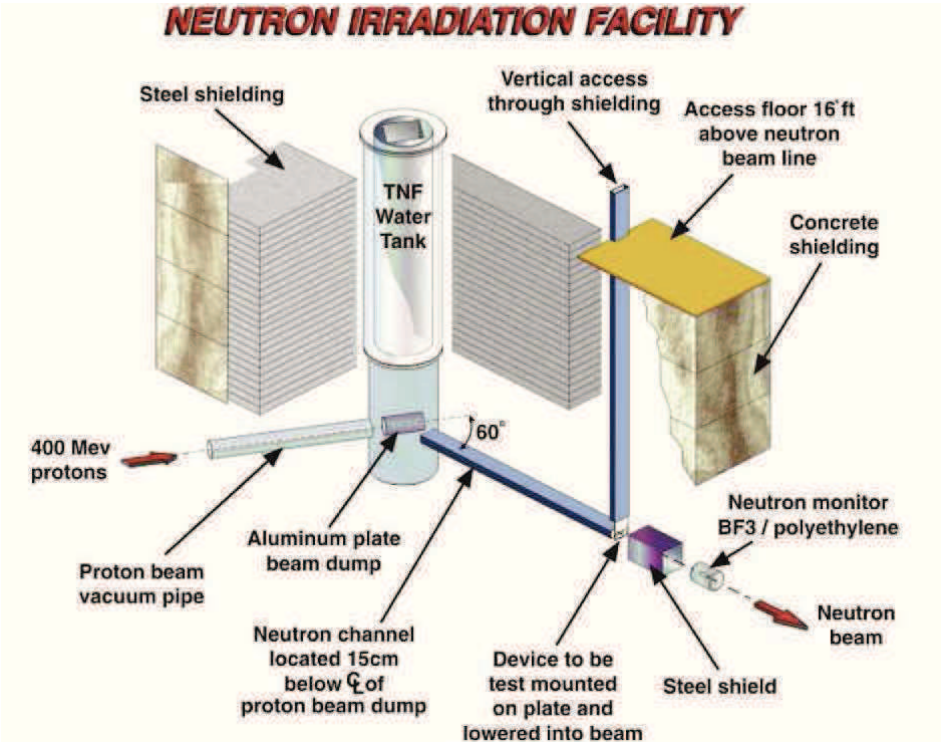

Figure 1.22: TRIUMF Neutron beam line [75].

signed for alpha experiments. The alpha source is made of americium (^{241}Am) isotope whose activity is equal to 3.7 MBq. Its active diameter is equal to 11 mm, source is encapsulated and placed above the die

area. The experimental alpha flux measured for a distance of 1 mm of a source is equal to $1.69 \cdot 10^6 \alpha \cdot cm^{-2} \cdot s^{-1}$. Unlike accelerated neutron and heavy-ion testings, for alpha experiments, the IC package has to be open to make possible the direct exposure (Figure 1.23) and the air gap between die area and alpha source has to be taken into account [77]. The source is placed above silicon surface with a distance of about 1 mm. The geometry factor [77] is precisely computed with a simulation model of the source using all mechanical information. Acceleration factor is the ratio between the alpha particle source flux and the packaged component alpha flux and varies between 10^5 to 10^{14}. Unaccelerated alpha particle SER can be calculated using the following formula [12]:

$$alphaSER = \frac{(\phi_{pkg}) \cdot (F_{geopkg})}{(\phi_{DUT}) \cdot (F_{geoDUT})} \cdot ASER \tag{1.3}$$

where ASER is the soft error rate obtained from the DUT during accelerated testing (number of errors for a given number of alpha particle events), ϕ_{pkg} is the alpha particle flux reaching the actual production component ($\alpha cm^{-2}h^{-1}$), F_{geopkg} is the geometry factor associated with the production component, ϕ_{DUT} is the alpha particle flux reaching the DUT during the experiment (normalized to ($\alpha cm^{-2}h^{-1}$)) and F_{geoDUT} is is the geometry factor during the experiment (defined by source-to-die spacing and source and die sizes).

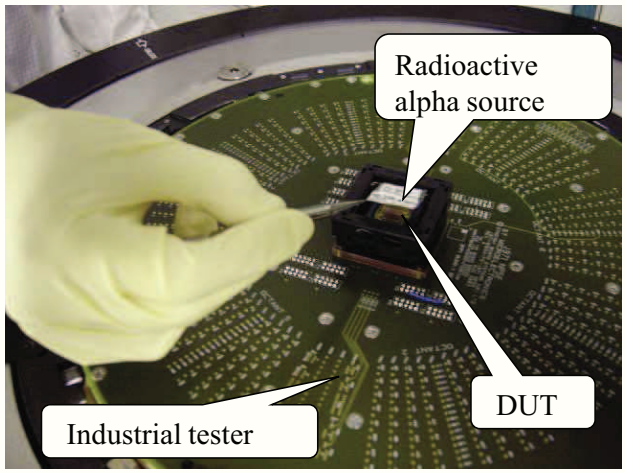

Figure 1.23: Radioactive alpha source (americium 241) placed on the tested IC. Industrial tester can be used to perform alpha experiments or dedicated test hardware can be used.

Experiments at Heavy-ion Radiation Facilities

The heavy ion experiments are performed at radiation facilities where the particles are accelerated to high energies. The experimental heavy ion results in this study were obtained from RADEF particle accelerator

located at the university of Jyväskylä, Finland [79]. In the contrary to the proton irradiations that are done in air, heavy ions are carried out in a vacuum chamber (Figure 1.24). Device Under Test (DUT) position can be changed in X, Y, Z directions and tilting is possible. The species used for these experiments include Nitrogen, Neon, Argon, Krypton, and Xeon with energies from 140 MeV to over 1.2 GeV. The ions easily penetrate the chip package and the chip thus ionizing the semiconductor substrate. Typical LET values for the ion coctails in radiation facilities range between several $MeV \cdot cm^2 \cdot mg^{-1}$ to several tens of $MeV \cdot cm^2 \cdot mg^{-1}$. To increase the resolutions of the test as a function of LET value, the beam is tilted in the repect to the DUT surface. For the same silicon die depth, the tilted ions deposit more important charge in the vicinity of transistor junctions according to Equation 1.4.

$$LET_{eff} = \frac{LET}{cos(\Theta)} \tag{1.4}$$

where Θ is the tilt angle of the beam in respect to the normal incidence.

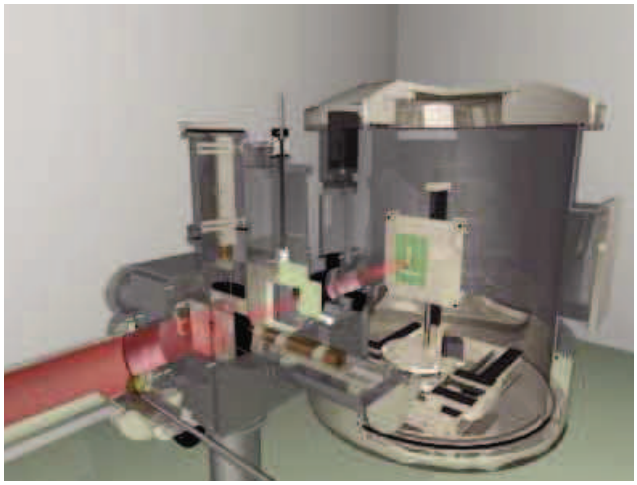

Figure 1.24: Heavy ion irradiation chamber installed at university of Jyväskylä, Finland. The linear movement apparatus allows position and tilting adjustments.

6 SEE Modeling approaches

Real time and accelerated experiments are necessary for quantification of a device/component's reliability. However, testings are possible late in the technology development after test chip manufacturing and require high costs and does not offer detailed explanation of ionizing radiation effects on a device level.

Already, back in 1967 at the Nuclear and Space Radiation Conference, the pioneering works on simulation were identified as complementary insight into radiation effects [80; 81]. Ever since, the simulation approaches have become an additional understanding of the physical mechanisms leading to the experimentally observed effects. Moreover, modeling allows for early radiation sensitivity assessment during the design process, early validation of hardening techniques thereby lowering development costs. Accurate and reliable modeling is an integral component of today's design procedure.

These advantages have lead to numerous simulation approaches that are proposed in the literature to assess SEE in electronic circuits. They can be classified in two main groups: physics-based methods which use the device simulation to obtain the ion-induced disturbance [82; 83; 84] and the methods based on analytical formulas and compact models to estimate the collected charge or collected current pulse [85; 87; 88].

6.1 TCAD-based

Technology Computer-Aided Design tools allow for the modeling of manufacturing process and device performance and have been used for many years in the semiconductor industry. Their capabilities include simulating manufacturing process steps as etch, deposition or lithography to predict the device doping profiles as well as electrical device operating conditions by solving the semiconductor transport equations for carriers together with electrostatics.

Full 3D TCAD

TCAD tools are also known for their capacity of simulating SEU effects. Sentautus Synopsys TCAD tools [89] implement special heavy ion/alpha models that define the charge generation using spacial charge distribution along the ion track and charge distribution as a function of time. State-of-the-art tools, thanks to the increase of computer performance in the last years, are capable also of creating models in 3 dimensions (3D) and simulating transient effects in a transistor or even a small circuits composed of several transistors. TCAD device models are numerical approximations on the time and space grids that control the convergence/CPU trade-off. On one hand, it is desirable to keep the grid dense to get the convergence and decrease the approximation errors, on the other had, however, the more mesh elements in the structure, the longer the simulation. Consequently, the TCAD tools are primarily used for conceptual understanding of the physical effects and as of today, full TCAD upset rate simulations has not been reported due to the

computational burden rendering the simulation time of a large numbers of particle strikes unreasonable .

Mixed-mode TCAD

The mixed-mode TCAD simulations consist of combining TCAD and circuit simulation for more complex circuits that cannot be modeled in one contiguous 3D domain or full 3D TCAD simulation is very long. To speed-up the simulation, parts of the structure that do not participate in charge collection use compact models while the transport processes in impacted devices are modeled as device. The example of mixed-mode set-up is shown in Figure 1.25. In this example, a NPN is modeled as a device while the rest using a circuit schematic and simulated with TCAD-coupled circuit engine (ex. SPICE). A major advantage of using mixed-mode is the ability to directly compute the voltage and current transients induced in the struck device by a given particle strike. Moreover, the CPU time is reduced thanks to partial use of compact models. In [84], the authors present the fully-coupled mixed-mode device physics simulations using the NanoTCAD 3-D code and Cadence Spectre SPICE solver. In the case study, the inverter chain contains eight stages and one struck NMOS transistor of the first stage is modeled in 3D. A potential drawback of the mixed-level method is that coupling effects between adjacent transistors have been shown to exist at the device level using 3D simulations [91; 92; 93]. These effects cannot be taken into account when only one struck device, is modeled at the device level. In order to consider multiple node charge generation in mixed-level simulation, more than one device needs to be simulated as device model. As inter-device spacing decreases with increasing integration levels, coupling effects can be expected to become more important, and other approaches are necessary. Moreover, although the more complex circuits can be treated with mixed-mode approach than with full 3D TCAD, the simulation runtime is still long and the device upset rate simulation methodologies have not yet been reported using this approach.

Upset rate simulation based on TCAD-extracted database

An interesting simulation approach using the TCAD simulation results has been proposed by iRoC Technologies which developed an empirical model, entirely based on a set of 3D mixed-mode simulation performed only on one basic CMOS inverter [90]. The ion strikes on the off-state NMOS or PMOS transistors are simulated as a function of ion strike position and LET and parasitic current are stored in a database. Based on this database, the Monte-Carlo method is used to predict the soft error

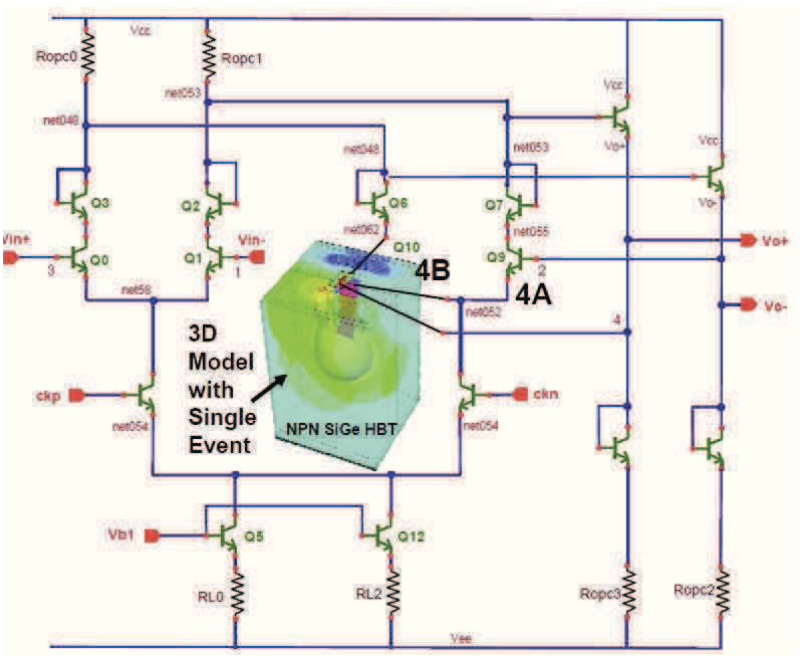

Figure 1.25: Mixed-Mode simulation setup of the SiGe HBT-based subcircuit for single-event effect (SEE) analysis: The 3D NanoTCAD model with physics based modeling of Radiation Event (an ionizing track, or imported Geant4 tracks) is coupled with a circuit solver (Spice or Cadence Spectre) (inspired from [84]).

rate calculations and the FIT performance of designed test cell's depending on the type of the particle environment specified. It is shown that this empirical model can be used to model much more complex circuits as NAND, NOR, large inverters with a good accuracy. The method seems to be very promising as it employs real technological process, doping profiles and TCAD-extracted accurate current models. To the weak points, however, belong the enormously time consuming construction of database before the SER predictions can be performed and the necessity of possessing the TCAD doping profiles and 3D structures that are very often available after the silicon tape out when the process is mature. The predictive simulations for new technologies would be extremely difficult to be carried out.

6.2 Monte-Carlo-based

The difficulty of simulating of large number of events to obtain a sufficient SEU statistics and to calculate circuit upset rates for a given environment has forced the research centres and manufacturers to develop alternative approaches that utilizes Monte-Carlo methods and are based on standalone codes [40; 87; 96; 97] or ones that use coupling with a circuit solver [85; 99]. These approaches replace computationally demanding 3D mesh structure with a simplified compact analytical

models decreasing the accuracy.

Two primary difficulties with transistor-level SEE modeling and simulation can be distinguished. One is the generation of an accurate SE current pulse or collected charge. Device simulators can much more accurately represent the SE current pulse generation, but are limited in size of a circuit to be modeled. The second difficulty is the charge sharing at multiple nodes. Typical transistor-level SEE modeling applies the ion strike to one node not allowing for multiple node charge collection and even if multiple node current injections are performed such simulations have to be tied to the spacial relationship of the circuit nodes that is not available on the schematic level.

MRED developed by Vanderbilt University

Warren et al. [85] proposes simulation methodology based on Monte-Carlo Radiative Energy Deposition (MRED) software developed at Vanderbilt University and integrated with the Synopsys HSPICE circuit simulator which is presented in Figure 1.26. For upset rate predictions, particle transport and energy deposition uses the Geant4 [61] physics and a device geometrical model that includes the inter-layer dielectrics and passivation layers. The innovative use of Geant4 libraries allows to model the spatial and temporal distribution of charge that is generated by a particle. Then, the energy deposition is tracked in the sensitive volumes, i.e. in a set of Rectangular Parrallel Piped (RPP), that are placed near off-state p-n junctions. There are some drawbacks of this method: 1) the placement of sensitive volumes, their collection efficiencies and their dimensions are calibrated to fit the experimental data by an iterative procedure described in [99], 2) the use of critical charge values does not account for the shape, magnitude and temporal occurrence of ion-induced current pulse that is arbitrarily computed from collected charge value. Despite these inconveniences, this simulation method is capable of predicting not only simple SRAM sensitivity but also the more complex radiation-hardened-by-design flip-flops and their upset rates [95].

SEMM-2 developed by IBM

Soft-Error Monte-Carlo Model 2 (SEMM) approach developed at IBM is described in details in [87]. This code is intended to take into account the particle transport in the complex geometries and Back-End-Of-Line (BEOL) material compositions [100]. Moreover, the different environment models have been developed to account for alpha particles, ion beam experiments, cosmic rays and other sources. Similarly to Vanderbilt University's approach, SEMM geometry uses the sensitive volume approach and the upset occurrence is verified by critical charge criterion extracted from circuit simulations or experimental tests. The

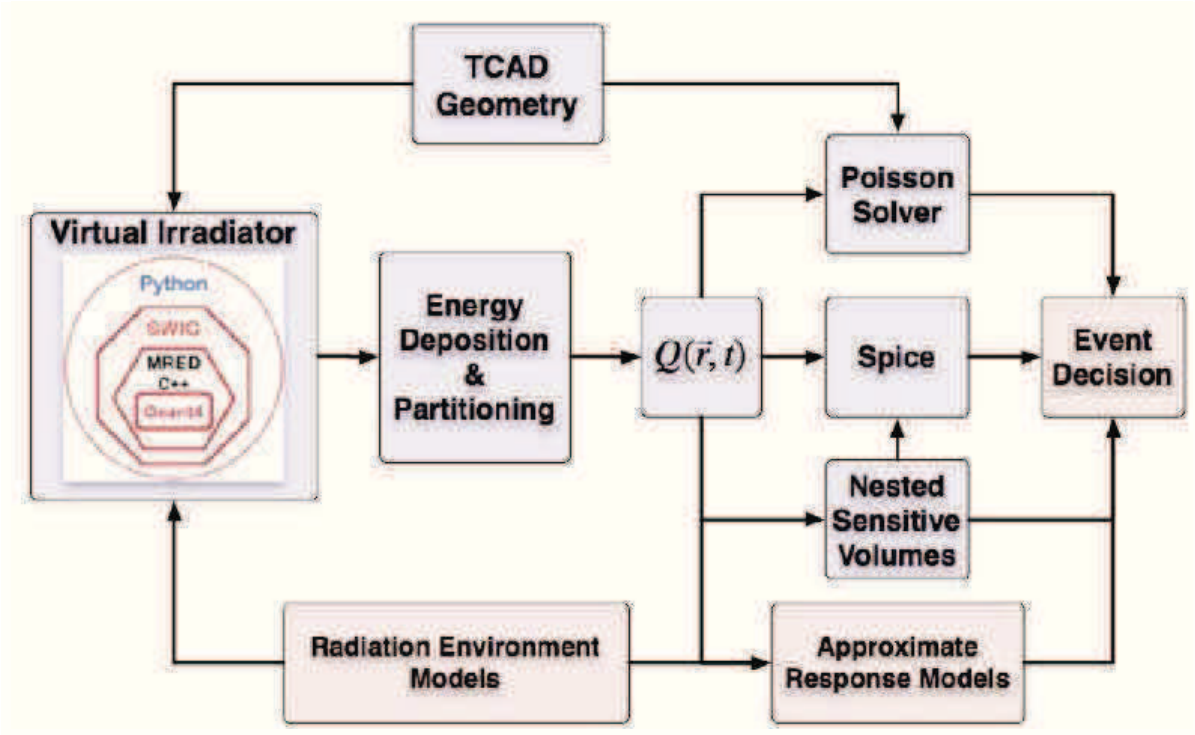

Figure 1.26: Monte-Carlo Radiation Energy Deposition simulation flow developed at Vanderbilt University (inspired from [86]).

advantage of SEMM-2 is the analysis of very complex BEOL geometries and their impact on SER, the inconveniences remain the same as in case of the approach proposed by Vanderbilt University.

PHISco and MCDASIE developed by CEM-2

Prediction of Heavy Ion Sensitivity code (PHISco) and Monte Carlo Detailed Analysis of Secondary Ions Effects (MCDASIE) approaches were developed at CEM-2 in Montpelier and allows the simulation of SRAM memories in both space and terrestrial environment. The codes are dedicated to SEU rate predictions and the in-depth analysis of SEU and MCU upset rates for SRAM memories. A different model is proposed that consists in estimation of ion-induced current pulse obtained from diffusion-collection equations. The parasitic currents are reported in a Imax=f(Tmax) abacus that is previously preprocessed with circuit simulator. The advantage over the static critical charge upset criterion is a partial inclusion of the temporal aspect in SEE simulation and the potential possibility of taking into account different current pulse forms. The weak point is the fixed SRAM geometry that can be simulated. More complex circuits like different Flip-Flop architectures cannot be simulated.

MUSCA SEP3 developed by ONERA

The Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP3) is develpoed at ONERA and described in details in [101]. This platform is dedicated to SEU and MCU estimations in SRAM memories. For ion transport the external database is extracted using GEANT4 application. The charge transport can be based on two different models: 1) charge concept that uses charge collection efficiencies computed as a function of distance of an ion track from the collecting electrode or 2) on the diffusion-collection model. MUSCA SEP3 allows extracting the cross-section, Soft-Error rates as well as the upset rates on orbit. However once more, the simulated geometry is limited to the SRAM memory modeled by the set of arbitrary placed volumes extracted by reverse-engineering techniques from the component. The approach also needs a calibration with ground test data.

7 Research objectives of this study

True integration into microelectronic design phases as part of the engineering CAD environment was identified as one of the major challenges and areas for single event modeling already back in 1993 [98]. The bibliographical research of the main radiation modeling approaches presented in previous chapter shows a capacity of SE simulation however at the same time reveals some common limitations decreasing their interest from a manufacturer's point of view.

This study is oriented towards an industrial integration of a single event simulation platform and benefits from the availability of all technological process data (as silicon measurements-based doping profiles), calibrated transistor PDK models and industrial design accessibility. To satisfy industrial constraints and provide the accurate sensitivity predictions, the following simulation platform requirements have to be fulfilled:

- supporting various circuit architectures and layout techniques
- supporting various technological nodes
- modeling of different radiation environments
- short and automated simulation set-up
- early assessment of circuit sensitivity before tape-out
- evaluation and validation of effectiveness of hardening techniques

- integration with standard IC design tools as Layout Editors (ex. Cadence Virtuoso XL), SPICE circuit solvers (ex. Menthor Graphics ELDO), TCAD simulation tools (ex. Synopsys Sentaurus TCAD), etc.
- optimized simulation run time to give a fast feedback on design

Appendix 1: Most common Single Event Effects

This section explains the most common Single Event Effects that can be classified in two main groups: hard errors (destructive) and soft errors (non-destructive).

To the most common hard errors belong:

- Single Event Gate Rupture (SEGR) is a destructive failure mode especially for power MOSFET caused by charge tracks passing through the gate oxide causing its rupture.
- Single Event Burnout (SEB) is a destructive runaway condition. A particle triggers a Safe Operating Area violation by initiating a high current,high voltage condition in a power device which subsequently enters second breakdown.
- Single Event Latch-up (SEL) consists in triggering of a parasitic PNPN thyristor inherent to CMOS structure by a particle hit. It is typically a combination of active device and isolation regions. The parasitic thyristor causes a short-circuit between power supplies that may sustain destructive high current levels. This high current state is maintained until power to the circuit is turned off.
- Single-Event Snap-back (SESB) single event snap-back, regenerative high current mode related to parasitic bipolar action, similar to latch-up, except that it occurs in three layer structures.

To the most common soft errors belong:

- SEU is a logic error resulting from a change of basic information kept in a latch or memory element. A particle deposits enough energy in a sensitive node to force a bit-flip.
- Single-Bit Upset (SBU) is a SEU that impacts only one cell due to a single particle strike.
- Multiple Cell Upset (MCU) are defined as topological multiple-upsets due a single particle strike.
- Multiple Bit Upset (MBU) are particular type of the MCU that is a logical multiple upset (impacted bits belong to the same bit-word).
- Single Event Transient (SET) is temporary deviation of an analog signal, the analog equivalent of SEU. The magnitude and duration of the output error are variable, and may become significant if sampled or acted upon.

- Single Event Functional Interrupt (SEFI) is a condition where the particle strike causes the device to stop operating normally, losing its function. The condition may be reset by re-writing information to the affected area or may require a reset or power cycle.

Appendix 2: SEU Cross-section and Soft Error Rate

There are two major metrics that were adapted by the radiation community to compare the circuit sensitivity: SEU cross-section and Error rate.

- A SEU cross-section is a parameter defining circuit sensitivity and can be measured during accelerated tests in the radiation facilities or during real time experiments. It can be expressed for a component in cm^2 or independently on the component size in $cm^2 bit^{-1}$. The cross-section is calculated by dividing the number of SEU detected during the experiment by the particle fluence and optionally by the component size:

$$XS = \frac{SEU_{num}}{Fluence \cdot bit_{num}} \tag{1.5}$$

  where SEU_num is a number of SEU detected during the experiment and bit_{num} is the component size in bits. Geometrically, the SEU cross-section can be associated with sensitive surface of a device.

- From the cross-section and knowing the particle spectrum at a given location, it is possible to derive the Error Rate. If the cross-section is multiplied by the particle flux and integrated on the whole spectrum, the result is the Error Rate or SEU rate. The general equation giving the error rate is the following:

$$ErrorRate = \int_{E_{min}}^{E_{max}} dE \frac{d\Phi(E)}{dE} \cdot XS_{SEU}(E) \tag{1.6}$$

  where $\frac{d\Phi(E)}{dE}$ is the differential flux of the particle in $cm^{-2} MeV^{-1} s^{-1}$, XS_{SEU} is the SEU cross-section of a particle in units of $cm^{-2} bit^{-1}$. Error rate is in units of $errors bit^{-1} s^{-1}$.

  To convert the units to FIT, error rate in $errors bit^{-1} s^{-1}$ has to be multiplied by 10^9. 1 FIT (Failure in time) corresponds to the number of failures per 10^9 device-hours.

Chapter 2

Tool Suite for Radiation Reliability Assessment (TIARA)

1 Introduction

This chapter describes in details the TIARA platform that has been developed in the framework of this study. TIARA is a complete general-purpose simulation platform allowing for accurate numerical evaluations of sensitivity of microelectronic circuits in various radiation environments. One of the most important platform requirements, kept in mind on every stage of development and defining the tool architecture, is the industrial use during design, optimization and qualification of circuits (as SRAMs and FFs) including the innovative solutions of both rad-tolerant and rad-hard IPs.

This chapter is organized as follows: section 1 and 2 respectively present the complete TIARA simulation flow with the major inputs and how the equivalent circuit geometrical structure for simulation is created. Section 3 focuses on the description of different environments that can be taken into account by TIARA. Then, transport modeling in both BEOL and Front-End-Of-Line (FEOL) are presented in details. The different bit-flip occurrence criteria are discussed in section 6. Section 7 discusses the code C++ implementation with engineering solutions and finally TIARA modeling uncertainties are the subject of the last section of this chapter.

2 TIARA Simulation flow

The simulation flow is structured in several independent modules in order to facilitate future upgrades as well as code adaptability to different

device architectures and technology options. The interfaces between modules are well defined to make possible autonomous developments and refinements of one module without the necessity of adapting the others. This modular design greatly simplifies the code maintenance.

The main simulation flow is shown in Figure 2.1. The core of the code corresponds to the center of figure, all inputs are on the left and on the right and the outputs are at the bottom. Three groups of input files can be distinguished: 1) design inputs, 2) environment models, 3) technological information:

- From the design phase, three inputs have to be provided to TIARA: the geometry of the simulated cell in GDS format (detailed in section 2), circuit schematic as a SPICE netlist file (*.cir) and the Process Design Kit (PDK) libraries with all transistor models, simulation corners, definition of operating conditions and parasitics. The major advantage is that these inputs are easily to obtain for a chip manufacturer as STMicroelectronics.

- The special environment module has been developed and contains reaction/ion databases reproducing real test conditions and is detailed in the section 3 of this chapter.

- The following technological information has to be delivered to TIARA: BEOL gemetrical information (to account for ion energy loss and particles that are stopped in BEOL), SRIM data, and transport model parameters. From SRIM simulations, the Ziegler's tables (ion LET as a function of ion energy) for all possible ions in silicon and silicon dioxide were extracted and are directly parsed by TIARA. The specially developed TIARA libraries, based on Ziegler's tables, allow for computing the ion LET, energy loss and ion range. For each new technology, the 3D TCAD simulations are first carried out for the purpose of analysing the carrier transport in the structure. These analysis are then used to calibrate analytical transport models that are used by TIARA.

The main program creates in a first step an equivalent 3D structure from a GDS file, then continues to the generation of a radiation event. In this study a radiation event is defined as a heavy ion, proton, muon, alpha strike or a neutron/silicon nuclear reaction in the simulation volume. The big variety of radiation event generation is supported: from reproducing the ion beam at the radiation facilities with particular ion energy, tilt and roll angles to the ion or reaction generation in the IC

volume to reproduce real time alpha as well as neutron experiments.

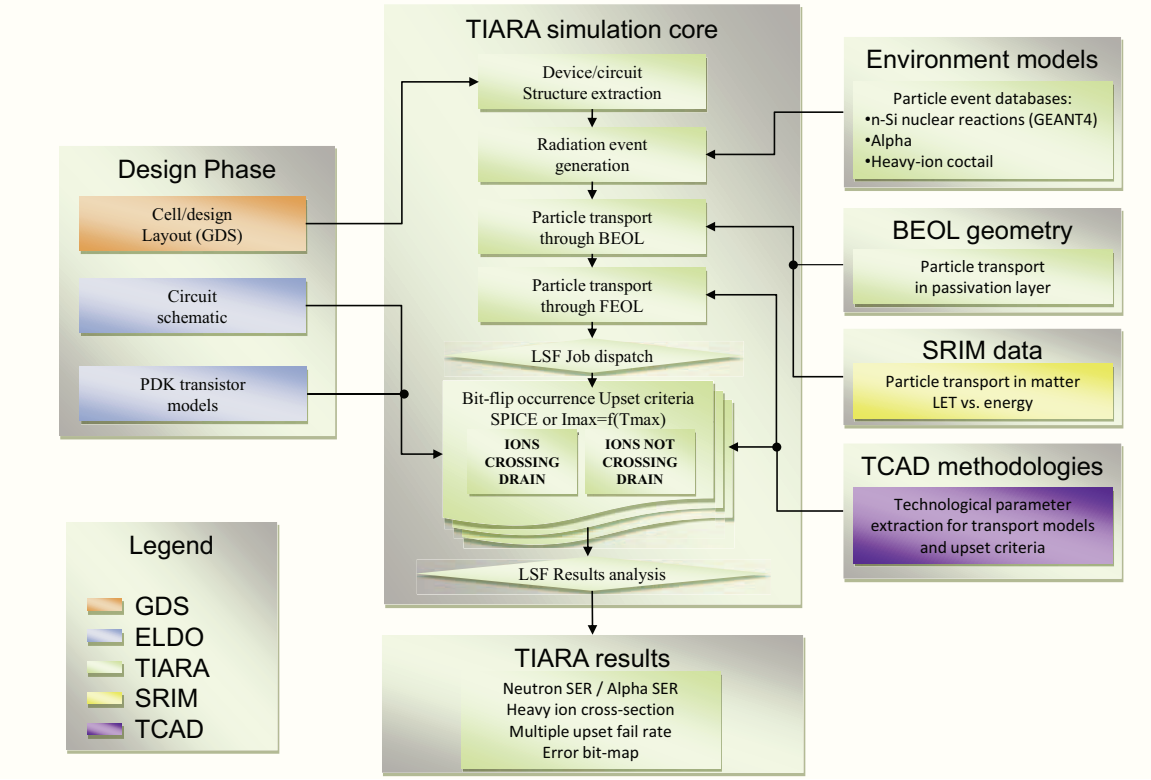

Figure 2.1: The overall view of TIARA simulation flow with main inputs/outputs and major modules.

Once radiation event is generated, the energy loss in BEOL and FEOL is computed until it stops or leaves the simulation volume. The FEOL transport module employs proper carrier transport models to compute the parasitic currents in the circuit nodes. Depending on the circuit simulation options, it is possible to use the distributed system via the LSF job scheduler. This option is especially useful for all FF radiation analyses when SPICE simulation is used as an upset criterion. Then the SPICE simulations are run in parallel on many CPUs accelerating significantly the simulation run time. The last module analyzes the upset number, treats the simulation data and saves it in the proper simulation output and log files.

Several TIARA outputs can be generated as a function of simulation options. They can be presented as alpha or neutron SER that can be directly compared with experimental tests carried out at the radiation facilities or using real time test platforms, as heavy ion cross-sections also directly comparable with experimental tests. For SRAMs, it is possible to obtain the multiple-cell upset percentages and compute the MCU fail rates. Very interesting feature from designers' perspective is the

error bit-map plot that is superposed on the GDS layout highlighting the most sensitive cell nodes. Simulation integrates interesting debug tools and cell sensitivity analyses that will be presented in the following paragraphs 6 and 7.

3 Device/Circuit simulation structure creation

The first stage before simulation is to prepare the simulated structure. Previously presented simulation tools in the literature [40; 96] used fixed geometries that cannot be changed without code modifications, they do not take into account many geometrical effects such as Shallow Trench Isolation (STI), depth of junctions or funnelling phenomena. In the latest developments [40] the Nwell regions were taken into account as charge diffusion barriers.

To fulfil the objectives presented in section 1.6., it is required to develop a structure extraction methodology that represents the simplified 3D structure of a cell directly using the industrial standards and industrially available technological data. TIARA structure creation module extracts the required information directly from layout files in GDS format such as the surfaces of the drain electrodes for NMOS and PMOS transistors, and their positions, the N-well dimensions and cell spacing, etc. The representative 3D structure for Monte-Carlo simulation only contains reverse-biased junctions of the design. The other junctions are omitted as their contribution to charge collection is small. The code also takes into account the N-well as a diffusion barrier for carriers [102]. All the necessary depth information are obtained from TCAD doping profiles or SIMS measurements, i.e. both the N-well, P-well, the substrate (P-sub) and DNW depths as well as junction and STI depths.

The simulated structure dimensions are chosen as a function of simulated cell and the radiation environment in order to take into account all effective particle strikes. For alpha and heavy ion simulations the simulated structure boundaries are equal to the real x and y structure dimensions and the real depth of BEOL/FEOL layers, however for neutron experiments the simulated volume is enlarged to account for nuclear reactions occurring outside of the cell (typically by +/- 5μm on each side of the cell).

4 Environment modeling module

One of the major objectives of this work is the ability of simulating radiation effects in space and terrestrial environments as well as reproducing the experimental tests for validation of simulation and calibration

purposes. To be able to satisfy these constraints, special architecture of environment module has been introduced, its interface format with TIARA and radiation event generation models are described in the following paragraphs.

4.1 Architecture of the environment module

Chapter one presented space and terrestrial radiation environments. Simplified models of these environment module and coupling strategies with TIARA are shown in Figure 2.2. The architecture of the environment module can be decomposed in two major environments, an in different particle types for each of these environment.

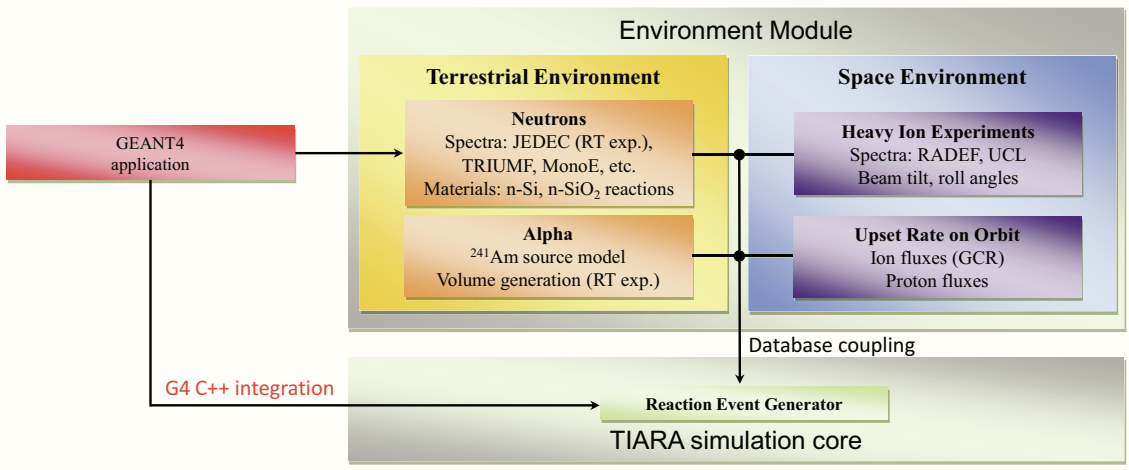

Figure 2.2: The architecture of the environment module.

TIARA terrestrial environment module contains the following simulation models:

- Neutron-silicon (n-Si) and neutron-silicon dioxide (n-SiO_2) reactions databases for different continuous neutron spectra as the reference New York JEDEC spectrum, TRIUMF and LANSCE as well as mono-energetic (monoE) reactions databases for different energies (1, 10, 14, 50, 100, 150 MeV and 1 GeV). Nevertheless, the reaction database for any spectrum can be compiled. These databases allow to reproduce real time (RT) and accelerated neutron experiments.
- Alpha americium ^{241}Am source emission database has been extracted as well as the the volume generation in the die volume that allows to perform simulations for real time (RT) experiments.

TIARA space environment module contains the following simulation models:

- Heavy ion experiments models contain databases that reproduce RADEF and UCL heavy ion cocktails with their beam orientation (tilt and roll angles) and ion species energies.
- Upset rate on orbit can be simulated using the compiled databases for Heavy ion and proton fluxes on orbits.

There are two available coupling interfaces between TIARA and environment module: coupling using a preprocessed radiation event database or a direct coupling with 4 C++ application that uses a General Purpose Particle Source (GPS) and generates a particle strike (ex. neutron strike in a silicon structure that causes spallation of a silicon atom into several ionizing fragments).

4.2 Interface data format between Environment module and TIARA

Figure 2.3 shows an example of interface format between the environment module and TIARA. This example is limited to two nuclear reactions extracted from the G4 JEDEC neutron-silicon database. The format of the entire database and all other databases is the same. Additionally, the above mentioned interface objects coupling G4 simulation and TIARA core contain strictly the same information.

Each radiation event is composed of at least two lines. The first line contains the incident particle and event information: number of the event in the database (Event#), energy of the incident particle (Energy), the reaction position (Vertex position) and finally the number of ionizing products (Products#). The following lines contain the information of each secondary product, i.e. its name and isotope (Name), the mass (Mass#) and atomic (Atomic#) numbers, the initial energy (Energy) and particle momentum (Momentum PX, PY, PZ). In the case of alpha or heavy ion databases, the incident particle and the ionizing product are the same.

4.3 Radiation event generation

Several models of radiation event generation are available and depend on the simulation configuration:

- For heavy ion simulations the following generation models are supported:
    - ⋆ Event generation on the active device surface with a random position and defined beam direction corresponding to

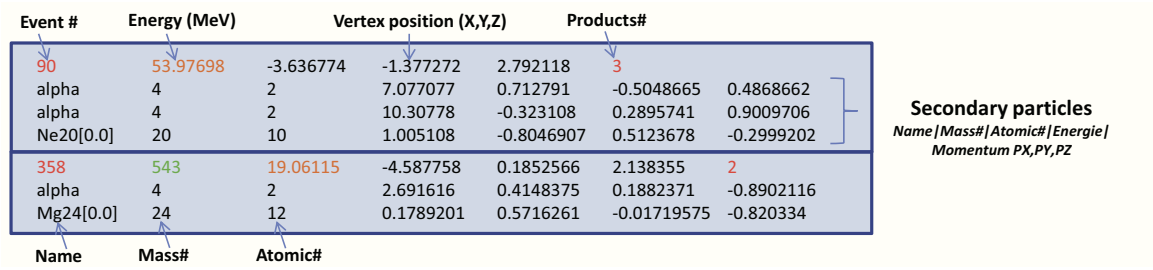

Figure 2.3: Illustration of the database format unified for every environment/particle type enabling handling a great variety of radiation environments.

the beam direction during the experiment that emulates the tests at a radiation facility.

⋆ Event generation on the active device surface with a random position and random direction that emulates the natural environment.

- For alpha simulations the following models are supported:

  ⋆ "Alpha source model" emulating accelerated alpha measurements. The model takes into account the real geometrical dimensions and emissivity of the americium alpha source available at STMicroelectronics in Crolles. It is supposed that the alpha source is directly placed on the top of the chip passivation, the generated particles are first transported via the passivation layers and then the die active area. Alphas are generated randomly in the source and with random direction.

  ⋆ "Alpha generation in die volume" with a random position and random direction that reproduces real-time alpha tests performed underground. A particular alpha emission from a radioactive atom can be considered as well as different families and different emitting atoms as [103].

- While simulating neutrons, the neutron-Silicon reaction position is randomly chosen, but the directions of all secondary ions remain the same as in the reaction database complied with G4 simulation. Since G4 simulation reproduces the test conditions, the neutron beam is considered to be orthogonal to the die active surface. This assumption is also valid for real-time experiments performed at ATEP, where atmospheric neutrons incidence is expected to be mainly normal to the Earth's surface.

5 Particle transport through BEOL

Particle transport through BEOL layers results in an energy loss and finally in the change of the initial particle LET. Several works in the past addressed the different BEOL topologies. In [100], the authors have reported an innovative methodology of taking into account the realistic BEOL geometries. Their method, named 3D Monte-Carlo Heavy Ion Charge Deposition (MCHIDQ), is based on the discretization of the BEOL region into a large number of pixels containing the information related to the mixture metal-dielectric composition. In Figure 2.4, the cross-section through the chip metallization layers is shown together with the metal content on three different BEOL levels. The middle level is characterized by high metal concentration while for the low level this concentration is the lowest. The SEMM-2 simulation tool developed by IBM can be coupled with realistic BEOL geometries. The authors clearly evidence the variation of the alpha particle energy as a function of different BEOL geometries and the change of deposited charge. They did not report the link between this energy loss and the SER estimation.

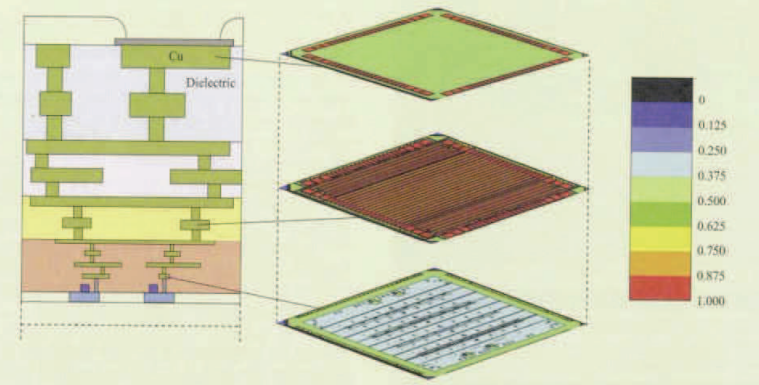

Figure 2.4: On the left the representation of real chip metalization layers and three cross-sections through the BEOL materials at different levels. The scale shows the percentage of metal-dielectric content (inspired from [100]).

In [40], two different BEOL geometries have been evaluated with their impact on the SEU rates. On one hand, the passivation layer composed of silicon dioxide only is studied and on the other hand the alternation of the silicon dioxide and full metal planes amplifying the metal coverage. The simulated SRAM geometry is shown in Figure 2.5(1), as well as two models of BEOL geometries in Figure 2.5(2a) and (2b). SRIM simulations showed that for the modeling with metal layers the particle energy loss is always superior to that for the simple silicon dioxide model, nevertheless this influence on the particle LET is low. Computations were performed for several ions ranging from carbon to iodine. Moreover, the Monte Carlo simulation results for both models are equiv-

alent giving the average single event upset cross-section variations inferior to 5%. According to [40], this upset cross-section variation stays very small even for particles with lowest LET values. For carbon ion with LET of 1.6 $MeV \cdot cm^2 \cdot mg^{-1}$ the cross-section variation equals to 3%. This result suggests that for alphas, neutrons as well as heavy ions the simplified modeling taking into account BEOL composed of silicon dioxide is a good approximation.

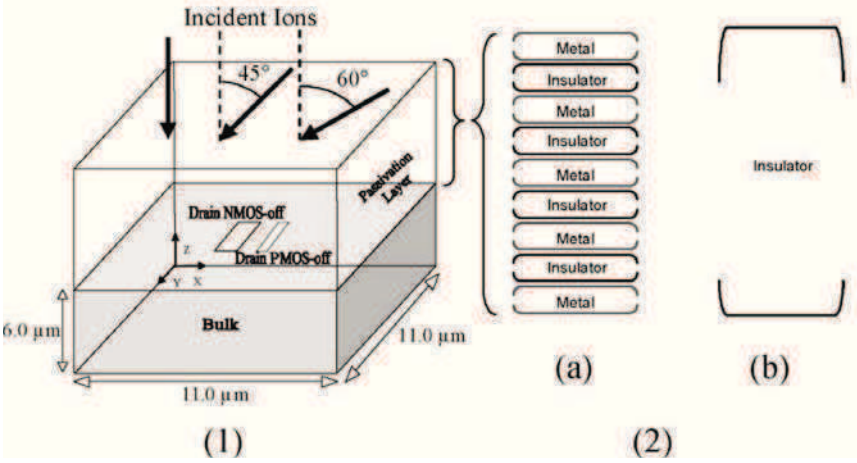

Figure 2.5: Schematic representation of the simulated structure by PHISco code (1) with two models of chip metalization layers evaluated (2a and 2b) in [40].

The TIARA's ion transport through metallization module computes the energy loss when it is relevant, i.e. when an ion is generated outside the chip active area (ex. accelerated alpha simulations with a radioactive source) or in the chip BEOL layers (neutron simulations). The tabulated Ziegler's tables [53] allow extracting information of energy loss in the passivation layers (the LET values and ranges of each particle) based on particle initial energy . The metallization layer is assumed to be made of silicon dioxide. As shown above, this approximation gave comparable results to those obtained when considering more complex metallization layers. Nevertheless, the extension for other layers is possible by creating more complex BEOL model using the copper, tungsten, etc.

6 Particle transport through FEOL

Carrier generation and transport in the silicon active area is the most important part of the simulation flow and influences very significantly the accuracy of SER assessment. Ion transport in the substrate module allows modeling of the electron-hole pairs generation in the semiconductor lattice as well as drift, diffusion, collection and recombination

processes of deposited carriers.

Charge transport in the semiconductor lattice is subjected to diffusion caused by the carrier concentration gradient and the drift caused by the electric field. TIARA classifies the single events similarly: when the ionizing particle crosses the space charge regions of the off-state drain junctions the special drain impact model is applied [88], otherwise the diffusion-collection model is used [104].

In the first part of this section, the diffusion-collection model is presented together with its newest refinements for highly scaled CMOS technologies, then, the double exponential current pulse for drain impacts is described and finally, the new modeling of bipolar amplification is given.

6.1 Diffusion-collection model for charge generated outside the electric field

Model presentation

According to both drift-diffusion and continuity equations and in absence of electric field (no drift contribution), the excess carriers generated by an ionizing particle are subjected to a pure thermal diffusion mechanism (Equation 2.1).

$$\frac{\partial n}{\partial t} = D \cdot \Delta n \tag{2.1}$$

where n is the carrier density (electron or hole) semiconductor and D is an ambipolar diffusion coefficient. Approximating the ion track as a succession of elementary punctual carrier densities and assuming that the behaviour of these quasi-point charges is governed by a spherical diffusion law, the temporal and spatial concentration of carriers diffusing in the p-substrate (n-well) is then described by the following equation [104]:

$$n(r,t) = \int N_0 \cdot \frac{e^{-\frac{r^2}{4Dt} - \frac{t}{\tau}}}{(4\pi Dt)^{3/2}} \cdot \mathrm{d}l \tag{2.2}$$

where N_0 the number of the electron-hole pairs, τ is the carrier lifetime, r is the distance of considered point from the track, and t is the time. With respect to previous works [40], the diffusion-collection model (presented in Equation 2.2) was enhanced by taking into account the recombination processes via the carriers' lifetime. Carrier recombination results from interaction between electrons and holes in

semiconductor structure and characterizes the disappearance of carriers per unit of time and per unit of volume. This enhancement influences mostly the SER estimations for large structures, such as RHBD FFs, that are presented in the following sections of this work, in which carriers generated far from the collecting electrode recombine before reaching the border of the space charge region of any junction. The direct relation between the number of electron-hole pairs generated in silicon and a particle linear energy transfer can be done:

$$N_0 = 10.3 \cdot \frac{1}{q} \cdot LET(l) \tag{2.3}$$

where q is the elementary charge in Coulombs and LET(l) is the linear energy transfer in $C/_{cm}$ as a function of particle penetration depth in silicon.

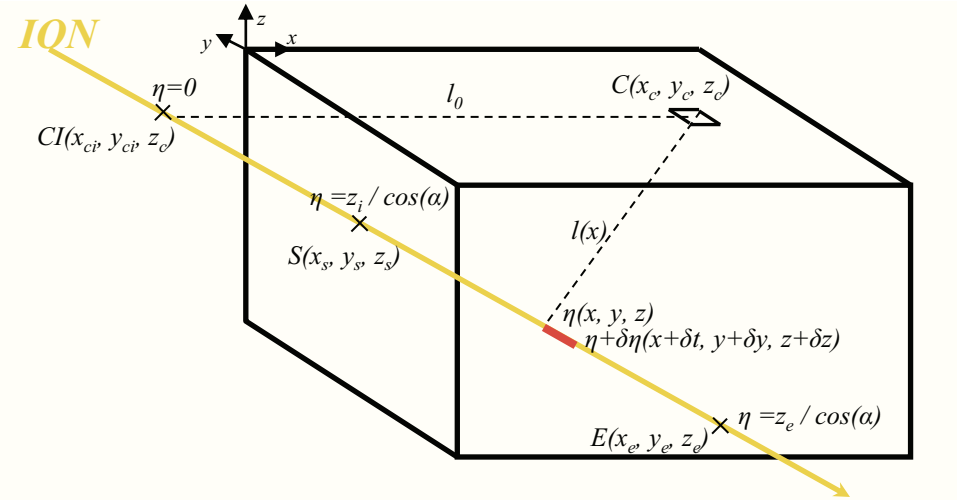

Figure 2.6: The simplified representation of considered geometry with main data used in diffusion-collection equations.

Let us consider the following geometry presented in Figure 2.6. A point on the electrode contact surface is denoted as $C = (x_c, y_c, z_c)$, the image of the impact point on the electrode surface $CI = (x_{ci}, y_{ci}, z_c)$, the ion generation start point $S = (x_s, y_s, z_s)$ and the ion generation end point $E = (x_e, y_e, z_e)$. l_0 distance on (x,y) plane between the ion trajectory and the considered point C is given by $l_0 = \sqrt{(x_{ci} - x_c)^2 + (y_{ci} - y_c)^2}$. As a first approximation, we consider particle LET constant while crossing the structure, thus this term can be taken out of the integral. By integrating the Equation 2.2 between the generation start and end points, the exact analytical solution of carrier concentration arriving at a considered point C of the semiconductor as a function of time can be expressed as follows (Equation 2.4).

$$n(t) = \frac{N_0}{8\pi Dt} \cdot e^{-(\frac{l_0^2}{4Dt} + \frac{t}{\tau} - \frac{k^2}{16Dt})} \cdot \left[erf(\frac{2z_e + kcos(\alpha)}{2cos(\alpha)\sqrt{4Dt}}) - erf(\frac{2z_s + kcos(\alpha)}{2cos(\alpha)\sqrt{4Dt}}) \right]$$

where *erf* is the error function, z_s and z_e are the z coordinates of the start and end point, respectively, α is the tilt of the trajectory from normal, and the parameter k is defined as follows (Equation 2.4).

$$k = 2sin(\alpha)[cos(\beta) \cdot (x_{ci} - x_c) + sin(\beta) \cdot (y_{ci} - y_c)] \tag{2.4}$$

where α and β are the ion tilt and rotation angles, x_{ci}, x_c, y_{ci}, y_c are x and y coordinates of the image of the impact point on the electrode surface and the point of electrode contact, respectively. The total charge from the ion track collected at the drain electrode is obtained by integrating the concentration of carriers on the drain surface. Then, the charge is converted into a current by multiplying the carrier concentration by the elementary charge and by the average collection velocity via space charge region of the reverse-biased drain.

$$I(t) = q \cdot v \cdot \iint_{xy} n(t) \cdot \mathrm{d}x\mathrm{d}y \tag{2.5}$$

where q is the elementary charge (q = $1.6 \cdot 10^{-19}$ C), v is the carrier collection velocity, and n(t) carrier concentration from the diffusion-collection model.

Determination of model input parameters

The diffusion-collection equations presented in previous paragraph require 3 input parameters for both NMOS and PMOS transistors to compute ion-induced currents at drain electrodes: the ambipolar diffusion coefficient, the carrier lifetime in the well/substrate and the carrier collection velocity via the space charge region. Two approaches were developed to determine these parameters: i) an analytical computation of parameters based on 3D TCAD ion simulation and ii) a matching of TCAD simulations with diffusion-collection model to fit the input parameters.

The first method consists in performing device simulations of horizontal ion impacts below the drain electrode [40] and calculating the model input parameters based on TCAD information of carrier velocity and carrier mobility as a function of time and space. The average collection velocity is calculated by the integration of the charge velocity during collection time and for the depth of space charge region of off-state junction. Equation 2.6 is used for the computations.

$$v = \frac{\iint_{\Delta x \Delta y} v(z,t) \cdot \mathrm{d}z\mathrm{d}t}{\Delta z \cdot \Delta t} \tag{2.6}$$

where v is the average collection velocity, v(z, t) is the carrier velocity as a function of time and depth in the substrate, Δz is the depth of the space charge region, and Δt is the ion-induced SET duration.

The ambipolar diffusion velocity is determined by the average diffusion coefficient. Its value is given be the following equation:

$$D = \frac{(n+p) \cdot D_n \cdot D_p}{n \cdot D_n + p \cdot D_p} \tag{2.7}$$

where n and p are electron and hole densities, D_n and D_p are the diffusion constants for electrons and holes, respectively. For semiconductor, diffusion constants are given by the Einstein's relationships:

$$D_n = \frac{k \cdot T}{q} \cdot \mu_n \tag{2.8}$$

$$D_p = \frac{k \cdot T}{q} \cdot \mu_p \tag{2.9}$$

The ambipolar diffusion coefficient, given by Equation 2.10, is calculated until stable memory logic states are stabilized and for the depth of the well/substrate.

$$D = \frac{\iint_{\Delta x \Delta y} D(z,t) \cdot \mathrm{d}z\mathrm{d}t}{\Delta z \cdot \Delta t} \tag{2.10}$$

where D is the average ambipolar diffusion coefficient, D(z, t) is the ambipolar diffusion coefficient as a function of time and depth in the well/substrate, Δz is the depth of the well, and Δt is the ion-induced SET duration.

All parameters presented above can be calculated based on data obtained from TCAD simulations, from which electron or hole concentrations, mobilities, and velocities are extracted. In this study, several heavy ion impacts in the full 3D SRAM cell have been simulated and the results have been compared with previous studies [40] for SRAM in CMOS 90nm LP/GP technology .

The obtained values of technological parameters compared to previous studies are the following:

- $v_{Nmos} = 5.97 \cdot 10^6 cm/s$ ($3.04 \cdot 10^6 cm/s$)
- $D_{Nmos} = 11.3 cm^2/s$ ($10 cm^2/s$)

- $v_{Pmos} = 1.91 \cdot 10^6 cm/s$ ($3.24 \cdot 10^6 cm/s$)
- $D_{Pmos} = 4.23 cm^2/s$ ($5 cm^2/s$)

Parameters D calculated analytically are quite similar to those calculated by Correas [40]. The method described above has been chosen to extract D parameters for CMOS 65nm LP and other technologies analyzed in this work.

However, for collection velocity parameter computations that use Equation 2.6 give different results. Although space charge region has been extracted very precisely with 1 nm step for z-axis integration, the values are not comparable to those calculated previously. The extraction method described above has several major drawbacks:

- First, the choice of the integration limits as a function of the depth of the space charge region has a huge influence on the calculated average collection velocity value and it is difficult to define precisely the space charge region border. For our computations, the integration limits have been defined between the maximum electric field and 1% of the maximum electric field value.
- Second, the variations of the v parameter during the disturbance are important (between $0.5 \cdot 10^6$ and $10.0 \cdot 10^6 cm/_s$) the simple integration for the whole duration of the SET can give very misleading values.

Collection velocity is directly proportional to the parasitic current magnitude estimated by the model (Equation 2.5), thus, should be computed with maximum precision, and even small discrepancies of this parameter can influence the overall simulation results. In the frame of this thesis, a second method has been proposed for extraction of v parameters, that consists in matching current pulses from TCAD simulations with current pulses obtained from diffusion-collection model. The TCAD impacts were simulated for a LET value equal to 10 $MeV \cdot cm^2/mg$ that is a representative LET value for secondary products from neutron-silicon reactions. Heavy ion impacts in source of NMOS and PMOS transistors and for several distances from the off-state drain were chosen. Current pulses have been saved and compared to those calculated using diffusion-collection model. Collection velocity parameters are adjusted to best TCAD fit especially to match the maximum ion pulse magnitude that is used in upset criterion. For 65 nm CMOS technology, those parameters are as follows:

- $v_{Nmos} = 2.42 \cdot 10^6 cm/_s$ ($3.04 \cdot 10^6 cm/_s$)
- $v_{Pmos} = 4.33 \cdot 10^6 cm/_s$ ($3.24 \cdot 10^6 cm/_s$)

The carrier lifetime depends on doping concentration and is presented in Figure 2.7 [105]. To extract the carrier lifetimes, the average doping profiles in the Nwells and in the substrate are calculated based on TCAD profiles.

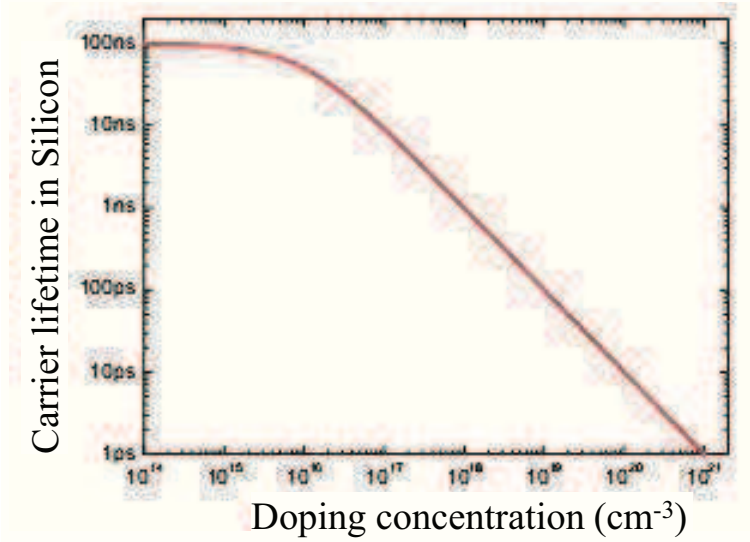

Figure 2.7: Carrier lifetime in silicon as a function of doping concentration [105].

6.2 Drift current model in the presence of electric field

When the ion strikes the off-state drain junction area of a NMOS or PMOS transistor, the generated carriers are instantly separated by the electric field and minority carriers in the well are promptly collected by the junction. Additionally, the funnelling phenomenon enhances field assisting collection (see Chapter 1.2.2. Charge transport and collection for more details). To obtain the estimation of this current pulse, a set of simulations as a function of LET have been performed using TCAD tools (Sentaurus Synopsys package)[89] and exact 3D geometry data optimized for the particular ST manufacturing process and for the structures under investigation. The models of ion induced currents for both transistor types have been derived from the specific TCAD structures representative for NMOS and PMOS transistors of the FF. The drain surface variations for the several Flip-Flop architectures have been analyzed and it was found that they weakly affect the collected current. The pulse of the struck reverse-biased drain is modeled by the following formula:

$$I(t) = \begin{cases} 0 & \text{if } t < t_{imp} \\ I_{max}(LET) \cdot e^{\frac{t-t_{imp}}{\tau_{rise}}} & \text{if } t_{imp} < t < t_{imp} + \tau_{rise} \\ I_{max}(LET) \cdot (1 - e^{-\frac{t-(t_{imp}-\tau_{rise})}{\tau_{fall}}}) & \text{if } t > t_{imp} + \tau_{rise} \end{cases} \quad (2.11)$$

where the t_{imp} is the ion impact time, τ_{rise} and τ_{fall} are the rising and the falling times of ion-induced current pulse, and $I_{max}(LET)$ is its magnitude defined by Equation 2.12. I_{max} values are computed for both NMOS and PMOS drains using TCAD simulations of ion strikes in the drain junctions for different LETs. It allows the assessment of I_{max} as a function LET.

$$I_{max}(LET) = A \cdot ln(LET) + B \quad (2.12)$$

where A and B are two constants fitted from TCAD data.

7 Bit-flip occurrence and Upset criteria

The most commonly used approach for latched circuits in the literature, introduced in the 70's by May [4], is to calculate the charge collected by a transistor and to compare it with a particular charge value, called critical charge. This critical charge is defined as the number of carriers that define the logical "1" or "0" states or more precisely as the minimal collected charge that causes a bit-flip and it is determined using the SPICE simulation [107] or deducted from the experimental data.

In this study, several upset criteria have been studied for different input circuits. For both SRAMs, standard and RHBD FFs, the upset occurrence is calculated using the estimation of the ion-induced current pulses in the drain electrodes that are obtained from diffusion-collection/drift current models and the circuit simulation thanks to the dynamic link between TIARA and SPICE circuit solver.

Additionally for SRAM simulations, the simplified analytical upset criteria can be applied: 1) when a strike that does not cross the off-state drain junction the I_{max} = f(T_{max}) characteristics are applied and 2) when a strike directly impacting the device in the off-state drain junction region the critical LET is used.

7.1 SPICE for SRAM memories standard and RHDB FFs

New upset approach was specially developed to give the possibility of increasing the precision by considering the ion induced current pulse

shape. Moreover, circuit simulation has become a standard design tool and is compatible with all circuit architectures and PDK models. For each nuclear event, a SPICE simulation of the entire SRAM bit-cell netlist is performed. The schematic of the circuit uses SPICE models and data obtained from the GDS file by parasitic extraction (capacitors, resistors). Parasitic currents are computed for each drain in proximity of the event and for all ionizing particles resulted from this event. Next, all generated current pulses are injected in the SPICE transient simulation at exact nodes. The initial values memorized in the latch are then compared with the values after the single event transient due to the impact. If a value(s) changed, an upset(s) is (are) counted.

7.2 Imax=f(Tmax) for SRAM memories and standard FFs - case of ions not crossing the sensitive drain junction

The upset criteria for ions not crossing the sensitive drain junction, known also as the I_{max} = f(T_{max}) criteria [106], plot the minimal peak amplitude of the ion-induced current pulse needed to cause an upset, as a function of the particular time corresponding to the occurrence of this amplitude.

In this study, the different I_{max} = f(T_{max}) characteristics have been calculated for NMOS and PMOS transistors of each memory architecture and for each technology using SPICE simulations. The parasitic current pulses obtained from diffusion-collection equations at a given TT_{max}) are injected into the SPICE simulation in order to find the lowest amplitude causing a bit-flip. This is repeated for many TT_{max}) values typically from 1ps to 10ns to obtain the complete I_{max})=f(T_{max})) characteristic. During the Monte-Carlo simulation, for each ion that does not cross the drain, the amplitude (I_{max}) and time of this amplitude (T_{max}) of the ion-induced current are reported and compared to the I_{max} = f(T_{max}) characteristic [104]. If the considered current pulse lies above the I_{max} = f(T_{max}) curve, an SEU occurs.

7.3 Critical LET for SRAM memories and standard FF - case of ions crossing sensitive drain junction

When an ion crosses the drain, the electric field promptly separates carriers which are instantaneously collected via a space charge region. This phenomenon is modeled with TCAD simulations to find the minimum LET (denoted as critical LET or LET_{crit}) required to upset the bit-cell. The LET_{crit} is used to determine if SEU occurs in the struck memory cell. If the incident ion LET on the drain electrode surface is superior

to the LET_{crit}, an SEU is counted [40]. The critical LET can be used for SRAM memories and standard FFs instead of using the drift current model presented in section 5.2. It is a simplified upset criterion when compared to the drift current model.

Note that considering this critical LET, only a SBU can occur when an ion crosses a drain. This model assumes that the whole ion-induced energy is collected at one drain junction. This assumption is not valid for very integrated CMOS technologies for which many sensitive nodes can be impacted, and MCUs are common at medium to high LET valuesâ¢. The experimental results for 65 nm technology [83] showed that for high LET values, there are no more single bit upsets. Therefore, a new model was developed to improve accuracy of MCU prediction. Figure 2.8c shows that part of the ion-deposited carriers diffuse in the substrate [108]. The criterion was thus modified to take into account this phenomenon. For the struck drain, the critical LET is applied. Additionally, carriers generated beneath the funneling depth are subjected to diffusion and can be collected by neighboring drains, thus possibly upsetting these cells. For neighboring drains, SPICE or I_{max} = f(T_{max}) criteria are applied depending on the user's choice. The space charge region and funneling widths (Figure 2.8c) are given by the following equations [105; 109]:

$$W_{SCR} = \sqrt{\frac{2 \cdot \epsilon_{Si} \cdot V_0}{q \cdot N_A}} \tag{2.13}$$

$$W_{fun} = \frac{\mu_n}{\mu_p} \cdot W_{SCR} \tag{2.14}$$

where ϵ_{Si} is the electric permittivity of silicon, V_0 is the hit node bias, N_A is the acceptor doping concentration, $q = 1.6 \cdot 10^{-19}$ C, and μ_n and μ_p are the electron and hole mobilities. This criterion was compared to the simple critical LET to evaluate its interest in the next chapter.

8 Simulation outputs

Depending on the simulation options and type of the simulated environment, user has several options for result visualization and output content. Moreover, the number of additional debugging and data post-processing tools have been developed to facilitate code validation and data representation. The most common TIARA outputs are: Error cross-sections and Soft Error Rates.

In case of heavy ion simulation, TIARA computes the cross-section as a function of effective LET value. For this purpose, for each effective

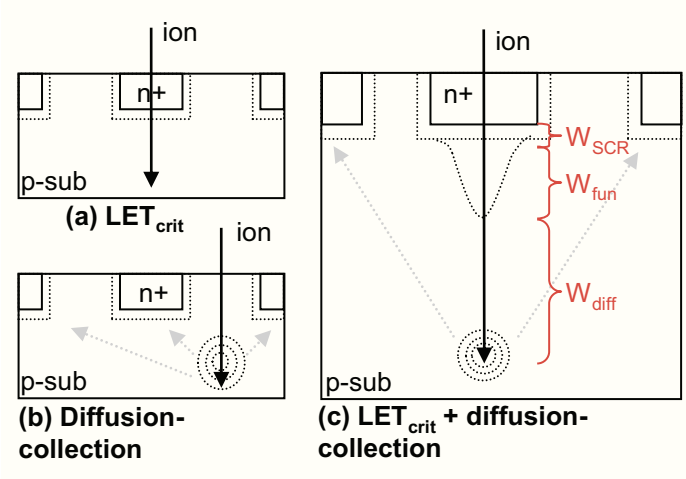

Figure 2.8: Modeling approaches of ion strikes in a SRAM memory: drain strike (use of simple LET_{crit} criterion (a)), ion strike outside the drain (use of diffusion-collection model (b)), and drain strike (use of new upset criteria: LET_{crit} + diffusion of carriers (c)).

LET value that is specified for the ion cocktail, thousands of ions are simulated. The simulated cross-section Equation 2.15 is derived from the cross-section computation for experimental tests and presented in Appendix 2 for which fluence is replaced by the quantity $Ion_{num}/Area$.

$$XS_{HI} = \frac{Area}{Cell_{num}} \cdot \frac{SEU_{num}}{Ion_{num}} \tag{2.15}$$

where $Area$ is the simulation area $Cell_{num}$ is the number of cells, SEU_{num} is the number errors found and Ion_{num} is the number of ions generated during the simulation. The resulting cross-section as a function of the effective LET value can then be directly compared to the experimental tests performed at a radiation facility.

In case of alpha or neutron simulations, TIARA gives directly the Soft Error Rate value. TIARA obtains the estimation of the Alpha and Neutron SER estimations from the following equations:

$$SER_{Alpha}[FIT/Mbit] = 1024^2 \cdot E_{package} \cdot \frac{Area}{Cell_{num}} \cdot 10^9 \cdot \frac{SEU_{num}}{Alpha_{num}} \tag{2.16}$$

$$SER_{Neutron}[FIT/Mbit] = 1024^2 \cdot Flux \cdot \frac{Area}{Cell_{num}} \cdot 10^9 \frac{SEU_{num}}{Neutron_{num}} \tag{2.17}$$

where $E_{package}$ is the package emissivity in $alphas{\cdot}cm^{-2}{\cdot}h^{-1}$, $Cell_{num}$ is the number of cells, 10^9 corresponds to conversion to FIT, SEU_{num} is the number errors detected during the simulation, $Flux$ is the integral

neutron flux for the considered neutron spectrum , and $Alpha_{num}$ and $Neutron_{num}$ is the number of alpha particles and neutrons generated during the simulation, respectively. The neutron flux is equal to 13 $n \cdot cm^{-2} \cdot h^{-1}$ for JEDEC spectrum when considering neutrons above 10 MeV and 26 $n \cdot cm^{-2} \cdot h^{-1}$ when considering neutrons above 1 MeV. These SER values are in FIT/Mbit.

Moreover, TIARA is capable of delivering very insightful analyses and graphics in addition to the cross-section and SER values. The SRAM memory layout can be generated without matrix dimension limitations and TIARA allows for MCU fail rate computations. An example of TIARA estimation of the MCU percentage occurrence of number of bit per radiation event for a SRAM designed and manufactured by STMicroelectronics are presented in Figure 2.9. Results given in this figure consider a memory matrix of 4 x 64 memory cells (i.e. 256 cells). These dimensions have been chosen first to assure good compromise with the test chip (well-tie contacts every 64 cells) and second, acceptable simulation run time.

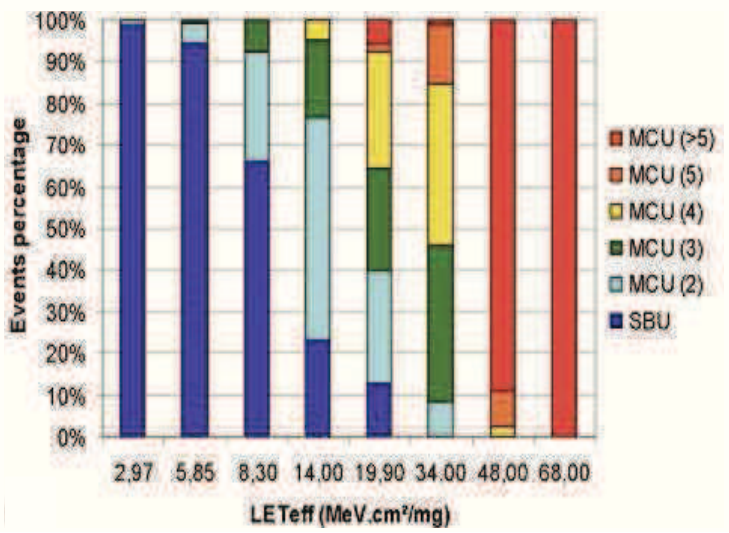

Figure 2.9: Example of TIARA simulated MCU percentage occurrence for a ST SRAM memory. SBU = MCU 1-bit, MCU(2) = MCU 2-bit, etc.

TIARA have the ability to plot Single Event Upset and Multiple Cell Upset bit-maps as a function of LET value that can be superposed on real layout of the simulated structure. This provides with a visual identification of the most sensitive layout areas.

Figure 2.10 illustrates the part of a layout from a simulation performed on a flip-flop architecture containing more more than 70 transistors. All off-state transistors are simulated and the TIARA results show the evolution of the sensitive zones as a function of particle LET. Such

information is extremely valuable from the designer's perspective and allows quick feedback on the cell architecture for hardening purposes.

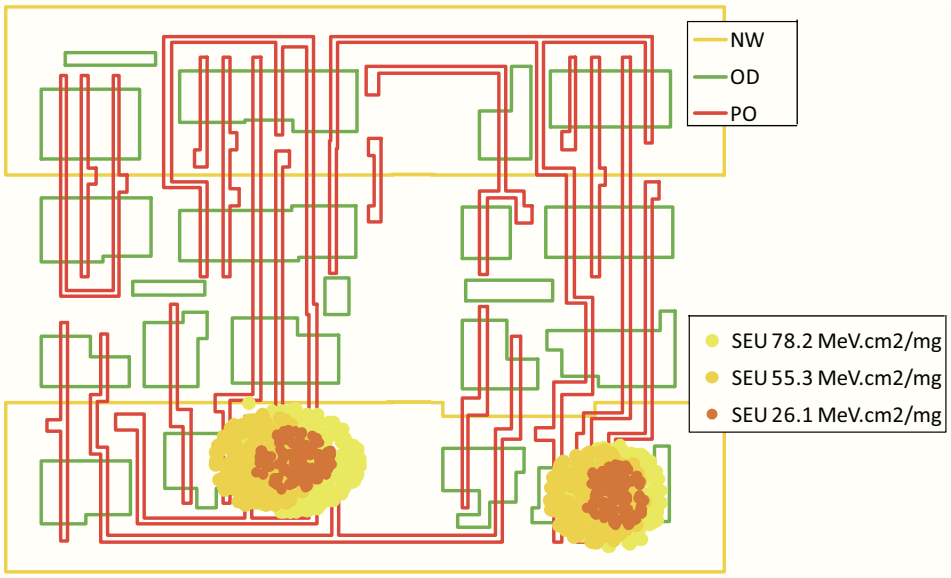

Figure 2.10: TIARA-generated Flip-Flop geometrical structure with active, poly and N-well areas obtained from the GDS file (all other layers have been removed). The yellow and orange areas superposed on the layout show the heavy-ion-induced simulated SEUs as a function of LET.

TIARA has been also coupled with the CERN's ROOT visualisation tool developed for GEANT4 [61] Figure 2.11. The simulated structure can be drawn in three dimensions and all reactions or ions can be tracked with all secondary products, impacting different regions of the structure.

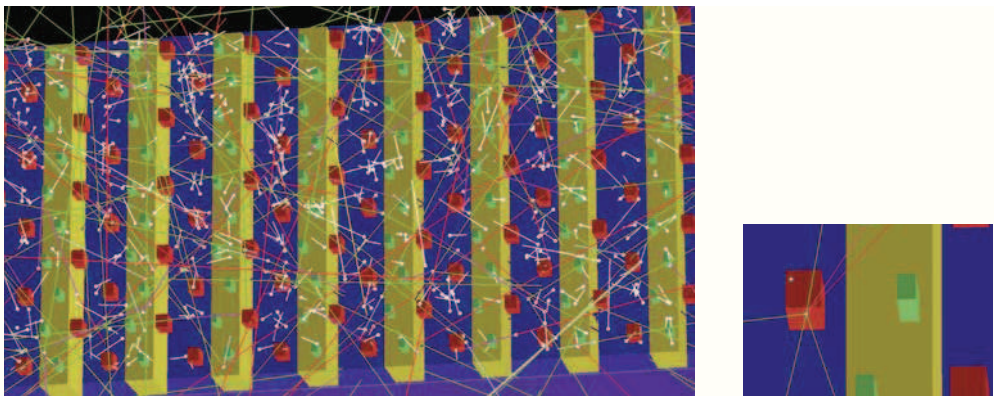

Figure 2.11: TIARA screenshot showing a part of a 20x20 memory cell matrix of a 65 nm SRAM curcuits under neutron irradiation. For clarity, only silicon recoil secondary ions inducing a SEU have been plotted. Also for clarity, Shallow Trench Isolation (STI) oxides have been removed. The Inset shows a detail of a reaction producing 6 secondary particles and impacting a NMOS drain (red box).

9 TIARA integration with the IC CAD environment

TIARA is developed in C++ and is dynamically linked with IC CAD flow through the coupling with a SPICE solver. TIARA also integrates a GDS parser and model parameters extraction methodologies from TCAD. The use of a LSF job scheduler and deployed on the STMicroelectronics' distributed system minimizes the simulation run time thus providing very fast feedback concerning cell sensitivity, weaknesses, allowing redesign and hardening that has not been available before.

This section presents briefly some technical aspects related to the TIARA implementation solutions.

9.1 GDS parser and dynamic link with SPICE engine

TIARA is coupled with two main design standards: a GDS file format describing the cell geometry and a SPICE engine for electrical cell simulation.

As presented in section 2, the structure creation in TIARA is based on GDS formatted data. A separate tool has been developed that extracts the necessary data from the GDS layout description. It parses the GDS file, obtains coordinate points of CAD layers and using geometrical computations tracks the positions and dimensions of the transistor active areas, cell dimensions, Nwell and Pwell shapes. Based on this information and additional data concerning the depth of the wells, junctions and STI regions (obtained from TCAD or SIMS measurements) TIARA creates a simplified 3D structure of the cell.

TIARA is dynamically coupled with a SPICE solver (ELDO [110]). During the simulation, the SPICE input files are prepared at the first time. They contain all node potentials, simulation options, initial conditions for a specific cell configuration that is simulated and all additional parameters as temperature, process corners, power supply voltage, etc. Then, TIARA instantiates the simulated cell using its netlist with parasitics and injects all radiation-induced perturbations in the corresponding circuit nodes. When input files are ready, the SPICE simulation is launched and after it finishes, TIARA extracts the information of an upset occurrence.

9.2 LSF use and parallelism on distributed system

TIARA uses full SPICE simulations for upset criteria, especially for RHBD FF simulations. Performing a large number of ion impacts using one

SPICE run for each ion strike to obtain sufficient statistics of SER estimation requires very long CPU run time. To decrease the simulation run time, TIARA has been adapted to be used on a distributed system via the (LSF) platform job scheduler [111; 112].

TIARA simulation flow presented at the beginning of this chapter (Figure 2.1) briefly depicts the strategy of the job dispatching. TIARA simulation core (let's call this task a controller) is run on one CPU. This controller employs Monte Carlo methods for the radiation events generation and preparation of the SPICE input files (*.cir) with circuit initial conditions, parasitic currents and circuit stimuli. Controller computations are repeated until the number of parallel SPICE simulations fills a job array whose dimensions are specified by user in TIARA configuration file.

In the second phase, the controller submits this job array on a distributed system together with the additional data gathering and analysis job. The latter job is run with a dependency condition and starts only if all previous SPICE simulations have finished. Its purpose is to post-process SPICE simulation log files and return all required information to the controller. The whole algorithm is repeated until all radiation events have been totally simulated.

Figure 2.12 presents the computations of the simulation run time and the speed-up factor as a function of number of the parallel jobs. The analysis was performed for parallel jobs number ranging from 1 to 200 leading to speed-up factor up to 43. The gain versus the number of jobs saturates because of the limitations in the communication between different tasks. The optimal number of parallel jobs is equal to 100 with a simulation acceleration of 39 as compared to the fully sequential SPICE simulation on one CPU. For TIARA neutron simulations of Flip-Flop architectures, the parallelism enables the simulation of approximately $2 \cdot 10^7$ neutrons per hour and the SER estimation converges to its final value in about 15 hours [113].

9.3 Running TIARA on Graphics Processing Unit

The standalone version of TIARA (using Imax=f(Tmax) upset criterion instead of SPICE simulation) has been also implemented to run on a Graphics Processing Unit (GPU). The diffusion-collection equations have been implemented in CUDA programming language allowing for parallelism on a NVIDIA Tesla C1060 GPU card. When analysing Equation 2.4 and Equation 2.5, the I(t) values given by the diffusion-collection equations are independent of each other, leading to a trivial parallelism on the discrete mesh values of time interval. A I(t) current pulse is evalu-

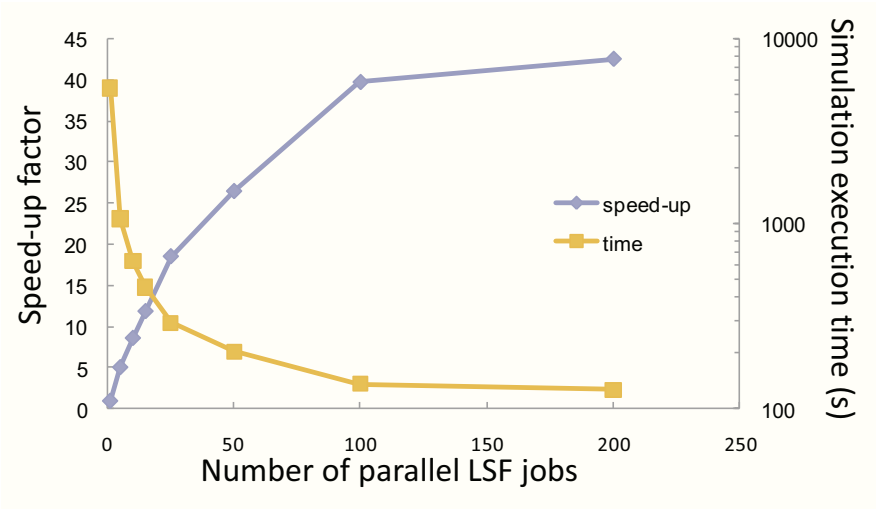

Figure 2.12: LSF speed-up factor thanks to SPICE simulation parallelism.

ated on 200 discrete time point ranging from 0.5 ps and following the geometrical progression with a 1.1 ratio, thus covering the complete time domain in all practical cases of ion strikes. The implementation details can be found in [114]

Then the diffusion-collection equation (Equation 2.4) is evaluated 200 times in parallel by the different CUDA threads. Additionally, the double integration on the drain surface electrode defined in Equation 2.5 is performed giving a total of 4305 floating-point elementary operations computed by different threads in parallel. At the end of computation the complete ion-induced current I(t) is returned to the controller task running on the CPU.

TIARA simulations have been performed on a Dell Precision T7400 workstation equipped with a NVIDIA TeslaTM C1060 GPU card [4] and with a CPU processor Intel XEONTM 5410 (2.33GHz). Simulation runs have been successfully performed with 1,000,000 generated alpha-particles. The comparison of global execution time data between he standard (CPU) and parallel (GPU) version of TIARA are shown in Figure 2.13(a). A total acceleration gain obtained by using the GPU is equal to about x10 and x30 when considering only the execution time dedicated to the calculation of the I(t) current. Figure 2.13(b) shows the respective contributions of the GPU calculations, data transfer between the GPU and the CPU and the rest of the program run on the CPU. More than 30% of the runtime is used for the CPU/GPU communication that limits the overall acceleration gain. Moreover, it is shown in [114] that a 53 gigaflops rate is reached for this implementation, that is well below the maximal GPU peak performance equal to 933 gigaflops.

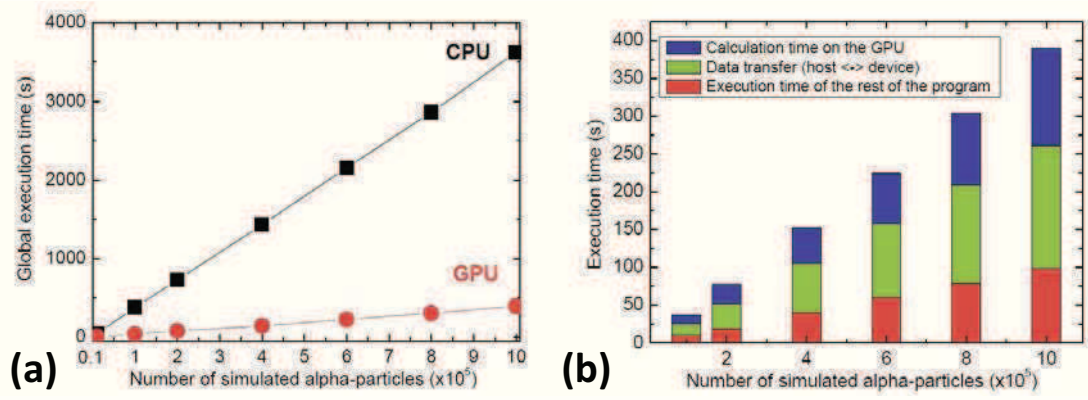

Figure 2.13: Execution time of the whole SER simulation as a function of number of generated alpha-particles: considered for both GPU and CPU implementations of the code (a) and showing the respective contributions of the GPU (communication+execution) and CPU execution time (rest of the program) [114].

10 TIARA modeling presision and uncertainties

Each estimation is characterized by its precision and is limited by uncertainties due to a certain number of assumptions. This section describes the precision and uncertainties for TIARA simulation. Then, the influence of model input parameter variations is studied and its impact on the cross-sections/SER simulations.

10.1 TIARA precision and upper limits

The precision of a simulation is its ability to reproduce the same results, i.e. a degree to which repeated measurements under unchanged conditions show the same results. TIARA simulates a large number of radiation events for each simulated environment obtaining an important statistic on error. For the results presented in this work, simulation error bars are smaller than 1% and are not shown in figures. When no upsets occur during the simulations, the upper limits at a 90% confidence level are drawn.

10.2 TIARA uncertainties

The uncertainty is a parameter that characterizes the dispersion of the value attributes and reflects incomplete knowledge of the estimated quantity. The sources of errors and uncertainties have to be evaluated for the correct interpretation of the simulation results. In the following paragraph, the sources of errors and uncertainties are analyzed and the

variations of main parameters that are the most critical for TIARA Soft Error Rate/cross-section estimation are quantified.

10.3 Uncertainties

According to [115], the sources of uncertainties while modeling of single events can be classified in three main groups:

- TCAD modeling uncertainties
- SPICE modeling uncertainties
- Rate prediction uncertainties

The following tables summarize the known possible uncertainty sources for TCAD modeling (Table 2.1), SPICE modeling (Table 2.2) and Rate prediction (Table 2.3). Each table contains the analyzed uncertainty in the first column, its major parameters in the seconde one, comments and the precision of the parameters in the third and fourth ones, respectively.

As far as TCAD simulations are concerned, six major uncertainties can be distinguished. The one that is the most difficult to quantify and influences significantly the TCAD simulation results is the accurate process modeling. All TCAD structures and device simulation results that are presented in this manuscript are based on the doping profiles adjusted with the particular STMicroelectronics manufacturing processes and are calibrated with the physical silicon measurements, thus their precision is extremely high. This is a great advantage that allows to use the 3D TCAD models as a reference while extracting the analytical transport models for TIARA. For device simulation, the proper physical models are used: doping dependent mobilities with high electric field saturation, appropriate boundary conditions are used. Ion spatial charge distribution is modeled with a Gaussian function and uses a constant LET value along the ion track.

The circuit modeling uncertainties are summarized in Table 2.2. The most critical is the estimation of ion-induced current pulse. Historically, the critical charge value was used for SEU analysis, however this approach, although very simple and easy to use, suffers from the lack of precision [116]. Similarly, the double exponential model does not offer sufficient precision of estimated current pulse. In this work, all transport models are directly extracted from TCAD simulations (drift current model for drain impacts, critical LET) or are based on TCAD-obtained physical data (diffusion-collection model for ions not crossing the drain junction). This approach allows for multiple solutions parasitic currents for the same critical value and give the realistic estimations of

TCAD modeling uncertainty	Major parameters	Comments	Uncertainty
Process accuracy	Junctions depths Substrate doping	Doping profiles adjusted with silicon electrical measurements	Very low
Models	Mobility models	Doping dependent e/h high electric field saturation	Very low
	Ion LET	Considered to be constant	Average
Parasitics	N-well collapse	Yes	Very low
Boundary conditions	Boundaries	Appropriate models for contacts (ex. ohmic contact model) All other reflective boundaries	Low
Coupling between adjacent devices	Multiple transistors affected by a single ion	Yes	Low
Loading	Charge collection is a function of field strength	Yes	Low

Table 2.1: Summary of the main identified TCAD modeling uncertainties.

the current shape. Coupling between devices is also taken into account and will be discussed in detail while charge sharing analysis (chapter 4). Concerning the electrical circuit's response to injected currents, TIARA uses the official ST Design Kits aligned with silicon and the post-synthesis cell netlists after parasitic extraction.

SPICE modeling uncertainty (TIARA)	Major parameters	Implementation	Uncertainty (Impact on SER)
Single event pulse	Accuracy of current model	Diffusion-collection model validated with TCAD	Average (high)
	Multiple solutions of Ipulse(t) for a given Qcrit	Yes, validated with TCAD	Low (high)
Models	Corners (PDK)	Yes, ST DK models	Very low
	Internal parasitics	Yes, netlist with parasitics	Very low
Coupling between adjacent devices	Coupling between adjacent nodes	Yes	Low (high)
State	Event time is random	Static conditions analyzed	n/a
	Possible internal states	Yes	Low

Table 2.2: Summary of the main SPICE modeling uncertainties.

From the rate prediction stand point, the ion transport and the ion disturbance have to be considered as the main sources of error. The alternation of back-end-of-line materials has been already evaluated in [40] and was proven not to influence the radiation sensitivity significantly (<5%). Critical for SEU rate prediction are the carrier transport parameters extracted from TCAD methodologies.

To summarize these results, the most critical for TIARA methodology is the generation of parasitic currents using diffusion-collection model. The model input parameters are the ambipolar diffusion coefficient, carrier collection velocities and carrier lifetime for both Nwells and Pwells.

Rate prediction uncertainty (TIARA)	Major parameters	Comments	Uncertainty (Impact on SER)
Transport	SEU rate as a function of Qcrit	n/a	n/a
	Alteration of material description	BEOL assumed to be composed of SiO2 only (verified in Ref. [34])	Average
	Sufficient statistics	Yes	Low
	Environmental variations	Yes	Low
Analytic Models	Appropriate	Diffusion-collection validated using TCAD simulations	Low
	What is parametric sensitivity on SEU rate?	Ambipolar diffusion coefficient, collection velocity, carrier lifetime	Low (High)
	Do model assumptions agree with the application?	Yes	Low

Table 2.3: Summary of the main SER/cross-section prediction uncertainties.

The influence of the variations of these parameters on the error rate predictions are quantified in the next section.

10.4 Influence of parameter variation on results

The influence of variations of the diffusion-collection model input parameters on heavy ion cross-section prediction is studied hereafter. Heavy ion TIARA simulations have been performed on a 65nm standard density SRAM with a LET value of 5 $MeV\dot{c}m^2mg^{-1}$. All parameters have been varied in the range between -50 and +50% of their nominal values. The variation of the heavy ion cross-section as a function of the parameter deviation are computed using the following formula:

$$\Delta XS = \frac{XS_{var} - XS_{nom}}{XS_{nom}} \cdot 100\% \tag{2.18}$$

where ΔXS is the cross-section variation, XS_{var} is the simulated cross-section after a parameter variation and XS_{nom} is the cross-section with nominal parameters. The influence on alpha and neutron SER remains the same as on the heavy-ion cross section because Neutron/Alpha SER can be derived directly computed from the cross-section value.

Figure 2.4 presents the cross-section variations as a function of the parameter variations for ambipolar diffusion coefficient in the well (a), carrier collection velocity via space charge region (b) and the ion excess carrier lifetime (c). While comparing figures (a) through (c), it can be seen that cross-section is the most sensitive to the carrier collection velocity parameter. When parameter v varies in the range +/-50%, cross-section variations are directly proportional. The velocity of the diffusion

defined by the D parameters causes smaller variations of the cross-section in the range of -5 to +15% for equivalent parameter variations (+/-50%). Interesting is the fact that this variation is not symmetrical. This can be explained by two mechanisms: first, for long single event transients, the cell feedback is capable of restoring the internal node bias and second, the recombination processes cause the decrease of the number of carriers thus limiting impact on the upset rate. Carrier lifetimes influence only very slightly the cross-section (<5%) without any visible trend.

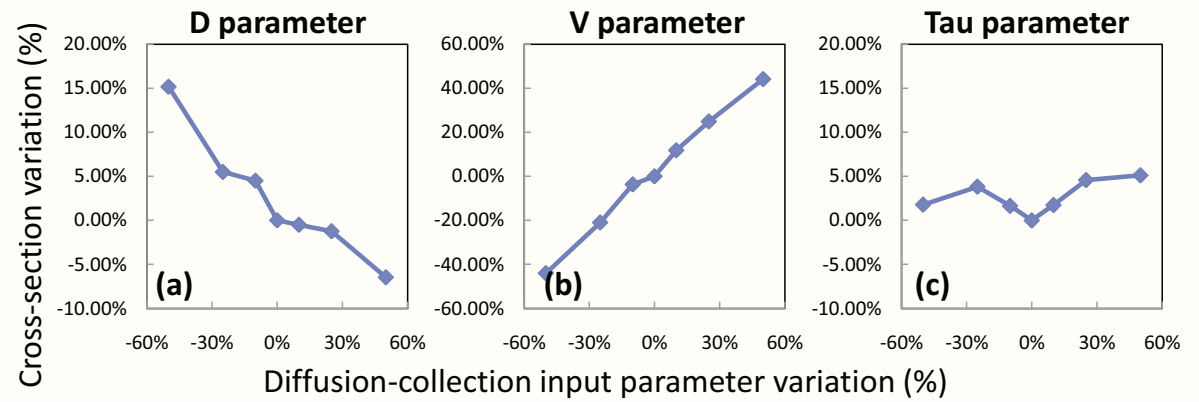

Table 2.4: Cross-section variation as a function of diffusion-collection input parameters: ambipolar diffusion coefficient (a), collection velocity via space charge region (b) and carrier lifetime (c).

However, it has to be kept in mind that the presented results are only specific for the 65nm standard density SRAM memory for ambient temperature, typical process corners and nominal Vdd voltage. The main model parameters have been studied and the value of v parameter influences the results most significantly. In addition, ambipolar diffusion coefficient and carrier lifetimes are based on computations using the process doping profiles that are extracted with very high precision. The v parameter is the most difficult to extract as the value of the electric field in the whole space charge region varies by 5 orders of magnitude.

11 Conclusion

In this chapter, TIARA simulation methodology was described in detail. New transport models and bit-flip occurrence criteria have been developed and an innovative coupling solutions between TIARA and IC CAD environment have been proposed to fulfil the platform requirements defined in section 1.9. Simulation precision and uncertainties have also

been assessed.

The following chapter will present a validation of main TIARA simulation features by comparison between simulation results and experimental tests performed on numerous STMicroelectronics' test vehicles dedicated for radiation characterization.

Chapter 3

Validation of TIARA radiation assessment and TIARA capabilities

1 Introduction

The previous chapter presented in detail Tool suIte for rAdiation Reliability Assessment (TIARA) simulation platform while in this chapter, extensive validation of simulation by comparison with experiments is performed for different radiation environments at different operating conditions (temperature, supply voltage). Single Event Effect mechanisms leading to upsets are analyzed.

Most of the presented results are based on Single-Port Register (SPREG) Static Random Access Memory that was manufactured in Bulk CMOS 65nm technology by STMicroelectronics. The memory bit-cell area is equal to 0.620 μm^2 and its operational supply voltage 1.2 V. TIARA estimations given in this paragraph consider a memory matrix of $4 \cdot 64$ cells (i.e. 256 cells). These dimensions were chosen first, to assure a good compromise with real test chip (well tie contacts every 64 cells) and second, an acceptable simulation run time. However, TIARA is capable of simulating the SRAM matrices with any dimensions.

All key parameters and criteria needed to perform the simulations have been extracted for this particular technology. The ambipolar diffusion coefficients D for both p-substrate and N-well, the average carrier velocities via space charge regions of NMOS and PMOS drains, carrier lifetimes, and the critical LET values for NMOS and PMOS transistor drains have been calculated using TCAD tools from the Sentaurus Synopsys package [89; 106]. The carrier recombination has been modeled by the carrier lifetimes in the p-substrate and in the N-well [105].

This chapter is organized as follows: section 2 presents most straightforward outputs as cross-sections and Soft Error Rate assessments. Section 3 shows different modeling strategies for prediction of Multiple Cell Upset rate. Finally, the additional TIARA modeling capabilities are discussed to which belong temperature, power supply and process corner influence on radiation sensitivity and handling additional architectures as different SRAM memory bit-cells, standard and Radiation-Hardened-By-Design Flip-Flops.

2 TIARA validation in different radiation environments

The major simulation capability of TIARA is the estimation of the simulated device cross-section and the Soft Error Rate in both space and terrestrial radiation environments. The accelerated and real time experimental test results are compared hereafter to validate the relevance of simulation approach.

2.1 Space environment through heavy ion cross-section simulation

As shown in section 1.1.1, the major threat to space-borne electronics are highly energetic heavy ions from GCR. To instigate their impact on circuits, the accelerated heavy ion experiments are performed in radiation facilities. TIARA reproduces the exact conditions during these tests (ion energy, beam direction, temperature, V_{dd} voltage) in order to be directly comparable with experimental results.

Extensive heavy ion tests were performed at RADEF (Radiation Effects Facility, Finland) [79] and UCL (Université Catholique de Louvain-La-Neuve, Belgium) [73] radiation facilities in compliance with the ESA test standard no 25100 [14].

Figure 3.1 shows the comparison of experimental and simulated heavy ion cross-sections.

A discrepancy between experimental and simulation results at lowest LET value is observed (2.97 $MeV\cot cm^2 \cdot mg^{-1}$). The error can be explained by the fact that it is caused by the ions striking in close proximity of drain junction which provoke upsets, thus increasing the cross-section. Since the simulation results at lowest LET show only SEUs due to drain strikes, these close to drain ions are not taken into account in the Monte-Carlo simulation, in which drain surfaces are strictly limited to those defined by the layout of the simulated structure. At high

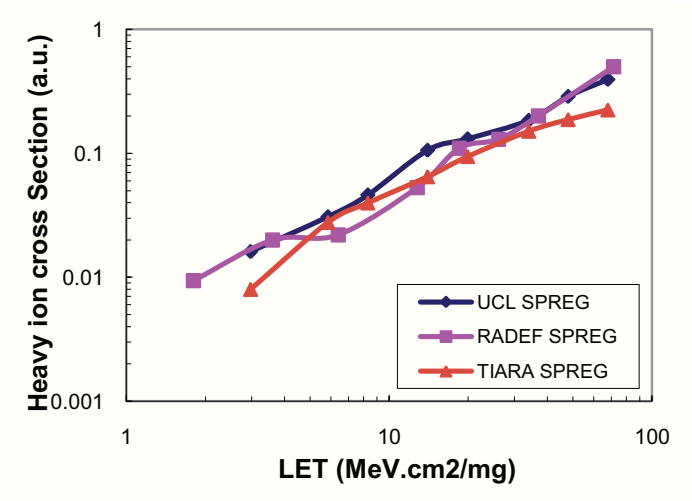

Figure 3.1: Simulated heavy ion cross-section as a function of the effective LET value and compred to the experimental tests performed at the RADEF and the UCL radiation facilities.

LETs (>40 $MeV \cdot cm^2 \cdot mg^{-1}$), simulated cross-section values are found lower than the experimental ones and tend to saturate causing an underestimation. According to [10] and investigated later on in [109], the main mechanism of SEU creation in the N-well is the parasitic bipolar effect, as the incident ion introduces important transient variations of the N-well potential. In the Psub region, those differences are much smaller since the substrate has a large volume. The bipolar effect is not yet accurately implemented in our simulation code, which explains this saturation. A model of bipolar amplification will be given in section 3.3.3.

Despite slight discrepancies at lowest and highest LETs, very good agreement is found between the simulated cross-section and experimental points for both radiation facilities, thus showing the relevance of TIARA assumptions.

2.2 Terrestrial environment through alpha SER simulation

Second ionizing source that can be handled by TIARA is alpha radiation (see section 1.1.2 for details).

Alpha experimental testings were performed at STMicroelectronics in Crolles with a ^{241}Am alpha source whose activity is equal to 3.7 MBq. During the tests the alpha radioactive source was placed on the open package at a distance lower than 2mm from the die. Geometrical cor-

rection factor was taken into account in both experiment and simulation [77].

In Figure 3.2, the TIARA simulation results are compared with the experimentations. Alpha simulations are in good agreement with the experiment with a reasonable underestimation of 14% of the simulated SER value. The alpha LET value for the bragg peak conditions is equal to $\sim$1.6 $MeV \cdot cm^2 \cdot mg^{-1}$ and at the same time, similar to the lowest LET value for the heavy ion experiments. This difference can be explained similarly to the discrepancy presented in the previous section that the number of ions striking in the close proximity of drain junction is underestimated. Nevertheless, the 14% offset between the simulation and experiment is low compared to experimental uncertainty reported in [12; 77]. The 14% difference can be related to underestimation of MCU percentage as shown in Table 3.1. Some rare Multiple Cell Events (4%) were recorded during alpha irradiation but simulation does not show these events.

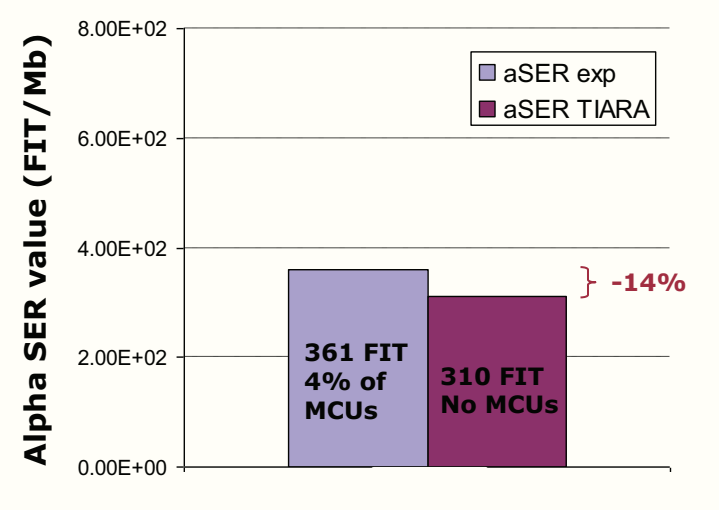

Figure 3.2: Simulated alpha Soft Error Rate compared with the experimental tests performed with the Americium alpha source experimental error bars has not been shown in figure for clearness (at 90% of confidence limit, error bars are inferior to 5%).

TIARA is able to provide information that is not accessible from the experiments. Table 3.1 summarizes some of the information that is obtained from the simulation. First, the contribution of NMOS/PMOS upsets in the total SER can be distinguished. For this memory all Soft Errors are attributed to the NMOS transistor as the critical LET value of the PMOS for this technology ($\sim$3.0 $MeV \cdot cm^2 \cdot mg^{-1}$) is higher than the maximal alpha LET. The direct drain ion strikes cause 87% of the total upset number and the ion strikes non-crossing the transistor drain are

the cause of 13% of errors.

Good agreement between simulation and experimental tests validates TIARA simulation approach for low LET ionizing radiation and additionally ion generation in random direction contrary to heavy-ion experiments where the ion beam is produced in a particular direction.

	TIARA sims		EXP measurement
Alpha SER value	310		361
MCU percentage	0%		4%
MOS type	NMOS 100%	PMOS 0%	N/A
Ion strike in junction	Yes 87%	No 13%	N/A

Table 3.1: Detailed synthesis of simulation and experimental test results.

2.3 Terrestrial environment through neutron SER simulation from accelerated or real time experiments

Neutron radiation is the third radiation type which impact on circuit behavior can be assessed by TIARA. As an example the real time neutron experiments are used for TIARA validation.

Real time testing on the ASTEP platform (see section 1.4.1 for details) has been compared to TIARA neutron simulations. The test system is composed of 384 identical test vehicles containing 8.5Mbit of 65nm static SRAMs (total of 3.3 Gbit). The hardware and software components of the test platform were designed to follow the JEDEC specification JESD89A [12]. Special test algorithms have been developed to distinguish the SBU and MCU. The main features of the experimental tests are summarized in Table 3.2.

TIARA Neutron simulations have been carried out for comparison purposes with the experimental characterizations. For the simulation, the atmospheric JEDEC neutron spectrum has been used [117] to simulate neutron-silicon interactions in the simulated structure. The nuclear events were generated by TIARA for a total of 500 milion simulated neutrons.

Figure 3.3 presents the comparison between the simulation and the experimental measurements. An excellent agreement is found between the simulation neutron Soft Error Rate and the value obtained experimentally (259 FIT vs. 260 FIT). Moreover, the MCU percentage for both

	EXP measurement
Duration	18 months
DUT Mbits	3.3Gbits
Event/bit-flips number	61/97
SBU number	44
MCU/MCU flips number	17/53
SBU/MCU SER (FIT/Mbit)	192/74
MCU percentage	54.6%

Table 3.2: Summary of main experimental test conditions and test results [69].

approaches is very close, thus validating the neutron-silicon reaction databases compiled from G4 simulation, TIARA simulation for medium LET values (ranging between sin4 and sin13 $MeV \cdot cm^2 \cdot mg^{-1}$) and TIARA estimation of MCU percentages.

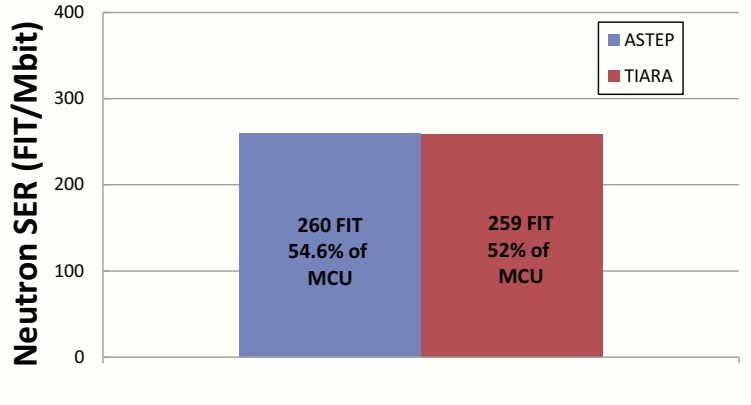

Figure 3.3: Simulated neutron Soft Error Rate compared with the experimental tests performed at ASTEP.

2.4 Insight in SEE effects

For all simulated radiation environments simulated and assessed in previous sections (heavy ions, alphas and neutrons) the different upset mechanisms are analyzed in this section. First, upsets due to diffusion processes and due to direct drain strikes are distinguished and second, the Nmos and Pmos contributions in total upset rate are discussed. Such information is not accessible from experimental tests and is a complementary information that can be assessed using the simulation approaches.

Figure 3.4 distinguishes upsets induced by the ions impacting directly the off-state junction and upsets due to charge diffusion mechanisms. When comparing upsets for alpha and neutron irradiation, it becomes clear that different mechanisms lead to SEU in both cases. For alphas most of the SEUs are induced by direct drain impacts and only 13% is due to diffusion from strikes in very close proximity to the drain junction. For neutrons, however, diffusion mechanisms play a dominant role (65-85%) depending on the reaction type. This situation explains low MCU rates for alphas and much higher MCU rates for neutrons (up to 7-8 cells impacted by the same ion).

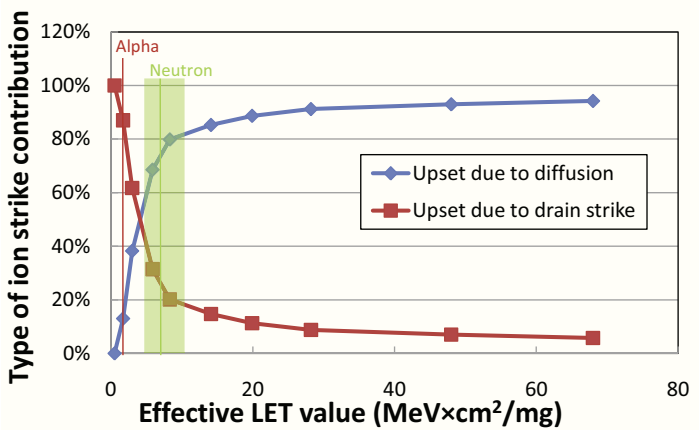

Figure 3.4: The contribution of upsets due to diffusion processes and due to drain strikes in the total upset rate as a function of the effective LET value.

The contribution per transistor type to total upset rate is presented in Figure 3.5. In this case, upsets induced by alpha particles are caused by ions striking Nmos transistor drain. This situation was correlated with full 3D TCAD simulations and it was found that the critical LET value for Pmos transistor for this particular memory is equal to 2.9 $MeV \cdot cm^2 \cdot mg^{-1}$, i.e. much higher than alpha maximum LET in silicon. The simulation done for 3.0 $MeV \cdot cm^2 \cdot mg^{-1}$ shows instant change of the Nmos/Pmos contribution ratio to 76/34% that is close to the ratio between Nmos/Pmos drain surface. For the neutron radiation, the Nmos contribution is the highest and ranges from 80 to 90%. These results show the interest to harden the Nmos transistor on the device level with the highest priority. According to [93; 118], the charge collection and charge sharing of ion-induced charge is present especially in the substrate and is much less important in the Nwell, thus confirming the TIARA simulation. The hardening technique using guard-diodes placed near Nmos transistors can be used and has shown its effectiveness in [119].

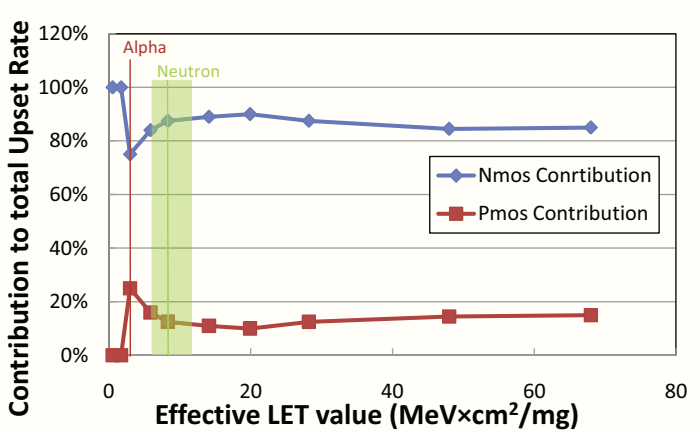

Figure 3.5: The contribution of transistor type contribution (Nmos/Pmos) as a function of the effective LET value in total upset rate.

3 TIARA assessment of Multiple Cell Upsets

In addition to the cross-section and Soft Error Rates, TIARA allows obtaining the MCU counting and estimation of MCU fail rates/percentages. The different MCU modeling strategies are presented in the next paragraph followed by MCU percentage analysis for different environments. Then, the influence of triple-well process option on SER and the modeling of parasitic bipolar amplification, which is necessary for simulation of structures implementing triple-well, are discussed.

3.1 Different modeling strategies for Multiple Cell Upsets

The different upset criteria presented in section 2.7 are evaluated in details and their impact on MCU rate estimation for heavy ion irradiations is analyzed. Three modeling approached have been proposed [88]:

- A critical LET value for ions crossing the drain junction and ImaxTmax upset criteria for ions not crossing the drain junction denoted as Sim1. This approach was also used before for simulations of SRAMs in 130nm [106] and 90nm [120] technology.
- New refined model accounting for diffusion of carriers beneath funneling depth for ion impacts in the drain junction and ImaxTmax upset criteria for ions not crossing the drain junction denoted as Sim2.
- The same new refined model accounting for diffusion of carriers beneath funneling depth for ion impacts in the drain junction plus a full SPICE transient simulation for each drain in proximity of ion impact denoted as Sim3.

The results of MCU counting as a function of simulation approach are compared to the experimental measurements are presented in Figure 3.6. When examining Exp, Sim1 and Sim2, it can be seen that the refined model for ion impacts in the drain, which takes into account the funneling phenomena, allows increasing the accuracy of SEU prediction by about 7% when compared to former criterion. The new model was retained in the simulator as the upset criterion for ions crossing the drain. Further comparison of Exp, Sim2, and Sim3 shows that the simulated results with SPICE were additionally enhanced (improvement by about 10%). It is noteworthy that the use of the SPICE simulation gives significant improvement in the MCU occurrence rate; however, the execution time increases by factor x100. The MCU percentage prediction has been improved in total by ≈17% by using the refined models, the rest of the results in this chapter employs the most accurate modeling approach.

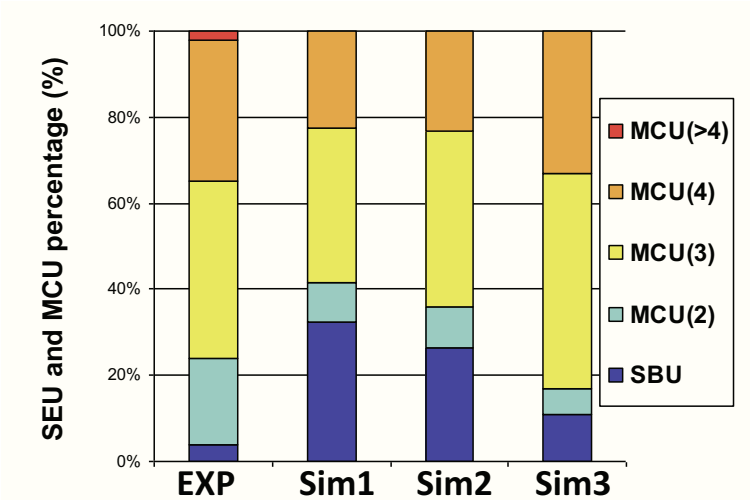

Figure 3.6: MCU occurrence for LET = 34MeV.cm2/mg. Exp stands for experiments at UCL, Sim1 stands for simulation with critical LET criteria and ImaxTmax, Sim2 stands for refined model (critical LET + diffusion for ion crossing drains) and ImaxTmax, Sim3 stands for refined model (critical LET + diffusion for ion crossing drains) and full SPICE simulation for ions not crossing the drain junction.

3.2 MCU percentages assessment

The most accurate modeling approach has been chosen to estimate the MCU percentages, i.e. the new refined model accounting for diffusion of carriers beneath the funnelling and full SPICE simulation as an upset criterion. Based on the TIARA simulation, the MCU percentage contribution in the total number of upsets and MCU fail rates can be computed using the following formulas:

$$MCU(\%) = (1 - \frac{SBU_{num}}{Flip_{num}}) \cdot 100\% = \frac{\sum_{i=2}^{n} i \cdot MCU_i}{SBU + \sum_{i=2}^{n} i \cdot MCU_i} \cdot 100\% \quad (3.1)$$

$$MCU(failrate) = SER - SER_{SBU} \quad (3.2)$$

where SBU stand for the Single Bit Upset number, MCU_i is the number of the MCU impacting i cells, SER is the total Soft Error Rate and SER_{SBU} is the Soft Error Rate due to Single Bit Upsets. The MCU percentage computations have been done for all types of radiations: alpha particles, neutrons and heavy ions.

TIARA-obtained values of MCU percentages for heavy ions, alpha particles and neutrons as a function of effective LET are compared with the experimental tests and are presented in Figure 3.7. The Alpha MCU percentage is traced for the LET value corresponding to the maximum alpha LET (Bragg peak condition). A range of effective LET values of secondary products of nuclear neutron-silicon reactions has been extracted for GEANT4 JEDEC reaction database. Only secondary ions with the atomic number higher than 2 and the initial energy after the reaction higher than 1 MeV have been considered in this computation. The extreme values of this range are 4.1 and 12.6 and the median value is equal to 7.4 $MeV \cdot cm^2 \cdot mg^{-1}$ (shown in Figure 3.7). As it can be seen, both neutron-induced and alpha particle induced MCU percentages match very well with the heavy-ion data. The experimental heavy ion MCU percentages match very well the MCU percentages obtained with TIARA, confirming the validity of models presented in section 3.3.1

3.3 TIARA vs. TCAD MCU rates

Additionally, TIARA plots Single Event Upset and Multiple Cell Upset cartographies as a function of LET value. These SEU/MCU can be superposed on real layout of the simulated structure. A simulated mapping of double MCUs as a function of LET is presented in Figure 3.8(b) and compared to TCAD simulations performed by Giot on two memory cells in a row [121]. The location of ion impacts causing the double MCUs is found to be the same for both modeling approaches, the most sensitive MCU(2) location are sources of pull-up and access Nmos transistors. Moreover, the same trends as a function of LET are observed in figures (a) and (b): as the incident ion LET increases, the sensitive area rises as well. The drawback of the simulation approach using TCAD is its run

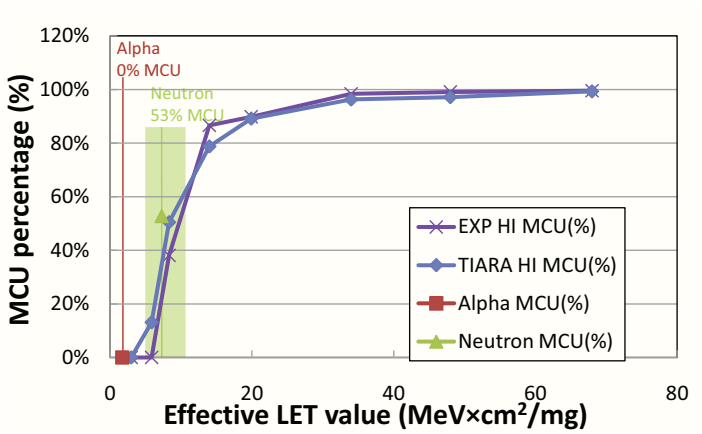

Figure 3.7: Percentage of MCU for different radiation environments: alpha, neutrons, heavy ions obtained by TIARA simulation.

time. Simulating one ion impact in an SRAM cell takes 1-2 days depending on strike position, whereas TIARA Monte-Carlo simulation gives full results over the LET range with mapping plots in hours for thousands of ion impacts and for a memory matrix (4 x 64 cells in this case). The simulation execution time is given for the state-of-the-art 64-bit multiprocessor systems. In addition to good agreement with experimental measurements, TIARA results are in very good agreement with TCAD.

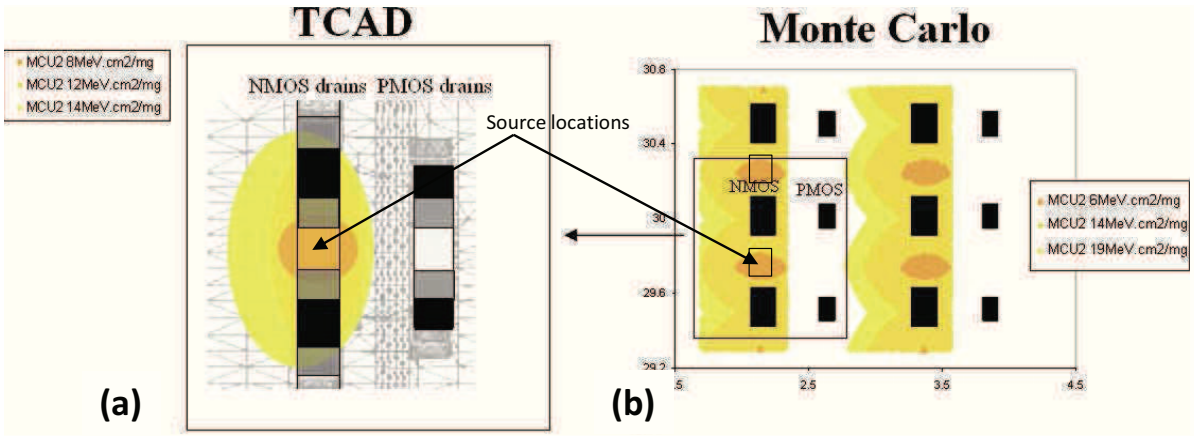

Figure 3.8: Mapping of TCAD simulated double MCU spread as a function of LET in NMOS and PMOS [121] (a) and simulated double MCU spread as a function of LET in NMOS and PMOS (b). Black rectangles represent sensitive drains.

3.4 Modeling of bipolar amplification and simulation of triple-well process option

The triple well layer is used as a standard technology option in order to reduce noise from the substrate (high interest for radio frequency CMOS components), lowers current leakage because of the Pwell electrical isolation and suppresses the Single-Event Latch-up [122; 123]. ST technologies implement Deep-Nwell (DNW), i.e. a buried N+ layer that is biased to V_{dd} through Nwells.

On the other hand it increases the parasitic bipolar amplification and finally the SER. Lack of the bipolar amplification model is a limitation to existing Monte-Carlo simulation approaches. TIARA shows a very good comparison with experimental results for structures without triple-well layer for which bipolar amplification is not significant. However, for structures with triple-well layer this bipolar amplification influence has to be taken into account. This section presents the analytical bipolar model that can be coupled with TIARA.

Triple Well effect on the Single-Event Latch-up

Figure 3.9 (after [10; 122]) explains the mechanism of SEL creation in the CMOS inverter with and without DNW. In the initial twin-well structure, the well resistances between well ties (R_{NW1} and R_{PW1}) can be sufficiently high to create a voltage drop along the well after an ion strike and as a consequence trigger the parasitic thyristor inherent to CMOS process (a). The use of highly doped N+ burried layer whose resistance is much lower than Nwell resistance without DNW ($R_{NWell} \ll R_{NW1}$) eliminates the parasitic PNP structure, thus the latch-up effect (b).

Charge amplification caused by Triple Well

On the other hand, as presented in Figure 3.10, the use of DNW isolates the Pwells from the substrate, lowering the well cross-section and as a result increases the $PW1$ resistance considerably (factor about x3). This well resistance increase causes much higher voltage drops in the Pwell after radiative events [121]. If the well bias disturbance is high enough, the transistor sources start injecting the electrons in the Pwell which are finally collected by the off-state drains thus increasing the total collected charge in the circuit node [122]. This mechanism is described more often as a parasitic bipolar amplification.

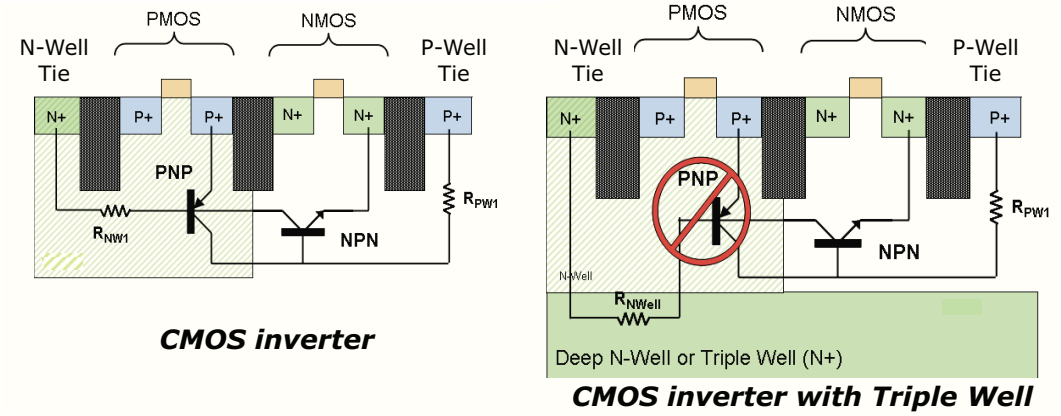

Figure 3.9: Schematic cross section of a CMOS inverter without deep-Nwell (a) and with deep-Nwell (b). The PNP transistor is suppressed and cannot be triggered because of the much lower R_{Nwell} resistance when compared with the structure without DNW [122].

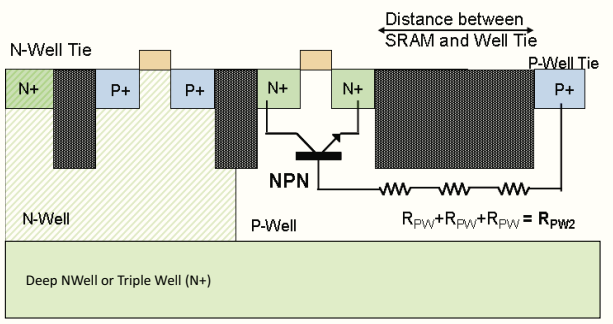

Figure 3.10: Schematic cross section of a CMOS inverter with dee-Nwell. The DNW isolation lowers the Pwell cross section, thus increasing the well resistance. This increases the NPN base resistance R_{PW2}. The NPN trigerring is facilitated [122]

Bipolar amplification model integrable with TIARA

Physical phenomena leading to parasitic bipolar action can be described in two stages: first stage is the voltage drop in the well studied by [121] and the second one is the reaction of the SRAM cell on this voltage drop [122]. Analytical models have been introduced for both phenomena that could be taken into account while simulating the SRAM memories with deep-Nwell with TIARA.

Device simulation is used to obtain the ion voltage disturbance in the well between the nearest well-ties by solving the Poisson's and the current continuity equations on the 3D TCAD model [124]. The well voltage variation obtained from device simulation is then injected into the circuit-level simulation. Finally, the voltage variations cause bipolar action in the SRAM cell leading to soft error. The major drawback of this approach is the voltage disturbance extracted from device simulation.

This disturbance strongly depends on the well-tie frequency [125] and the distance between the ion strike and the well-ties.

In this work, to obtain the ion-induced voltage perturbation, it is proposed to use TCAD simulation to extract the ion-induced majority current as a function of time in the location of ion strike. The majority carriers while diffusing in the well cause the voltage drop. This phenomenon can be modeled using the resistance-capacitance chain (also used by Osada [124]). The well square resistance and capacitance values can be found directly in manufacurer's Design Rule Manuals (DRM). The voltage variations as a function of time for each SRAM bit-cell between the well-ties can be obtained from normal RC chain circuit SPICE simulation using these R, C values and the ion-induced majority carrier current pulse.

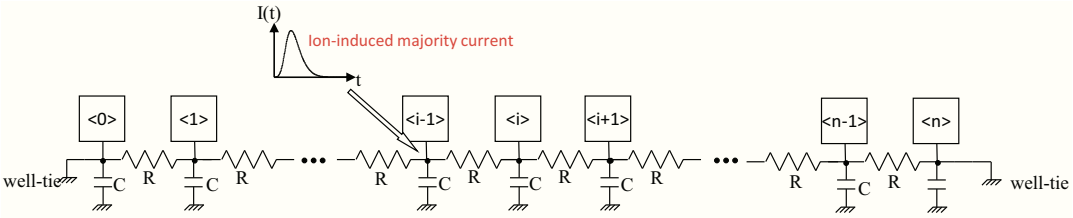

Figure 3.11: The equivalent RC chain for the propagation of the ion-induced majority carrier current. This circuit allows for obtaining the voltage variation as a function of time and as a function of the distance to the nearest well-tie (inspired from [124]).

Then, this voltage drop, just below each SRAM cell, can be used to model the injected current by the transistor source and finally the collected current at the drain electrode. Full 2D TCAD simulations for Pmos not isolated with DNW and Nmos transistors isolated with DNW (the worst cases from the bipolar amplification stand point) have been done as a function of well bias. The results are presented in Figure 3.12(a). This drain current function as a function of well bias can be used for estimation of current collected by drain due to bipolar amplification Figure 3.12(b). The voltage controlled current source is injected in the SPICE netlist that is controlled by the well bias. This current is injected in addition to ion-induced current pulses from diffusion-collection equations or from the drift current model (in case of drain impact).

This model is integrated with TIARA. All the required model information is obtained from DRM specification or using TCAD simulations. TIARA is already coupled with the SPICE engine, and the additional current pulses due to bipolar action is injected in addition to other ion-induced currents. While this model is integrated, it has not yet been validated. Next TIARA releases envisage the validation of model with experimental data to reproduce MCU patterns observed for different

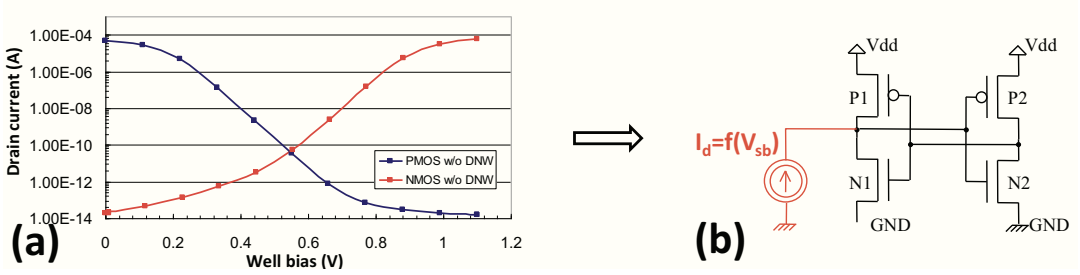

Figure 3.12: The TCAD extracted drain currents for a Nmos and Pmos transistors as a function of the well bias (a) and the bit-cell equivalent circuit with a bipolar amplification current model (b).

radiation environments for structures with DNW.

4 Investigation of TIARA capabilities

TIARA modeling capabilities include simulation of radiation sensitivity for different circuit operating conditions as temperature, power supply voltage to be able to emulate the circuit operation in real time conditions. Additionally, different process corners can be simulated to account for the radiation sensitivity variation between different components as a function of the process variability. At the end of this section, TIARA simulations for several different circuit architectures are presented that proves that the approach can be applied to practically each digital cell. All available experimental characterizations are compared to the TIARA simulation results.

In this section, unless otherwise stated, the results apply to a new high-density SRAM memory with 0.149 μm^2 bit-cell area and designed and manufactured in the 32nm CMOS process. For all possible parameters, the TIARA results are compared with experimental radiation tests. The ambipolar diffusion coefficients D for both p-substrate, N-well and the average carrier velocities via space charge regions of Nmos and Pmos drains, carrier lifetimes, and the critical LET values for Nmos and Pmos transistor drains have been analytically extrapolated for ST 32nm technology from the previous technological nodes (CMOS 130nm down to CMOS 45nm technology). All parameters for previous technology nodes have been calculated using full 3D TCAD simulations of ion strikes from the Sentaurus Synopsys package [106]. For the 32nm technology, as of the day of this thesis, the reliable doping profiles were not available. The upset criteria use either full SPICE simulation of the bit-cell netlists with parasitic extraction and transistor models from ST Bulk 32nm LP PDKs for each radiation event for both Nmos and Pmos transistors or SPICE pre-processed Imax=f(Tmax) upset criteria.

4.1 Effect of temperature range from -40°C to 125°C

The previous studies [123; 126; 127; 128] show that Upset rate is temperature dependent. The overall trend is the increase of the SEU rate with the temperature increase. Previous works [129] classify temperature impact on the SRAM memory response to radiations in two main groups:

- first, by affecting the transport properties of the charge generated by ionizing particle passage through the silicon
- and second, by the variation of cell electrical characteristics.

TIARA is used to assess SEU as a function of temperature following these two groups.

Charge transport as a function of temperature

All technological parameter values (ambipolar diffusion coefficients, carrier collection velocities, and carrier lifetimes) have been computed at different temperatures.

The ambipolar diffusion coefficients D parameters for initial ambient temperature were calculated using Sentaurus Synopsys 3D TCAD models and doping profiles adjusted with the ST technology process. D coefficients can be computed using the Equation 2.7. Assuming that in strong injection $n \approx p$ and employing the Einstein's relations Equation 2.8, Equation 2.9, ambipolar diffusion coefficient can be calculated as follows:

$$D \approx \frac{2 \cdot D_n \cdot D_p}{D_n + D_p} = 2 \cdot \frac{k \cdot T}{q} \cdot \frac{\mu_n \cdot \mu_p}{\mu_n + \mu_p} \tag{3.3}$$

where k is the Boltzmann constant equal to $1.38{\cdot}10^{-23} m^2 \cdot kg \cdot s^{-2} \cdot K^{-1}$, T is temperature in K, q is the elementary charge equal to $1.6{\cdot}10^{-19} C$, μ_n and μ_p are the electron and holes mobilities in $cm^2 \cdot V^{-1} \cdot s^{-1}$, respectively. According to [130], the carrier mobilities are functions of temperature and doping concentration in silicon, as follows:

$$\mu_n = 88 \cdot T_n^{-0.57} + \frac{7.4 \cdot 10^8 \cdot T^{-2.33}}{1 + [N/(1.26 \cdot 10^{17} \cdot T_n^{2.4})] \cdot 0.88 \cdot T_n^{-0.146}} \tag{3.4}$$

$$\mu_p = 54.3 \cdot T_n^{-0.57} + \frac{1.36 \cdot 10^8 \cdot T^{-2.23}}{1 + [N/(2.35 \cdot 10^{17} \cdot T_n^{2.4})] \cdot 0.88 \cdot T_n^{-0.146}} \tag{3.5}$$

where T_n is equal to $T/300$. The above equations determine the ambipolar diffusion coefficient in the well as a function of temperature and doping concentration. The variations of ambipolar diffusion coefficients as a function of temperature for both well types (Nwell and Pwell) have been obtained by using a fixed doping concentration while varying the temperature.

The collection velocity depends mostly on space charge region (SCR) width and power supply voltage. In [129], it is assessed that SCR width variation is limited to ∼5% for temperature ranging from 25°C to 125°C. In this study, it is considered that the collection velocity varies in the same way as the SCR width. Electron and hole lifetimes in the wells depend mostly on the doping concentration and do not vary with the temperature. However, for the unchanged carrier lifetimes and because of the variation of the diffusion constant the average diffusion length changes.

Variations of electrical cell characteristics

Additionally, TIARA takes also into account the temperature effect at bit-cell level. The behaviour of the cell transistors is modeled using SPICE simulations and transistor PDK models that are certified over a large temperature range. The transistor model parameters as a function of temperature are very precise thanks for the calibration with silicon electrical measurements.

To model cell electrical behavior varaition with temperature in TIARA, two possibilities are available: one is to compute the Imax=f(Tmax) abacuses at different temperatures. The second one is the use of full SPICE simulation as an upset criterion. Figure 3.13 shows a variation of NMOS transistor drain current as a function of V_{DS} voltage simulated using SPICE and ST PDK models. It is clearly seen that the drain current decreases with the increase of the temperature. This can be explained by electrons/holes mobility decrease, thus decrease in transistor drive current, and finally resulting in a lower capability of restoring nodal voltage after a disturbance.

Results

Figure 3.14 shows TIARA assessment of heavy ion cross-section variation as a function of temperature compared to the experimental variations collected at the RADEF for ion with the 37 $MeV \cdot cm^2 \cdot mg^{-1}$. This LET value has been chosen to maximize cross-section variations and to be able to compare variations to the measurements reported in the

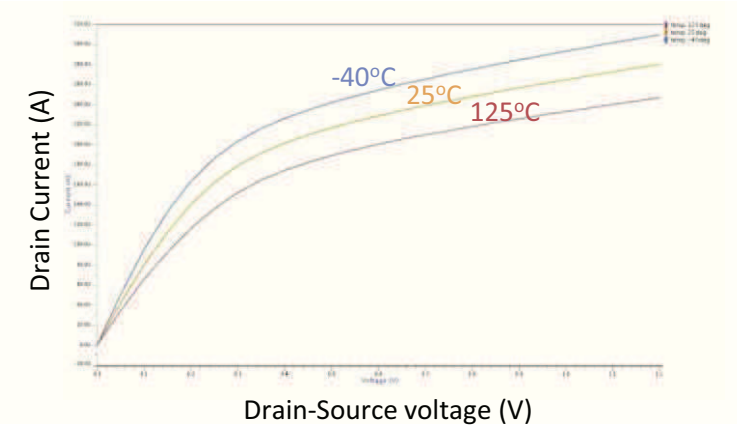

Figure 3.13: NMOS transistor on current (V_{DD} voltage applied to the gate) as a function of drain-source voltage for different temparatures (-40°C, 25°C and 125°C).

literature [123] that were reported for cross-section values at saturation. The cross-section was normalized to 100% at ambient temperature. The variation is equal to about 30% at 125°C and -24% at -40°C. Although during the radiation measurements the temperature influence of the SEU cross-section has not been tested, similar results have been reported in [123] for ST 65nm CMOS technology. Reported increase of heavy ion cross-section is around 32-40%. The TIARA temperature cross-sextion/SER assessment can be done for any environment and any device.

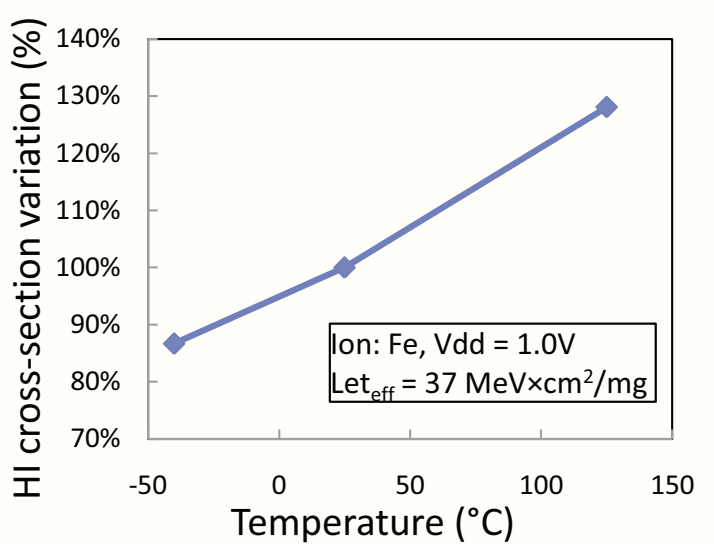

Figure 3.14: Simulated heavy ion cross-sections as a function of temperature (single-port high-density SRAM memory) normalized to ambient temperature.

4.2 Effect of supply voltage

In a small range of power supply voltages, it can be considered that power supply only marginally modifies the ion-induced charge transport in a semiconductor structure, whereas as for extreme power supply voltage variations the charge collection efficiency varies significantly and collection velocity parameter has to be computed as a function of the applied voltage. This section is divided in two paragraphs: one analyzes the variation of heavy ion cross-section for 32nm SRAM memory for small V_{dd} variations while the second one analyzes the radiation sensitivity of a SRAM cell optimized for operation in a very large operation voltage range.

Small variations of supply voltage around nominal value

For small V_{dd} voltage variations, mainly the electrical cell response are impacted as both the ability of forward-biased NMOS/PMOS transistors to restore the nodal voltage after an ion strike increases as well as the amount of charge used to store a logical value increases according to the formula proposed by Roche et al. [82]:

$$Q_{crit} = C_n \cdot V_{dd} + t_{flip} \cdot I_{restore} \tag{3.6}$$

where C_n is the total struck node capacitance, t_{flip} is the flipping time, and $I_{restore}$ is the restore current. In order to analyze the power supply effect on heavy ion cross-sections by TIARA, the SPICE simulation is run with different power supply voltages (alternatively Imax=f(Tmax) characteristics are recalculated for different power supply voltages when used as an upset criterion). Transport parameters remain unchanged. Figure 3.15 shows the heavy ion cross-sections as a function of V_{dd} voltage. As it can be seen, the simulated increase (decrease) of the power supply voltage by 0.1V results in decrease (increase) of the cross-section by about 15% while experimental data show a typical variation of 10%.

TIARA capacity to handle extreme voltage variations

TIARA simulations have been compared to the experimental radiation measurements carried out on 65nm CMOS memory with an Ultra-Low Voltage (ULV) optimized 10-transistor bit-cell designed to be operational thought the extended power supply voltage range from 0.35 to 1.2V [131]. The memory was tested with a radioactive alpha source of 3.7 MBq activity. The design-of experiment included complete range of operational V_{dd} voltages.

Figure 3.16 shows the variation of alpha Soft Error Rate as a function of supply voltage for this ULV SRAM. Experimental measurements

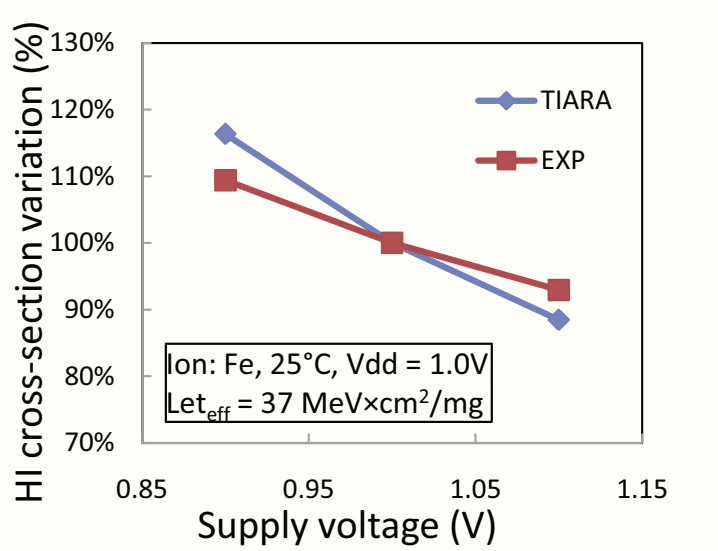

Figure 3.15: Simulated heavy ion cross-sections compared to experimental ones as a function of power supply voltage (single-port high-density SRAM memory) normalized to nominal voltage equal to 1.0V.

show the SER increase by factor x7 at 0.35V compared to the nominal voltage. For the voltage range between 1.2V down to 0.7V, TIARA simulations are in very good agreement. However, for the voltages below 0.7V, an overestimation of the alpha SER is observed confirming that for relatively small variations of V_{dd}, technological parameters do not change significantly and give accurate SER estimations. Transport model parameter imitation for lower voltages is attributed to a change in carrier collection efficiency via the space charge region of the junction. For low voltages, the space charge region depth is decreased and carriers are collected at smaller velocity because of weaker electric field. The supply voltage does influence neither diffusion processes nor carrier lifetimes.

The second set of TIARA simulations (denoted in Figure 3.16 as TIARA new v) with changed v parameters have been performed and shows an excellent match with the experiment. In section 2.9.3, the influence of input parameters on SER estimations has been presented. As shown in Figure 2.4(b), the SER variation is directly proportional to variations of v, thus, collection velocity for both Nmos and Pmos transistors have been changed according to a difference between experimental (EXP) and simulation results (TIARA) shown in Figure 3.16. Using the obtained values of collection velocities as a function of Vdd voltage, a model presented in Figure 3.17 has been extrapolated. Using this model that has been calibrated with experimental measurements, simulation at any Vdd voltage can be carried out.

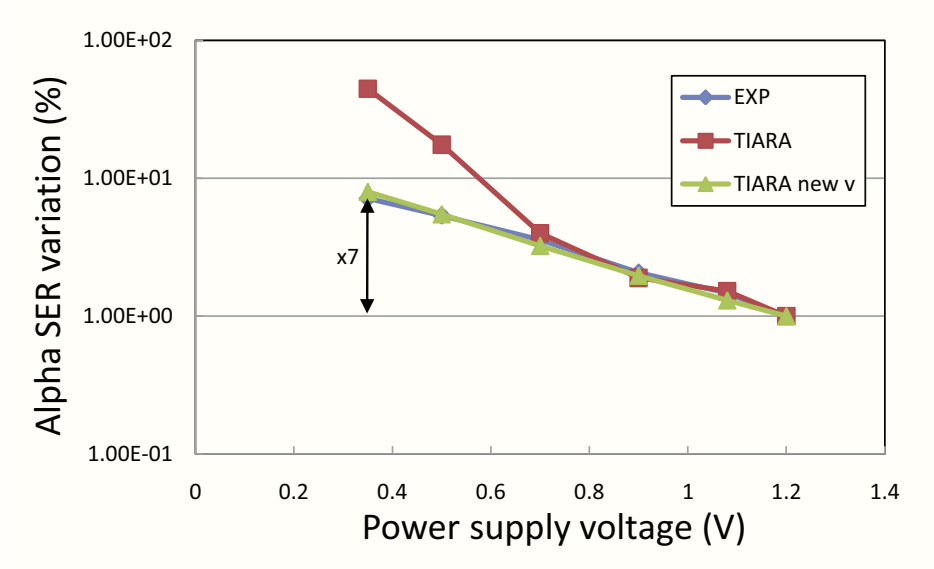

Figure 3.16: Simulated and experimental heavy ion cross-sections as a function of temperature for ULV SRAM memory [131] normalized to 1 at 1.2V.

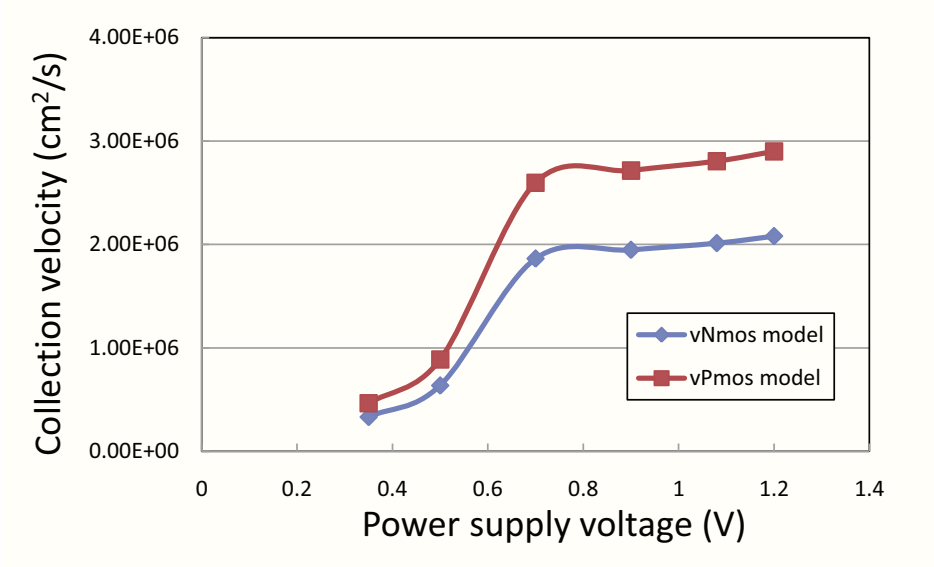

Figure 3.17: Values of collection velocities extrapolated from Alpha SER measurements for CMOS 65 nm technology as a function of Vdd voltage.

4.3 Assessment of process corners effect

In addition to temperature and V_{dd} assessment, TIARA simulations can be performed to analyze the influence of different process corners. Similar to power supply effect, there are two possibilities to account for process corner variation in SRAM memory: run full SPICE simulation using dedicated process corners defined in the PDK card models or extract from SPICE simulations Imax=f(Tmax) characteristics.

Introduction to process corners

Process corners refer to a variability of fabrication parameters during manufacturing of an integrated circuit. This section presents 3 sigma process corners variation effect on SEU response for ambient temperature and nominal power supply voltage. Process corners can be classified in two different groups: Front-End-Of-Line and Back -End-Of-Line process corners. Figure 3.18 shows a schematic of a SRAM cell structures that are impacted by the FEOL and BEOL process corners in blue and in red, respectively.

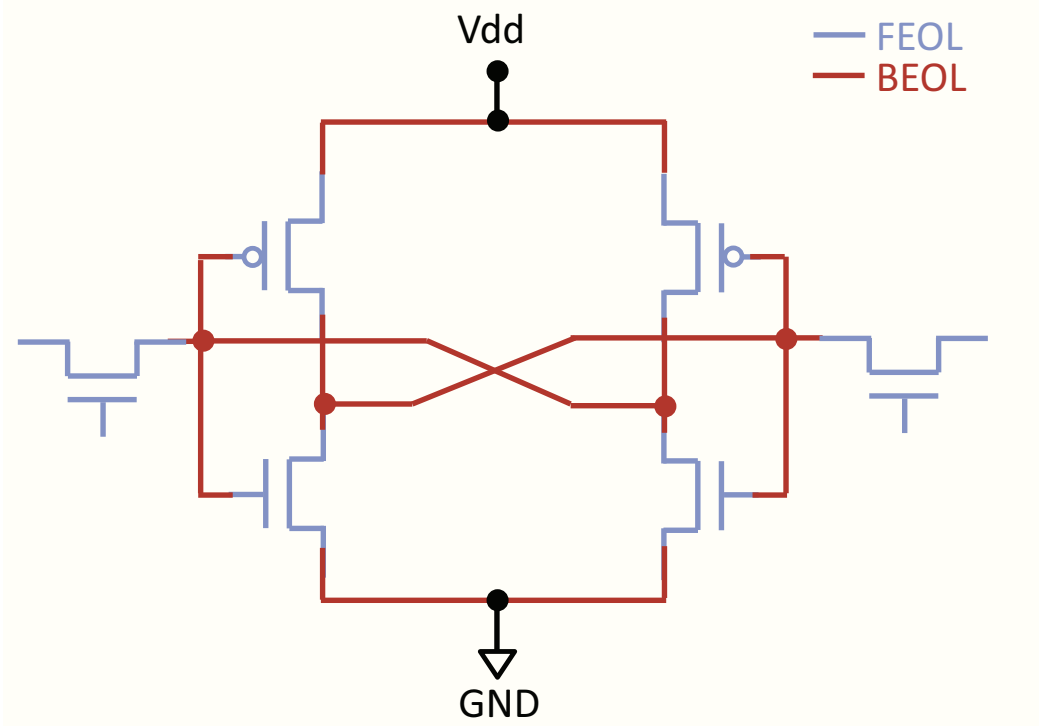

Figure 3.18: Schematic of a SRAM cell. Structures impacted by FEOL process corners are shown in blue while structures impacted by BEOL process corners are shown in red.

To FEOL corners belong typical, slow and fast corners for both NMOS and PMOS transistors. Slow and fast corners exhibit slower and faster MOS transistors due to variation of carrier mobilities, transistor channel length and width. In CMOS technology, the main process corners are typical NMOS/typical PMOS (or TT), slow NMOS/slow PMOS transistors (slow-slow or SS) and fast NMOS/fast PMOS transistors (fast-fast or FF).

The BEOL corners are attributed to the geometrical variations of passivation structures as metal lines, contacts, VIAs and passivation

dielectrics. These variations change the resistances and capacitances of interconnections. To account for the BEOL corners, the post-layout netlists are created with different parasitic extraction options. In this section, BEOL corners are denoted as Ctyp, Cmin and Cmax.

Assessment of FEOL process corners

SS and FF corners are the worst- and the best-case radiation-wise, respectively [132]. For SS corners, both NMOS and PMOS devices have lower drive currents (transistor I_{on}), thus lower capability of restoring of the nodal voltage after a disturbance and finally, the increased sensitivity. Figure 3.19 shows heavy ion cross-section for three FEOL process corners (SS, TT, FF) Heavy ion cross-section variation has been found to be around +/-8%.

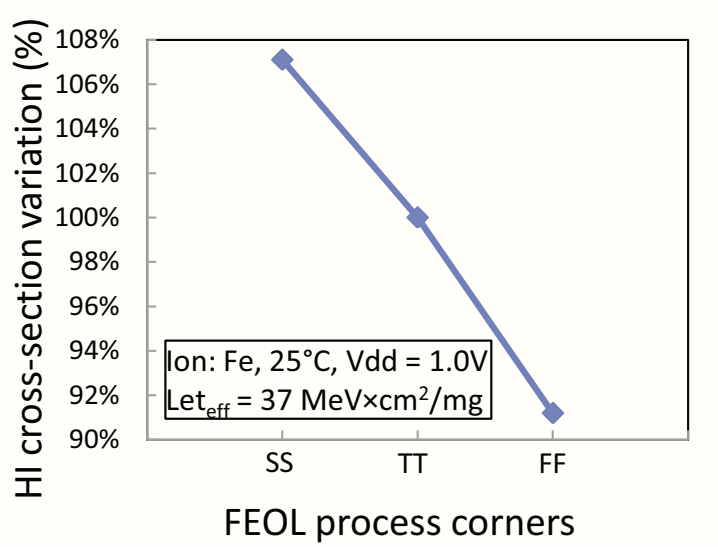

Figure 3.19: Simulated heavy ion cross-sections as a function of front-end process corners (single-port high-density SRAM memory) normalized to TT corners. TT stands for typical/typical, FF for fast/fast and SS for slow/slow process corners.

Assessment of BEOL process corners

In addition to the front-end-of-line, the back-end-of-line process corner effect on the radiation response of the circuit has been studied. The BEOL process corners are obtained by the post-layout netlist extraction using different parasitics values. These netlists have been obtained for the studied 32nm CMOS SRAM netlist and the TIARA estimation using full SPICE simulation as the upset criterion have been carried out to evaluate their effect on heavy ion cross-section (Figure 3.20). As it

can be seen, the BEOL process corners have the least impact on the sensitivity of the studied SRAM cell when compared to temperature, the power supply voltage and FEOL process corners. The influence of the BEOL capacitance variations should be more visible for LET particles as alpha environment.

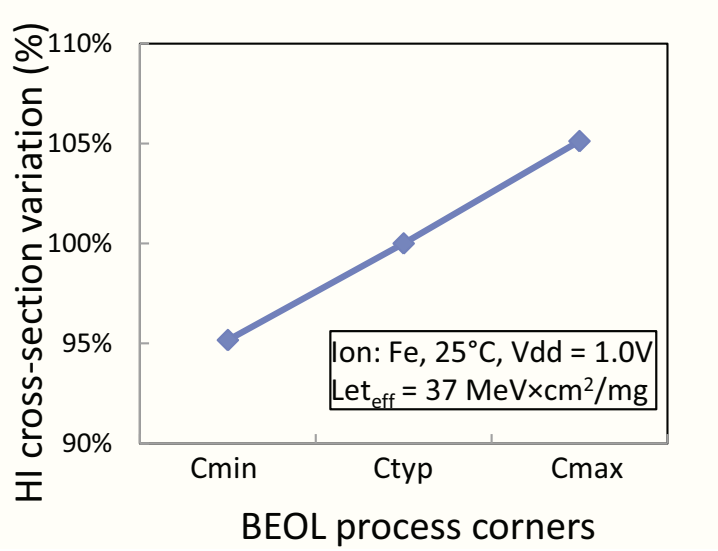

Figure 3.20: Simulated heavy ion cross-sections as a function of back-end process corners (single-port high-density SRAM memory) normalized to Ctyp corners. Ctyp stands for typical BEOL corners, Cmin for minimal parasitics and Cmax for maximal parasitics corners.

Conclusions

A moderate influence of FEOL as well as BEOL process corners on TIARA simulation results has been observed. The analysis have been performed for an iron ion of LET 37 $MeV \cdot cm^2 \cdot mg^{-1}$ to be able to compare the variations with previous studies performed for temperature and supply voltage assessments. However, this process influence should be more visible for low LET particles as alphas. Especially BEOL capacitance variation influence would be magnified. The aim of this section was to demonstrate TIARA capability. Nevertheless, further TIARA simulations and dedicated test vehicles are necessary to explain the SER differences as a function of process variability.

4.4 Additional cell layouts and architectures handled by TIARA

TIARA simulation capabilities presented in this chapter have been based on the standard-density single-port SRAM memory, however TIARA is capable of handling any design whose geometry in GDS format and

SPICE netlist are available. During this research work, TIARA has been extensively used for modeling the radiation effects in various SRAM and FF architectures. In this section, some examples are given.

Dual-port SRAMs

A dual-port SRAM is presented in Figure 3.21. The solid electrical schematic presents a standard 6-transistor single-port Static Random Access Memory cell while dotted transistors are a second pair of the access transistor of the dual-port SRAM bit-cell. This second pair of access transistors provides second independent access to the cell. From a radiation stand point, the additional transistor drains connected to the sensitive nodes via the metallization create additional sensitive surfaces that increase the cell sensitivity. To perform TIARA evaluations the sensitive surfaces of the access transistors were added to the usual NMOS sensitive surface [88].

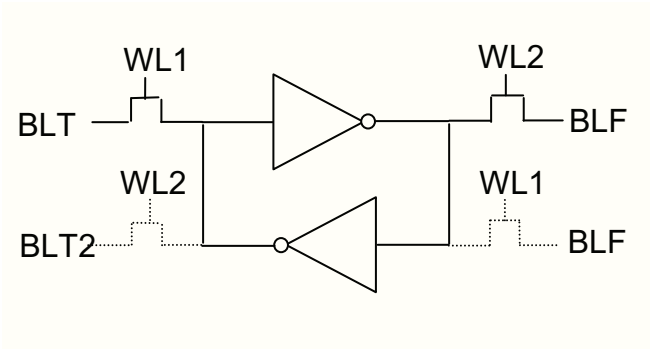

Figure 3.21: Single-port SRAM (solid) and dual-port SRAM schematics (solid + dotted) showing additional access transistors [83].

The experimental measurements have been carried out at the RADEF and UCL radiation facilities. The experimental set-up is strictly the same as presented in section 3.1.1. The measured test vehicle contains a 2Mbit matrix of dual-port high-density (DPHD) SRAM manufactured by STMicroelectronics in 65 nm CMOS technology. TIARA-simulated heavy ion cross-sections simulation results are compared with the experimental measurements in Figure 3.22 giving good agreement with the experiment. TIARA simulations in this chapter have been performed on 6-transistor standard-density single-port SRAM, 10-transistor Ultra-Low Voltage SRAM, 8-transistor dual-port high-density SRAM and 6-transistor standard density SRAM in 32nm technology, thus confirming TIARA's ability to model any SRAM architecture in different technological nodes.

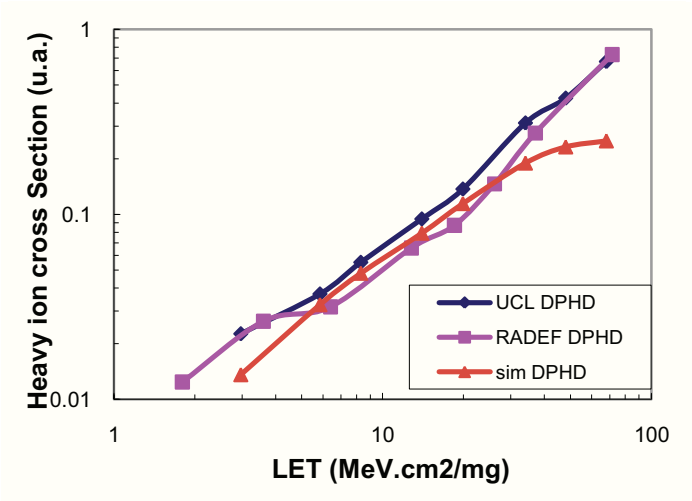

Figure 3.22: Dual-port SRAM simulated cross-section as a function of LET compared to experimental values.

TIARA simulation of Flip-Flops

Thanks to true integration with IC CAD environment, TIARA allows for modeling any cell as long as layout and SPICE netlist are available. Several Flip-Flop cells from standard ST libraries have been characterized with alpha particles with a radioactive americium source and with neutrons at the TRIUMF radiation facility. D-type FFs have been designed in 65nm technology, with standard- and high-densities, different drives, options (plain/clear/reset FFs) and with/without triple well process option.

The characterized Flip-Flops range from high-density to standard-density with different Flip-Flop features as reset, set, different drives, etc. The layout and the schematic of the basic standard-density Flip-Flop with the smallest drive is presented in Figure 3.23.

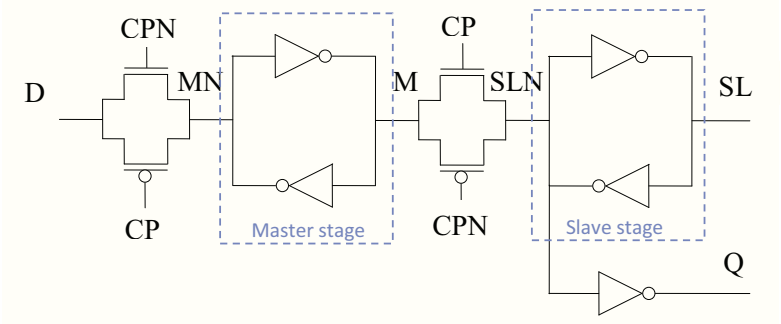

Figure 3.23: CMOS FF schematic with input (D, CP), output (Q) and main internal nodes (MN, M, SLN, SL).

The schematic of a CMOS egde-triggered FF is composed of two

latches called a master and a slave stage (shown in Figure 3.23) and is used as a data storage elements. Master and slave latches are enabled with opposite polarity of the clock signal: slave latch is controlled by the clock signal, while the master latch is enabled by the negated clock. As a result of such clock signal wiring, the first latch is transparent while the clock signal CP is low, and the current value of the D input is propagated to the input of the second transmission gate (TG). However, its input is non-conducting and FF outputs the value stored in the slave. The situation changes when the CP is high: the slave latch becomes transparent and the FF outpus the master value. Four configurations of each FF can be defined (all combinations of data and clock signals):

- CLK LOW DATA '0'
- CLK LOW DATA '1'
- CLK HIGH DATA '0'
- CLK HIGH DATA '1'

TIARA simulations have been performed on the tested FF. The comparison between TIARA simulated results and experimental ones for pain-FF and lowest drive are presented in Figure 3.3. The alpha simulations are in good agreement with experiment (8% of underestimation for TIARA). Neutron SER assessments show an underestimation of about 30% for the simulations compared to the experiment. The detailed analysis of the Neutron SER as a function of the simulated FF configuration is presented in Figure 3.4. The results are in a perfect agreement for three out of four configurations. The discrepancy for the third configuration causes this underestimation between TIARA results and experiment. Despite the detailed analysis of the simulations and electrical circuit behaviour using SPICE simulations, the cause of this discrepancy is not yet fully understood.

	EXP	TIARA
Alpha SER (FIT)	802	733
Neutron SER (FIT)	445	302

Table 3.3: Comparison between simulation and experimental results for basic standard-density Flip-Flop from ST library (averaged out of four configurations).

The validation of TIARA with a FF architecture confirms once more TIARA ability to model any digital circuit in any environment. Much more complex circuits can be simulated with TIARA [88; 133] such as the radiation-hardened-by-design circuits and are presented in the next chapter.

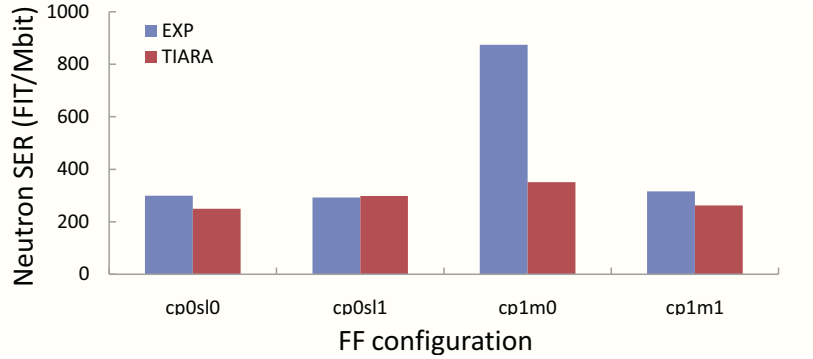

Table 3.4: Neutron Soft Error Rate as a function of Flip-Flop configurations.

5 Conclusion

In this chapter, TIARA simulations have been extensively validated by comparisons with experimental measurements and TCAD simulations in different radiation environments (heavy ions, alphas, neutrons). A good agreement between simulation and experiment show the relevance of the modeling approach. This validation shows that TIARA allows for assessing radiation reliability for a very wide LET range from tens of keV to hundreds of MeV proving the relevance of model assumptions. Moreover, TIARA allows handling any digital circuit architecture which has been proven with simulation of numerous SRAM bit-cell architectures and Flip-Flops designed in different CMOS technologies. Finally, TIARA capabilities demonstrated the feasibility of assessment for different temperatures, power supply voltages and process corners.

The final chapter of this thesis will present a TIARA use for the most complex Monte-Carlo SEE analyses as charge sharing assessment , different upset mechanisms for different simulated circuits and comparison between SER testings with different radiation sources. Projections of CMOS downscaling on the digital cells sensitivity for the future technologies and design challenges will be discussed.

Chapter 4

TIARA use for advanced analysis of SEE mechanisms in standard and radiation-hardened circuits

1 Introduction

This chapter presents the most complex Monte-Carlo analyses of SEE effects that can be conducted using TIARA and the latest topics being raised by the radiation effects community are addressed. Heavy ion cross-sections as a function of effective LET as well as alpha and neutron SER values are investigated in a RHBD Flip-Flop that is based on the dual-interlocked storage cell latch. Moreover, SEE analyses are performed such as charge sharing, different upset mechanisms as a function of simulated architecture as well as several hardening solutions are evaluated. Radiation sensitivity is assessed as a function of CMOS technology downscaling and the future design challenges are discussed.

This chapter is organized as follows: section 1 presents an introduction to the DICE architecture followed by detailed analysis of a ST implementation of a single-row DICE in 65nm CMOS technology in all radiation environments. Hardening by use of Double-Height Cell (DHC) technology is assessed on the real design developed in the framework of this thesis. Section 2 focuses on charge sharing investigations and TIARA-driven design optimization by transistor placement. In section 3, the focus is put on an in-depth analysis of terrestrial neutron environment as the most difficult to be modeled and effect of different neutron spectra on Soft Error Rate. Final section presents TIARA projections on future technology nodes.

2 Experiments and simulations on a 65nm DICE Flip-Flop

Lately, the Dual-Interlocked Storage Cell (DICE) RHBD architecture have received a lot of attention from the radiation effects community and is reported as the most common hardening technique for latch-based digital circuits. This section describes the basics of the DICE, discusses its implementations and presents heavy ion cross-sections/neutron SER/alpha SER for both TIARA simulations and experimental measurements.

2.1 Dual-Interlocked Storage Cell architecture - foreword

Historically, the high-reliability electronics, especially space-borne electronics, were manufactured using special processes allowing for improving the radiation tolerance such as [134]. However, the old-fashioned process-level hardening solutions known also as radiation-hardening-by-process (RHBP) tend to be superseded by the radiation-hardening-by-design (RHBD); except of Silicon-On-Insulator (SOI) technology and tripple-well process option. RHBP involves important RD costs, the necessity of developing a dedicated manufacturing process and finally poor performances when compared with the state-of-the-art commercial technologies. The rapid growth of RHBD techniques has lead to a wide variety of solutions ranging from device-level through circuit-level to system level solutions [135].

At device- and circuit-level, the most common hardening techniques are based on increasing the critical charge of a sensitive node by adding additional capacitances [references] or resistances in a feedback loop [references] and the redundancy either in time or space domain.

Concerning the increase of charge capacitance, often it is realized by using Metal-Insulator-Metal (MIM) and eDRAM capacitors. The reference [135] gives the detailed analysis of this technique. The integration of two MIM capacitors to a SRAM cell decreases the SER of the device, while the device area is not impacted. In the presented memory, the capacitors are inserted between the poly-silicon and the metal layer in a third dimension just above the standard six-transistor SRAM cell. The internal node capacitance in 90nm CMOS process can be increased up to 12fF per unit resulting in highly increased critical charge, thus significantly lower SER. Although the read currents and static noise margin (SNM) of the cell are not impacted by this technique, the major drawback is the increased write time. For the capacitor value of 12fF per node, the write operation is slowed down by a factor of three.

The temporal redundancy is based on sampling the input signal at different time instances. In order to be effective, the sampling speed has to be lower that ion-induced transient widths [136]. The advantage of this technique is that not only SEU can be mitigated but also a SET in the input. However, the huge performance penalty (at least the double width of the parasitic current width) causes that temporal redundancies are not a common mitigation method.

As far as the spacial redundancy is concerned, the most straightforward technique is the Triple Modular Redundancy (TMR) that consists in triplication of circuit nodes, i.e. latches or FF, and the use of a majority voter circuit that votes out the corrupted one. TMR results in huge area and power penalties as transistor count in the design is tripled. On the other hand, the circuit performance degradation is very low since only the voter transmission time impacts the speed.

The others techniques employing the spacial redundancy replicate the circuit nodes that store the logical information and use a feedback to restore a correct value after an ion strike. To these techniques belong: the Dual-Interlocked Storage Cell (DICE) [137], the Single Event Resistant Topology (SERT) [138] or Heavy Ion Tolerant cell [139]. The DICE cell has been widely used in the industry for years as it offers area and power penalties inferior to the TMR and very satisfactory radiation-event effect mitigation. Its architecture, that contains information in the form of two pairs of complementary nodes of the circuit, is able to restore any logical value to its initial state after modification due to the disturbance.

DICE latch electrical schematic is presented in Figure 4.1. The circuit nodes ’1’, ’2’, ’3’, and ’4’ contain the values 0, 1, 0, and 1, respectively. This means that the transistors N1, N3, P2 and P4 conduct and transistors N2, N4, P1 and P3 are off. Let us consider a radiation-event impacting only the N2 NMOS transistor. An ion-induced single-event transient is produced in the circuit node ’2’ and causes current flow through P2 PMOS transistor that tries to recover the original node state. This P2 PMOS drive current is the source of a voltage drop at node 2. Finally, voltage drop on the node ’2’ provokes the on-state of the N1 NMOS and the off-state of the P3 PMOS. Nevertheless, the disturbance does not propagate further in the circuit as the P1 PMOS gate is well biased by node ’4’ and the N4 NMOS gate by node ’1’. The node ’2’ bias will slowly be recovered by the P2 PMOS and the bit-flip will not occur. As seen, the ion strikes to a single node will not result in an SEU.

As a consequence, to corrupt the memorized data both redundant nodes have to be affected by the carrier collection mechanisms. It means that if a particle strikes the Pwell, N2/N4 have to simultaneously

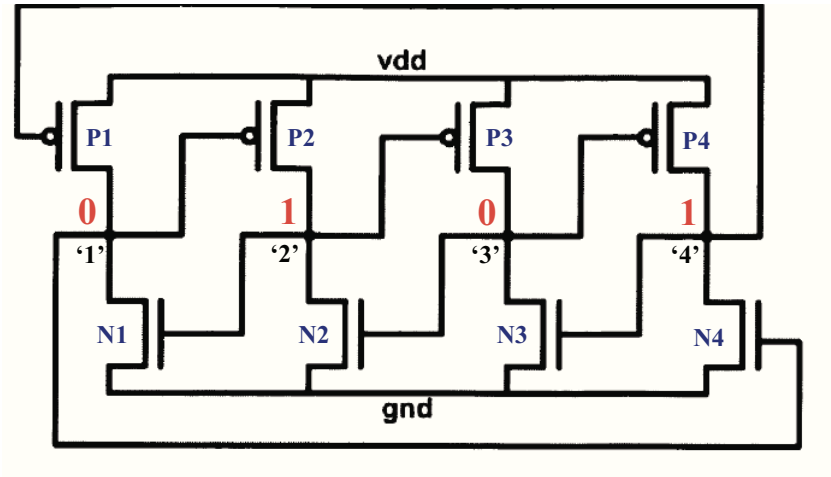

Figure 4.1: The dual-interlocked storage cell schematic [137].

Symbol	Name
(A)	Succesive hits by one ion
(B)	Multiple hits by multiple ions
(C)	Drift-Diffusion charge (charge sharing)
(D)	Parasitic Bipolar Effect

Table 4.1: Possible mechanisms of multiple-node charge collection that can corrupt the memorized value in a DICE structure [140].

collect carriers. Then, in addition to node '2' disturbance, there is a SET causing the node '4' de-bias and affecting the N3 NMOS and P1 PMOS behaviour and the cell changes the value. The upset analysis for the P1/P3 pair collection is straightforward and not detailed here.

Four mechanisms have been identified that cause multi-node charge collection [140]. Table 4.1 lists all these mechamisms. The authors have identified the most probable mechanisms of multi-node charge collection: the charge sharing due to drift and diffusion (C). For high energy neutrons, as a result of a nuclear reaction, many secondary ionizing products can be produced (protons, alphas, heavier ions) that may strike multiple nodes (B). Additionally, the charged particles with high LET values may provoke the well de-polarization and as a consequence the parasitic bipolar action (D). All these 4 DICE upset mechanisms will be analyzed in the following sections using the experimental data from different radiation facilities and dedicated TIARA simulations on order to confirm or decline these findings in the studied cells.

2.2 Flip-Flop implementation

Flip-Flop cell

A Dual-Interlocked Storage Cell Flip-Flop was designed in compliance with the ST 65 nm CMOS design rules. The FF circuit contains the input stage with scan-in, test, reset features and the output stage, which gives more than 70 transistors. Four different static configurations of the FF can be distinguished: two logic states '0' or '1' stored in the master (M) or in the slave (SL), depending on the clock state. Additional collection surfaces of the reset transistor drains and clock transmission gate transistor drains connected via metallization layers to the sensitive nodes play an important part in the charge collection and cannot be neglected. Moreover, those surfaces depend on the previously mentioned configurations of the FF. In the worst configuration, four off-state NMOS transistors and three PMOS transistors are connected to the sensitive nodes, while in the best case only two NMOS and two PMOS transistors are connected to a single sensitive node. In TIARA simulations all these off-state drains will be taken into account as charge collection junctions to reproduce the real cell response to radiation. Notheworthy is the fact that the FF layout is very dense with optimized cell area (full custom design).

Test chip description

A dedicated test chip was designed and manufactured by STMicroelectronics in a 65 nm low power (LP) CMOS technology with a twin-well process option. Its supply voltage is equal to 1.2V and Shallow Trench Isolations (STI) are used for isolation between devices. The die dimensions are 2.5 mm^2, the test vehicle embeds the RHBD FFs presented briefly in the previous paragraph. The FFs are implemented as two identical shift registers instances for a total of +50k FFs. The chip was specially manufactured to validate this particular FF design optimized for high-speed terrestrial applications.

2.3 Simulation results vs. experiments for heavy-ions and alphas

Heavy-ion cross-sections

The heavy ion experiments were carried out at the RADEF (Radiation Effects Facility, Finland) [79] radiation facility in compliance with ESA test standard no.25100 [14]. The species used for experiment were Nitrogen, Neon, Argon, Krypton, and Xeon. During the experiment, the FFs were programmed in four configurations (all combinations of clock and data signal) and their static cross-sections were measured under

heavy-ion irradiation.

The first TIARA Monte-Carlo simulations of the full DICE FF presented in [88] showed good agreement with experimental results for normal to the die surface broadbeam direction. At that time, TIARA did not cope with tilt and roll angles. Now, TIARA simulations take into account tilt and roll angles in cross section calculations. It allows simulating the entire range of experimental heavy ion cocktail used at RADEF. Figure 4.2 shows a comparison of these simulated cross-sections with the experimental ones for all FF configurations. In this figure, simulation upper limits, when no upset is recorded, are depicted with purple arrows. The cross-sections and effective LET values are plotted in arbitrary units due to confidentiality. An excellent agreement between experimental and simulated data is observed. The upper limits denoted in figure with arrows can be decreased by simulating higher number of ion strikes.

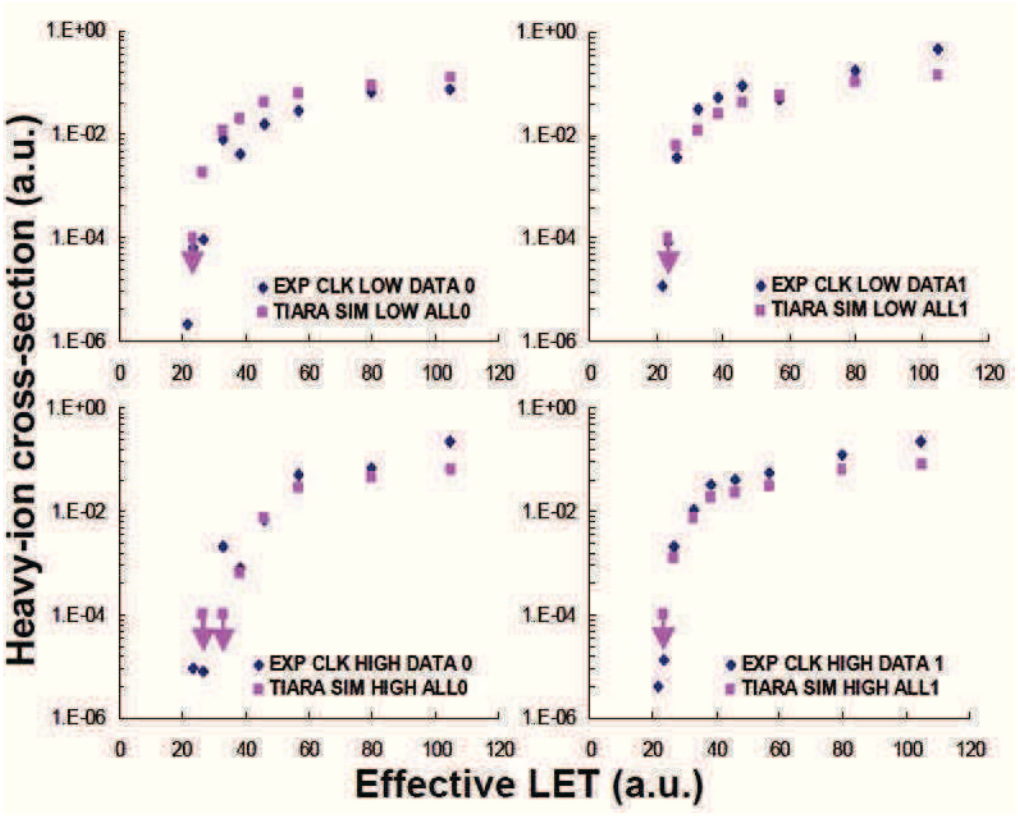

Figure 4.2: Comparison between experimental and simulated heavy ion cross-sections as a function of LET value. The same ion tilt and roll angles are used in the simulation and during the experiments. The purple arrows show the simulation upper limits when no upset has been recorded.

TIARA is capable of modeling three out of four DICE upset mechanisms listed in Table 4.1: the successive hits of sensitive nodes by one ion (A), multiple hits by multiple ions (B) and ion-deposited charge dif-

fusion and collection by the off-state junctions (C). For the heavy ion irradiation, the probability of multiple hits by multiple ions (B) at the same time is extremely low and thus it is not analyzed in this section. An excellent agreement between TIARA simulations results and experimental data obtained from RADEF confirms that bipolar amplification (D) is less important parameter for this considered DICE structure. Parasitic bipolar action is observed especially in N-wells because of their large square resistance which causes big potential variations after an ion strike. In the FF structures the bipolar effect is much less visible due to larger N-wells (about x7) and denser well-tie distribution. The large wells cause the decrease of resistance between well-ties and as a consequence the decrease of bipolar effect.

These simulation results confirm the results presented in [140] that charge drift-diffusion charge sharing is the main upset mechanisms for DICE-like FF, the parasitic bipolar action is much less important, successive hits of redundant nodes by one ion are very unlikely because of the beam orientation that is tilted maximally up to 60∘ and multiple hist by multiple ions are not possible during experiments.

For one of the ions, irradiations were performed with 60 degrees of tilt and two perpendicular roll angles: parallel to the well orientation (0∘ of roll) and perpendicular to the well orientation (90∘ of roll). The comparison between the experimental results and simulation data is shown in Table 4.2. The cross-sections are normalized to the value of the experimental cross-section (XS exp) for the ion strike at 60∘ of tilt and 90∘ of roll (60∘ / 90∘). The cross-section for ion strikes parallel to the well direction is 3 times higher than strikes perpendicular to the well direction. The same trend is observed for TIARA simulation results that take into account the roll and tilt angles. The middle column (XS LETeff) shows the vertical ion impacts [88] with the ion effective LET value: $LET_{eff} = LET/cos(\theta)$, where θ is the tilt angle. Those results highlight the importance of taking into account the tilt/roll angles in simulation to accurately reproduce experimental observations. Similar trends are observed in [143], in which directional dependency of the cross-section as a function of roll angle was measured in a 90 nm technology. The ion beam parallel to the wells shows the significant cross-section increase and decrease in LET threshold while the ion beam perpendicular to the well orientation results in similar cross-section to the vertical ion strikes.

Alpha Soft Error Rate

Alpha experimental testings were performed at STMicroelectronics. The experimental set-up and alpha americium source are presented in section 3.1.2.

Ion strike : tilt/roll	exp XS (a.u.)	TIARA XS [1] no tilt (a.u.)	TIARA XS tilt (a.u.)
60°/ 0°	3.26	0.838	3.39
60°/ 90°	1.00		1.28

Table 4.2: Comparison between experimental data and simulation results for one ion tilted by 60deg and for two different roll angles: parallel and perpendicular to the well direction. Data have been normalized to experimental cross-sections for 60∘ of tilt and 90∘ of roll.

Test Condition	EXP Flips (FIT)		EXP MCU (FIT)		TIARA (FIT)	
	FIT Value	Upper Limit	FIT Value	Upper Limit	FIT Value	Upper Limit
CLK LOW DATA '0'	0	3	0	3	0	1.52e-2
CLK LOW DATA '1'	0	1	0	1	0	1.52e-2
CLK HIGH DATA '0'	0	4	0	4	0	1.52e-2
CLK HIGH DATA '1'	0	3	0	3	0	1.52e-2

Table 4.3: Experimental Alpha test results as a function of DICE FF configurations.

The comparison of experimental alpha test results and TIARA simulations as a function of the DICE FF configuration is summarized in Table 4.3. The experimental and simulation upper limits were computed and are shown in the table. Both experimental and simulation results confirm the complete immunity to alpha particles of this particular Flip-Flop design.

According to [140], the alpha particles cannot induce upsets based on mechanism (B). Geometrically, it is also improbable for alphas to directly hit both redundant nodes when the generation occurs in the source placed above the active die area (A). The only possible mechanism would be multiple-node charge sharing but the distance between the redundant nodes is high enough to keep the simultaneous charge collection under the critical level.

2.4 In-depth analysis of neutron-induced Upset mechanisms

Experimental set-up

The neutron irradiations were carried out with the continuous neutron source available at TRIUMF radiation facility in Vancouver, Canada. The neutron spectrum closely matches the terrestrial environment for energies ranging from 10 MeV up to 800 MeV. The design-of-experiment included different test patterns and supply voltages. The test procedure is compliant with the JEDEC SER test standard JESD89A [12]. During the experiment, the FFs were programmed in four configurations and their static neutron SERs were measured. The FF configurations represent all combinations of clock and data signals, denoted in this work as: CLK LOW DATA '0', CLK LOW DATA '1', CLK HIGH DATA '0', CLK HIGH DATA '1'.

Simulation vs. experiment

An excellent agreement between the experimental data and TIARA simulation has been obtained for this DICE FF. For the less sensitive of the DICE FF configurations, TIARA simulation has been performed several times with very high amount of neutron strikes (exceeding 1 billion generated neutrons), because initially no upsets were recorded. The initial number of simulated neutrons was not sufficient to observe such a low SER value. The neutron Soft Error Rates for standard Flip-Flop have been already discussed briefly in chapter 3 section 5.2. Figure 3.4 shows very good agreement between the TIARA estimation and experiment for three out of four configurations of the FF. Noteworthy is the fact that between the most and the least sensitive of the SER for both structures (DICE and standard FF), there is a difference of over two orders of magnitudes and the simulation approach stays valid in this range.

Detailed analysis of nuclear reactions leading to upsets

For both TIARA simulations (standard 26-transistor FF and DICE FF architectures), a detailed analysis of the upset mechanisms has been performed. TIARA output files allow to obtain information about reactions that caused an upset and which did not. Moreover, for each simulated upset, the post-processing of simulation output gives full details such as the reaction position, type of the reaction (elastic or inelastic collision), if relevant the number of secondary ions with their momentums, ranges, energies, etc.

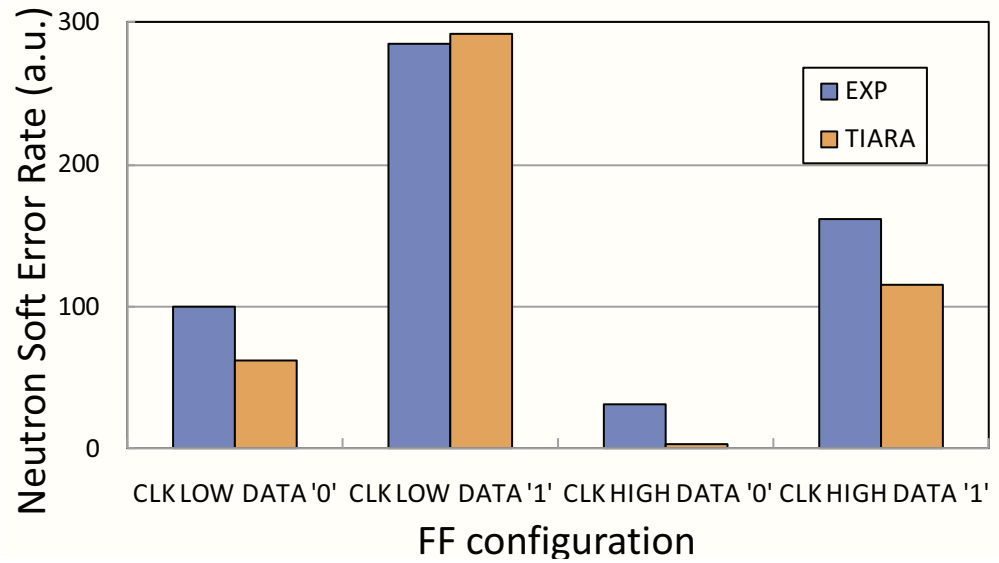

Figure 4.3: Agreement between simulated and experimental neutron SER as a function of different FF configuration for Dual-Interlocked Storage Cell (DICE) FF. The values were normalized to 100 for the experimental SER for CLK HIGH DATA ’0’ configuration.

In Figure 4.4 the neutron-induced percentage of Soft Errors is plotted as a function of number of secondary ions generated by a nuclear reaction and as a function of FF configuration. For this standard FF, between 70% and 80% of upsets are caused by elastic scattering between neutrons and silicon atoms of the crystalline structure. It is sufficient that a particle (displacement of Si atom in this case) deposits enough charge near one reverse biased junction to upset a value stored by the FF. The reactions with multiple products cause (average of all configurations) 28% of upsets, i.e. 19%, 6%, 2.4% and 0.5% are caused by reactions with two-, three-, four and more than four secondary ionizing particles, respectively. Using both Figure 3.4 and Figure 4.4, an interesting trend is observed that the more sensitive the configuration, the higher the percentage of errors caused by elastic reactions. The elastic reactions cause the deposition of charge very locally by silicon recoil which range is small but LET value is high. On the other hand, charge deposited by nuclear reactions with many secondary is more distributed.

Figure 4.5 presents an analogous error percentages as a function of multiple products for different configurations of the DICE FF. In this case, the difference as a function of FF configuration is much more important. For the most sensitive FF configuration, that is clock LOW data equal to ’1’, the contribution of elastic scattering to total upset number is lower than for the standard architecture but still dominant. However, for less sensitive (as shwon in Figure 4.3) clock HIGH data ’1’ the percentage of elastic reactions decrease to about 50% and accordingly the multiple product reactions increase. The reactions with multiple prod-

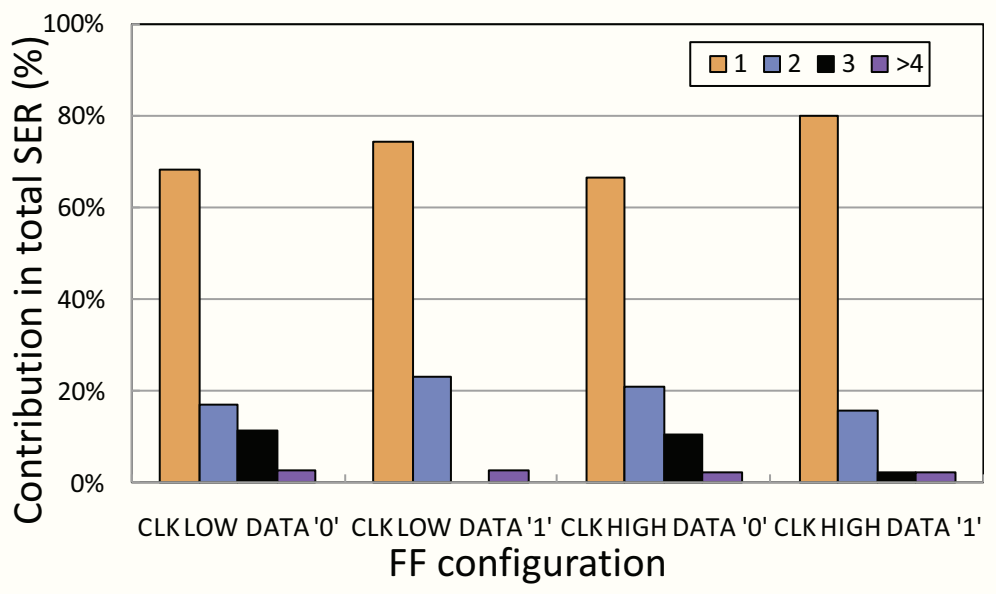

Figure 4.4: Percentage of Soft Errors as a function of the FF configuration and as a function of the number of secondary products for standard Flip-Flop.

ucts increase significantly from less than 40% to over 50%. For the CLK LOW DATA ’0’ configuration, almost 80% of errors appear due to multi-product reactions with a maximum for a reaction producing two particles (44%). This situation is caused by the specific DICE architecture. As already analyzed in the introduction to DICE section and shown in the literature both redundant nodes have to be impacted to cause a bit-flip in DICE [88; 137].

The most effective reactions causing the SEUs in DICE structure are presented in Table 4.4 (only inelastic scattering taken into account, same results for STD FF). When comparing the composition of G4 database and reactions in Table 4.4, the contribution in total upset rate is clearly linked with the occurrence of the secondary ions in the database: 87% of upsets due to inelastic collisions is caused by aluminum and magnesium (first three most effective reactions), 10% by neon and sodium, 1.3% by oxygen. Their occurrences in database are respectively 28.6%, 2.3% and 0.3%. Table 4.4 summarizes the reactions that provoke at least 1% of the total Soft Errors.

SPICE analysis of injected charge in the DICE netlist shows that even small collected charge on the redundant node (< 0.5fC) can create an error if the second node is impacted [141]. TIARA simulation results seem to confirm this theory for less sensitive configurations. When one node collects a big charge from a heavy product and the redundant one is impacted by a lighter particle as a proton or alpha, a SEU occurs. For more sensitive configurations, the deposited charge by one heavy

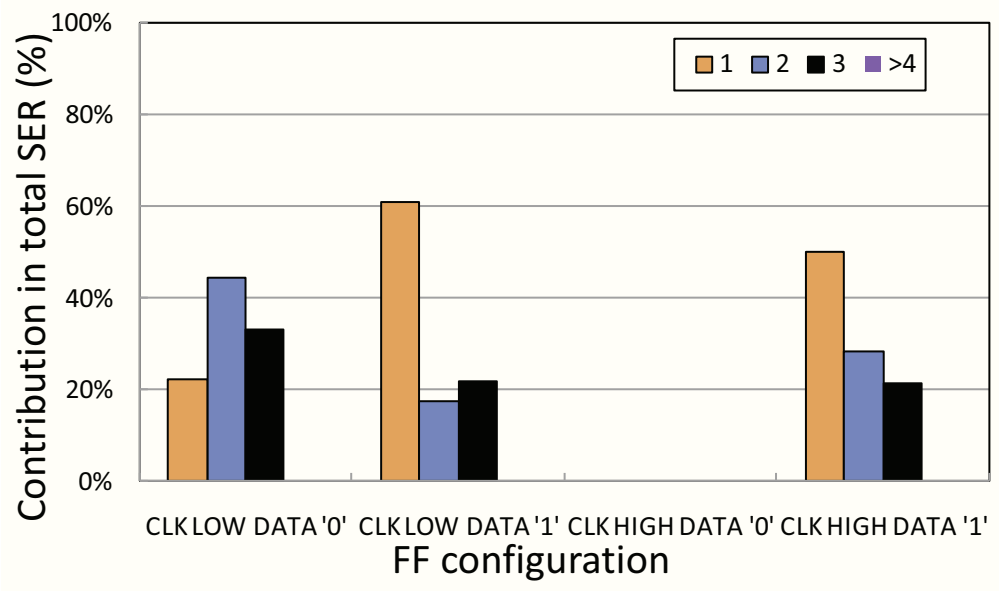

Figure 4.5: Percentage of Soft Errors as a function of the FF configuration and for different number of secondary products for radiation-hardened-by-design Flip-Flop.

Number of products	Reaction products	Percentage of erros
2	Al, p	45%
3	Mg, 2p	28%
2	Al, α	14%
4	Ne, α, 2p	4%
3	Na, α, p	3%
5	Ne, 4p	1.7%
4	Na, 3p	1.3%
4	O, 3α	1.3%
		Total Upsets 98.3%

Table 4.4: The most effective nuclear reactions for a DICE FF simulation averaged for all FF configurations showing the product atoms and percentages in total upset rate.

product can already be sufficient to upset even a DICE-based FF. This shows slightly different upset mechanisms for neutron irradiation than for heavy ions presented before in this section. Contrary to heavy ions, for neutrons multiple hits by multiple ions are possible and show significant contribution especially for the least sensitive configurations. For the most sensitive ones the charge sharing together with multiple hist by multiple ions induce bit-flips.

2.5 Single- vs. double-height implementation of DICE

The previous section analyzed in details the single-height cell implementation of DICE. It was also identified that charge sharing is the major upset mechanism. The simplest method to decrease charge sharing is to increase the distance between the redundant nodes. This leads to large area overheads that are not acceptable in commercial designs. Moreover, with ever decreasing feature size of the technology, these distances are reduced, thus limiting the circuit robustness [93].

In order to increase the design freedom of radiation-hardened-by-design cells, the use of double height cell (DHC) technology has been proposed [142]. In the DHC technology, the drift-diffusion collection (i.e. charge sharing) is mitigated by placing the PMOS transistors between the redundant NMOS nodes. Moreover, the parasitic bipolar effect does not affect the same NMOS redundant nodes as they are placed in two separate wells. Figure 4.6 compares both the single height cell and double height cell implementations. In ref [142], the double-height cell shows the SER improvement of about a factor of 15 when compared to the simple-height cell with no area penalty, thus responding perfectly to the commercial design needs.

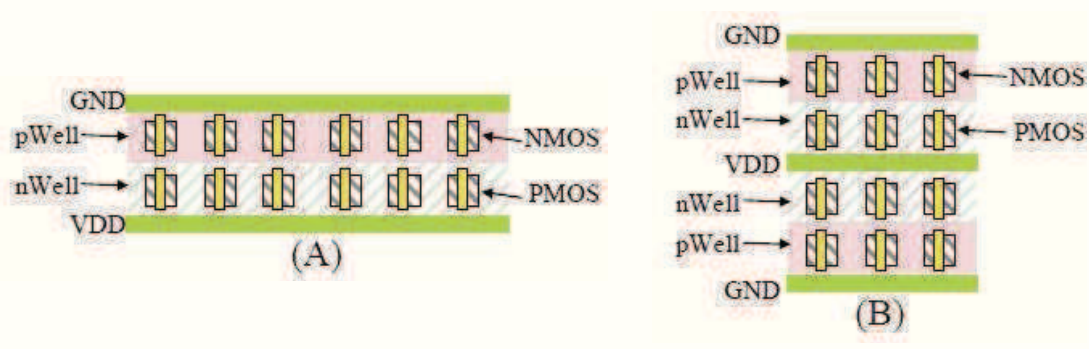

Figure 4.6: Two implementations of hardiation-hardened-by-design latch: in single height cell (a) and double height cell (DHC) technology. In both cases the cell area is the same, though the cell area shapes are different [142].

Hence, it was decided to independently assess this gain with TIARA. After designing a first layout, TIARA simulations were performed to detect layout weaknesses (most sensitive transistor pairs) and layout modifications have been introduced to improve hardening and to maximize gain of DHC technology. The simulations were carried out with the same set of technological parameters, transport models and radiation environments for both types of FFs (single-height and double-height) and taking into account cell geometries provided in GDS format. TIARA heavy-ion cross section simulation results as a function of effective LET value are presented in Figure 4.7. It is clearly seen that double cell height allows for increasing the FF hardness significantly for 3 out of four FF configurations (x10-x100). For the CLK HIGH DATA '1' configuration, the gain is moderate but still superior to x3.

The average DHC gain has also been computed from the presented cross section results. First, the SHC simulation results were extrapolated for the same values as the simulation for DHC technology and second, the gain of DHC technology for each of the heavy ion cross-section values has been calculated. The average gain value is equal to 21.3. This value is in good agreement with data presented in ref [142].

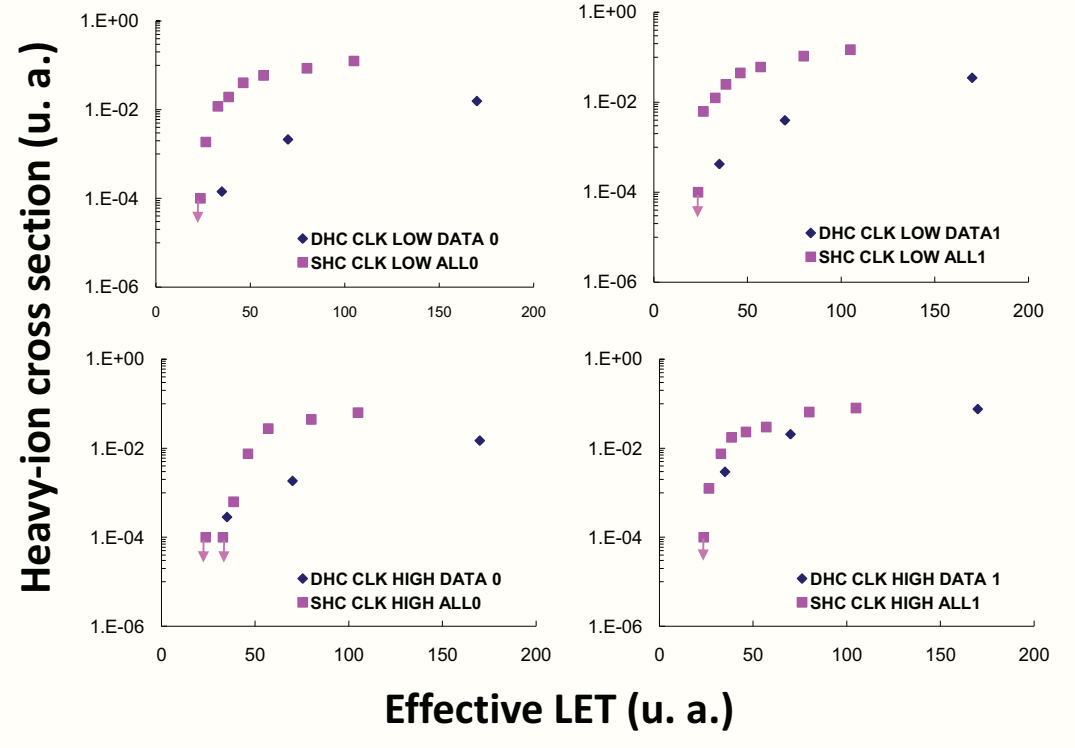

Figure 4.7: Comparison between TIARA simulated heavy ion cross-sections for simple-height cell and double-height cell technology as a function of LET value.

3 Monte-Carlo based charge sharing investigations

The technology downscaling has resulted in reducing the distance between redundant transistors which leads to a significant charge sharing increase [11]. Recently, several studies have been performed to mitigate charge sharing on sub-100nm technologies by using guard-diodes and guard-rings [94] or transistor separation [11]. Their goal was to increase the hardness of the DICE architecture by various design techniques [85; 142; 144]. In this section, the charge sharing investigations are performed using Monte-Carlo approach. First, analytical models of charge sharing are validated with TCAD and than are used to analyse charge sharing and propose hardened simulation-driven transistor placements.

3.1 Correlation between analytical models and TCAD

At first, the 3D Flip-Flop TCAD model (Figure 4.8) is constructed from a standard FF GDS layout using TCAD tools (Sentaurus Synopsys package)[89]. The exact 3D geometry data with doping profiles are optimized for the ST 65nm manufacturing process. This structure has been constructued to analyse in detail charge sharing mechanisms between transistor of a FF. 3D device ion strike simulations have been performed on a powerful 64-bit multiprocessor system; the simulation of one ion strike converges in approximately 15 days. The full 3D structure of a RHBD FF (50 transistors or more) is very difficult to create and probably could not be simulated in the satisfactory time, thus simplified structures (as the one presented in Figure 4.9(a) have to be used for charge sharing investigations.

Finally, to examine the charge sharing processes due to an ion strike, a specific simplified TCAD structure has been created: it contains two NMOS (NM1 NM2) and two PMOS transistors (PM1 PM2) (Figure 4.9a). The distances between NMOS transistor drains, PMOS transistor drains, and pairs NM1-PM1 / NM2- PM2 are all equal to 0.4μm. The NMOS/PMOS transistor dimensions and their spacing are chosen to assure a good compromise with respect to the real Flip-Flop designs. 3D device simulations are performed using a Sentaurus Device with the following physical models: Drift Diffusion for transport of carriers, Shockley-Read-Hall and Auger for recombination, electric field and doping dependant models for mobility and heavy ion module for carrier deposition along particles track. The heavy ion generation model uses the Gaussian radial distribution of charges with a fixed characteristic radius of 0.07μm and ion penetration depth of 2μm which exceeds the effective charge collection depth [11]. It is assumed that the charge collection depths do

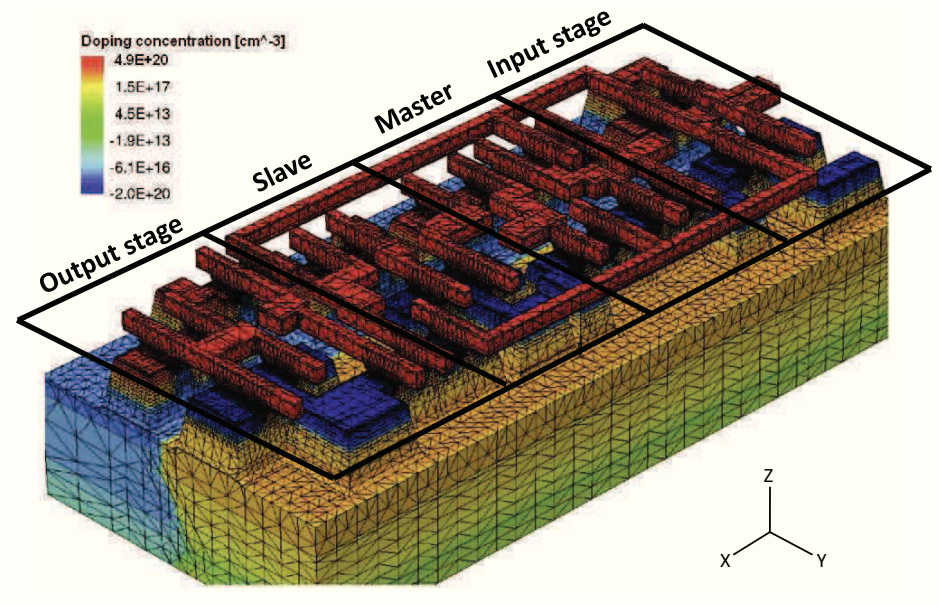

Figure 4.8: 3D TCAD FF model showing doping profiles. Shallow Trench Isolations filled with SiO2 dielectrics are removed from this display for clarity. The structure is composed of 2.5 million mesh elements.

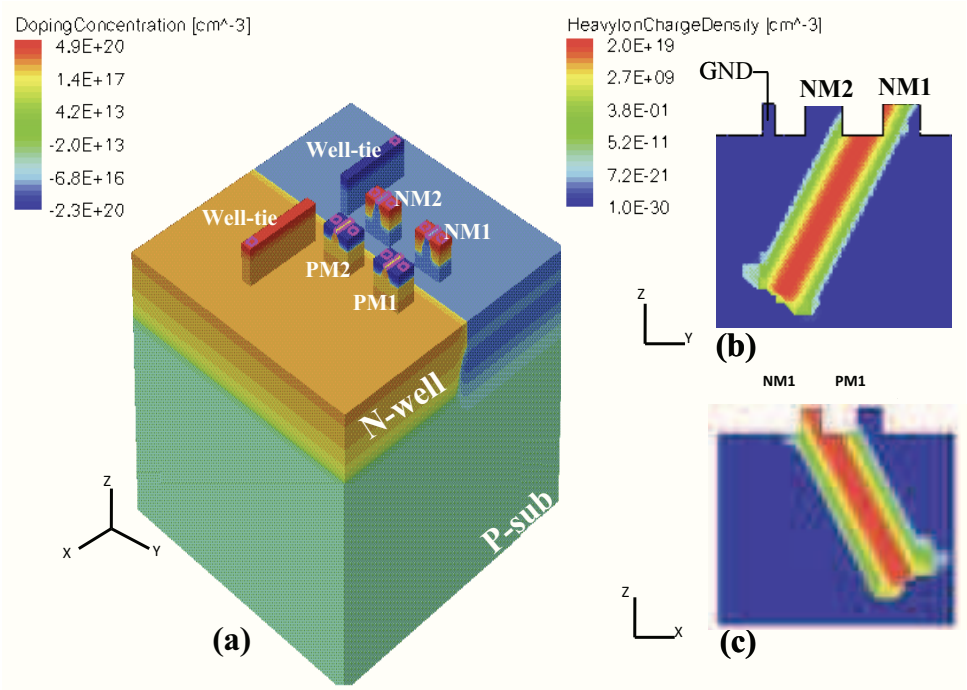

Figure 4.9: TCAD structure used for NMOS-NMOS / PMOS-PMOS / NMOS-PMOS charge sharing studies: 3D model showing doping profiles (a), heavy ion charge density for NMOS1 drain impact and towards NMOS2 (b), heavy ion charge density for NMOS1 drain impact and towards PMOS1 (c). The Shallow Trench Isolations filled with SiO2 dielectrics are removed for clarity.

not vary significantly as a function of technology because of small variations of doping profiles deep in the substrate (sin2μm). LET along the track is considered to be constant and equal to 10 $MeV \cdot cm^2/mg$.

3D TCAD simulations of ion strikes in the NM1 transistor drain have been performed for several tilt angles towards the second NMOS transistor - NM2 (Figure 4.9b) and the closest PMOS transistor - PM1 (Figure 4.9c). Ion induced current pulses from TCAD simulations have then been compared with the analytical diffusion-collection current model. Figure 4.10a shows the example of ion-induced currents collected by NM2 and PM1 transistors for the ion strike with the LET value equal to 10 $MeV \cdot cm^2/mg$ and the tilt angle = 30deg in the NM1 transistor towards NM2. It can be observed that the charge collection for PM1 is negligible when compared to NM2, thus in the analytical model, we consider that if the ion track does not cross the Nwell, the charge collected by PMOS transistors is equal to zero. Figure 4.10b shows the simulation results of ion strike in NM1 towards PM1 transistor. In this case, the charge sharing between the two NMOS transistors is still higher than between NMOS and PMOS. It can be explained by the fact that more charge is deposited in the substrate than in the N-well. Ion path goes through P-well, N-well, and finally P-substrate beneath the N-well. These simulations confirm that the well boundary acts as a charge diffusion barrier as already observed for 130nm and 90nm technologies [102; 143].

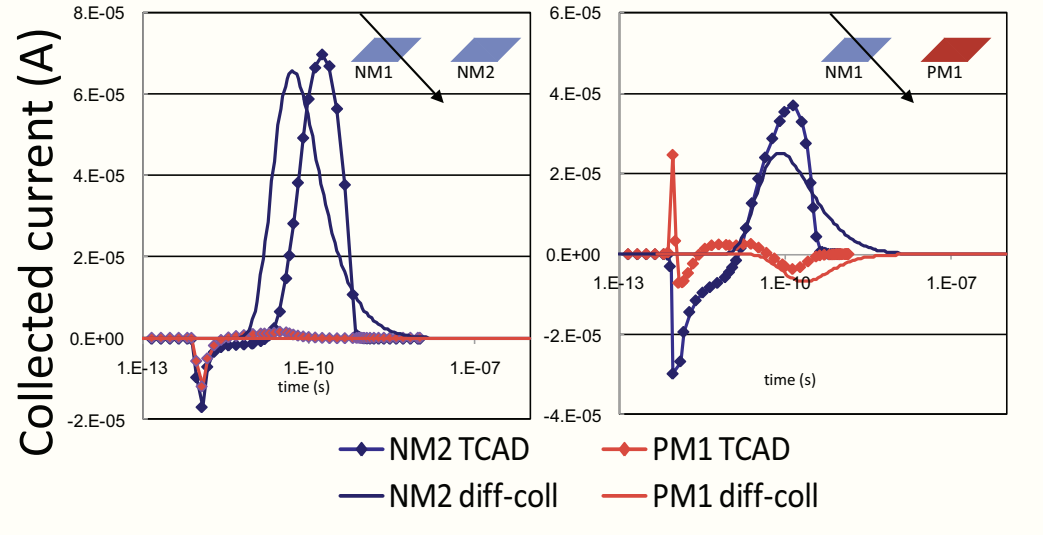

Figure 4.10: Comparison between TCAD ion-induced current pulses and diffusion-collection model for ion strike in the NM1 towards NM2 (a), and ion strike in the NM1 towards PM1.

Diffusion-collection current pulses showed a good agreement with TCAD simulation data. The discrepancies between current pulses are due to: 1) the fact that the analytical model assumes the abrupt and

perfectly biased Nwell/P-well boundary (during ion-induced SET) and 2) that the ion track does not account for the ion spatial distribution of charge. Nevertheless, this agreement is very satisfactory keeping in mind the simplicity of the model. Noteworthy is the execution time of the analytical approach when compared to TCAD simulation. For this particular structure, the simulation time gain is equal to about 5 orders of magnitude (TCAD CPU time sin13h vs. analytical model CPU time sin5s using the same hardware). Figure 4.11 shows the evolution of the collected charge by NM2 and PM1 as a function of the roll angle computed using the analytical approach. The available TCAD data are shown in the figure for comparison purpose (0deg, 270deg, and 360deg). The maximum of collected charge by NM1 transistor is observed for 0deg/360deg of roll (impact towards NM2) and minimum for sin270deg (maximum of PM2 collection).

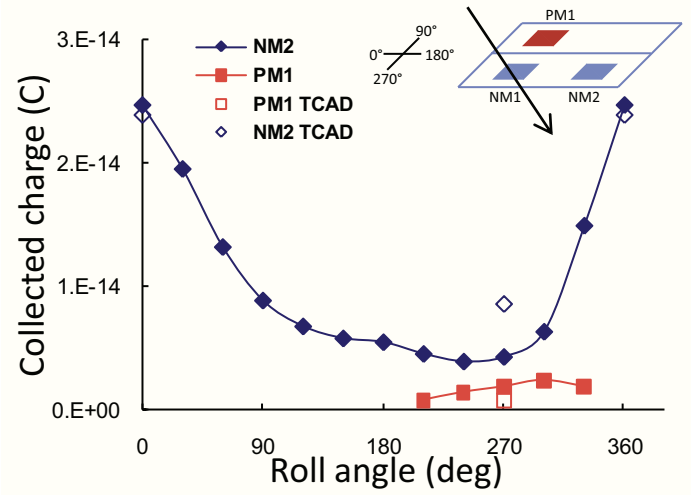

Figure 4.11: Collected charge by redundant nodes as a function of roll angle obtained from TCAD simulations and diffusion-collection equations.

First analytically-obtained ion-induced current pulses showed good agreement with TCAD data and second, the charge sharing in one well and via well boundary confirmed the relevance of the analytical approach. In the next paragraph the TIARA Monte-Carlo simulations will be performed using thousands of ion impacts.

3.2 TIARA assessment of charge sharing

Charge collection after an ion strike in a RHBD Latch

An example of transistor drain placement of DICE Latch (Master Stage of analyzed FF) is shown in Figure 4.12(right); the rectangles show the drain areas for one static configuration, the white rectangles are forward-biased drains, the filled ones show the sensitive reverse-biased drain junctions connected to two redundant nodes N1 (blue) and N2

(red), respectively. The red point depicts the simulated strike.

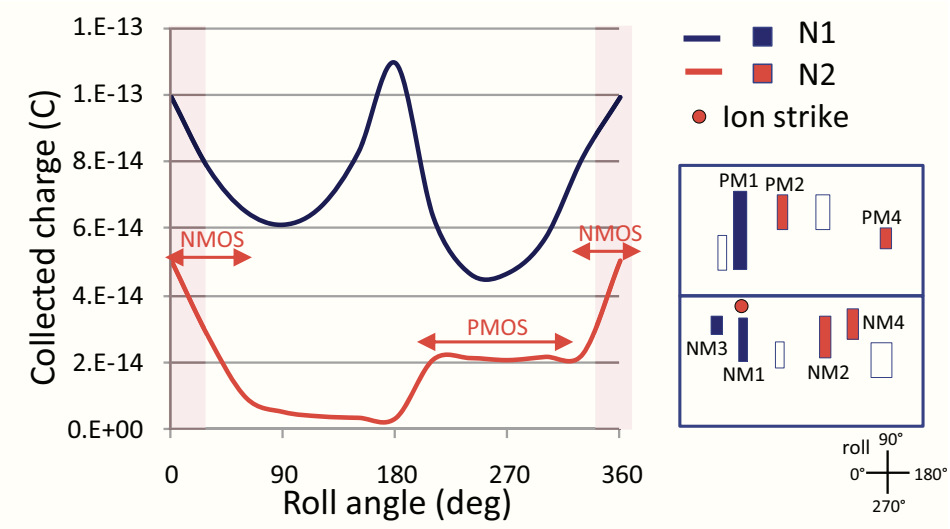

Figure 4.12: Collected charge by redundant nodes as a function of roll angle. Red areas show the roll angles for which upset occurs. On the right, the simplified simulated FF structure is shown: the white rectangles show forward-biased drain areas, blue and red rectangles the reverse-biased drains and a red point simulated ion strike.

The parasitic current pulses due to the ion impact with LET=15 $MeV \cdot cm^2/mg$ and tilt=30deg are computed for all reverse-biased drains and are converted into charge by integrating the current over time. Figure 4.12(left) shows the sum of collected charge on both redundant nodes N1 N2 as a function of the roll angle. The biggest charge is collected by the closest transistor to the impact (NM1). The overall maximum of charge on both nodes is collected for roll 0deg by the pair NM1/NM2 and for 180deg by the pair NM1/NM3 which corresponds to the impact along X-axis (P-well orientation). It is considered that the junction N-well/P-well is a barrier for carrier diffusion, so the part of an ion track traversing the Nwell is not taken into account in parasitic current computation for NMOS transistors. This causes the minimum for impact in Y-axis direction (90deg/270deg).

In order to upset the cell, a charge has to be collected on both redundant nodes N1 and N2. While analyzing the collected charge on N2, largest collected charge for NM2 and NM4 is observed for 0 and 360 degrees on one hand and for PM2 for angles between 200 and 320 degrees on the other hand. The roll angle ranges between 0deg-45deg and 345deg-360deg in Fig. 8 show the angles for which upsets occur. Collected charge by PMOS drains is not sufficient in this case to corrupt the stored value. More ionizing ions are needed to upset the FF due to PMOS charge collection.

Monte-Carlo charge sharing simulations

Charge collection by multiple nodes and its impact on the RHBD FF cross section is analyzed in this section. Heavy-ion strikes have been generated for all tilt and roll angles and collected charges by NMOS and PMOS transistors are computed. The total ion-induced charge on N1 or N2 is equal to the sum of the collected charges by the transistors connected to the considered node (ex. the reverse-biased transistor memorizing the logic sate, additional collection surfaces of the reset/set transistors or clock transmission gate transistors connected via metallization layers to the sensitive node).

Simulation assumption for SEU occurrence due to NMOS-NMOS charge sharing is that charges collected by NMOS drains on both nodes N1 N2 are superior to those collected by PMOS drains. Similarly, we count an SEU due to NMOS-PMOS charge collection when a largest charge is collected by NMOS transistors on one node and the charge collected by PMOS is superior to the charge collected by NMOS on the redundant node. The definition of PMOS-PMOS and PMOS-NMOS charge sharing is straightforward. Figure 4.13 presents the number of SEU due to NMOS-NMOS/PMOS-PMOS and NMOS-PMOS/PMOS-NMOS charge sharing as a function of the LET. The ratio of upsets due to the charge sharing in the same well for this simulated RHBD FF is plotted. For low LET values, this ratio is close to 100% and decreases for increased LET down to 85% for a LET of 70 MeV.cm2/mg. Upset probability due to charge sharing in the same well is at least 5 times higher when compared to charge collection by different transistor types. These data show that, the transistor placement can be separately analyzed for different wells. The design weaknesses in the same well have to first be optimized as they are the most critical for robustness. In [99], the overall error rate is shown to be almost equally dependant on mixed transistor type events and those from NMOS and PMOS only.

Nevertheless, these results can be explained by the differences in the layout of FF. The distances between NMOS-PMOS seem to be much smaller than distances between NMOS-NMOS or PMOS-PMOS transistors, while the design presented in this study is dense and these distances are minimized.

3.3 TIARA-driven transistor placement

Three different transistor placements are proposed for the master stage of the FF. They are obtained by analysis of TIARA simulations results and by optimization of the most vulnerable transistor pairs detected by the simulation. We optimize separately NMOS transistor placement (Figure 4.14(b)) and then PMOS transistor placement (Fig 10c). As the

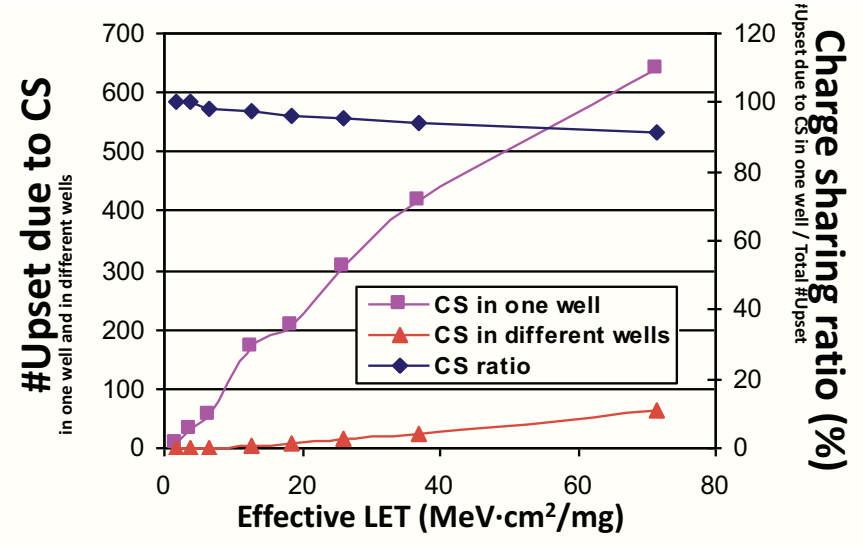

Figure 4.13: Number of upsets due to the NMOS-NMOS/PMOS-PMOS and NMOS-PMOS/PMOS-NMOS simultaneous charge collection as a function of LET. Additionally, the NMOS-NMOS/PMOS-PMOS charge sharing ratio is plotted.

NMOS-NMOS/PMOS-PMOS charge sharing is found to be the most probable upset mechanism, the NMOS-PMOS charge sharing is not mitigated.

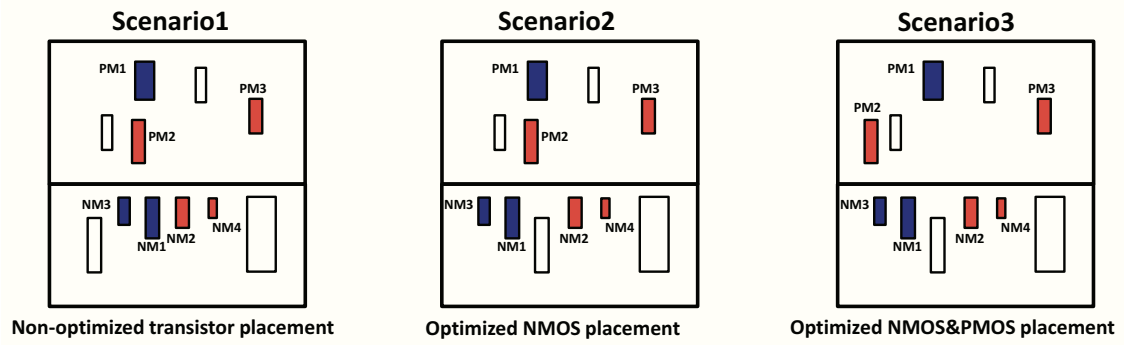

Figure 4.14: Three different transistor placement scenarios: initial RHBD FF layout (a), structure with optimized NMOS transistor placement (b), structure with optimized NMOS PMOS transistor placement.

In scenario 2, one of the forward-biased transistors is placed between the sensitive nodes of the Flip-Flop, thus increasing the nodal separation between N1 and N2. This layout change does not result in an increase of total cell area. In scenario 3, additionally to the previous modification, PM2 is moved to increase the separation with respect to PM1. This results in an area increase of the FF master stage by 14%.

For all transistor placement scenarios, the NMOS-NMOS/PMOS-PMOS upset ratio is plotted in Figure 4.15. This ratio decreases as a function of

LET and decreases for the three proposed structures, as it is expected while the NMOS-NMOS/PMOS-PMOS upset number is reduced and SEU number due to NMOS-PMOS charge sharing remains almost unchanged.

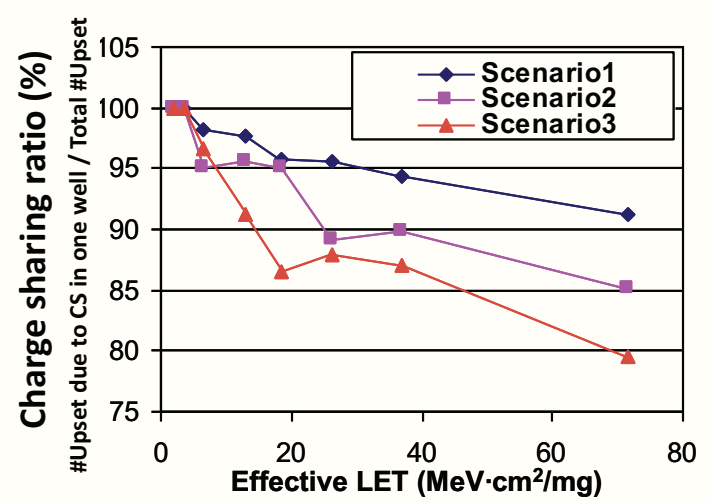

Figure 4.15: NMOS-NMOS/PMOS-PMOS charge sharing ratio for three different transistor placements presented in Figure 4.14.

The simulated heavy-ion cross-sections as a function of effective LET value of the three scenarios are shown in Figure 4.16. For TIARA simulation results presented in Figure 4.16, LET threshold value is defined as the effective LET corresponding to 5% of the heavy-ion cross-section at saturation. The calculated threshold LET (LETth) values are the following: 15 MeV.cm2/mg for Scenario1, 17.3 MeV.cm2/mg for Scenario2, and 22.5 MeV.cm2/mg for Scenario3, which means a maximum increase of 50% in LETth between the three scenarios. As it can be seen at high LET, the different scenarios do not have a significant impact on circuit sensitivity since the nodal separation in these cases was moderate to minimize the cell area overhead.

3.4 Conclusion

The diffusion-collection model implemented in TIARA Monte-Carlo platform allows conducting a complete analysis of charge sharing at multiple nodes of RHBD Latches and Flip-Flops. This model showed good agreement with TCAD simulations for tilted ions and for different roll angles. Moreover, it reduces by 5 orders of magnitude simulation execution time compared to 3D TCAD simulation. TIARA simulations additionally reproduce the experimental heavy ion cross-sections for the 65 nm CMOS DICE-like FF. The simultaneous charge collection by transistors located in one well (N-well or P-well) have been found to be at least 5 X more important than charge sharing via well boundary. Finally, tran-

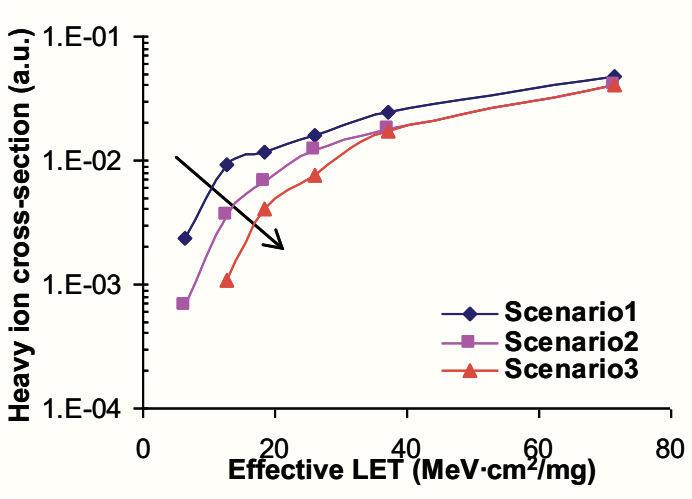

Figure 4.16: Heavy ion cross-sections as a function of LET for three proposed transistor placement scenarios.

sistor placements in each well have been modified by increasing nodal separation between circuit sensitive nodes while minimizing the area overhead. The modified FF layout showed an increase of LET threshold up to 50%.

4 Focus on terrestrial environment and effect of neutron spectra on Neutron Soft Error Rate

In chapter 2 section 2.4 (Environment models), the environment module architecture was presented together with the interface data format that is used to exchange the information between reaction databases and TIARA. This module has been enhanced by different neutron-silicon interaction databases that are compiled with GEANT4. TIARA ability to compare different white beam spectra and mono-energetic neutron sources is discussed in this section. A detailed analysis of the nuclear reactions as well as secondary products as is carried out. Then, the simulation results and comparison with experimental characterizations for the 65 nm SRAM memory measured at TRIUMF is presented. Finally, different SER characterization methods are discussed and its impact on the neutron Soft Error Rate.

4.1 GEANT4 nuclear reaction databases

In order to analyze the soft errors due to neutrons, neutron-silicon (n-Si) reactions databases have been created using a dedicated GEANT4

application with different atmospheric-like neutron spectra: the terrestrial reference New York City JEDEC neutron spectrum [12], the neutron source of LANSCE ICE House [148] and the TRIUMF Neutron Facility neutron source at the University of British Columbia [146]. All spectra are compared in Figure 4.17. Additionally, we consider the different mono-energetic sources used for neutron SER computation in the previous JEDEC specification [117]: 14, 50, 100, and 150 MeV mono-energetic neutron sources.

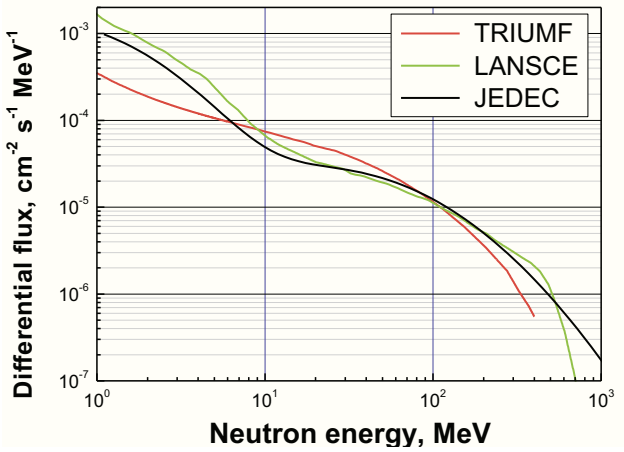

Figure 4.17: Terrestrial high-energy neutron spectrum JESD89A compared to LANSCE and TRIUMF spectra. Distributions are normalized to the integral flux above 10 MeV as in [149].

For compilation of n-Si databases, the GEANT4 4.9.4p01 release has been used [145]. All physical processes employed in simulation are based on the standard physics package QGSP_BIC_HP [147] that includes among others hadronic interactions, high energy interactions and nuclear capture. The complete list of G4 classes that is considered for general purpose neutron-silicon interactions is synthesized in Table 4.5. Concerning the hadronic interactions, in QGSP group of physics lists the quark gluon string model is applied for high energy interactions of neutrons. The high energy interaction creates an exited nucleus, which is passed to the pre-compound model describing the nuclear de-excitation.

For accurate generation of neutron flux according to the distributions, the different neutron source models have been developed using the General Particle Source (GPS) G4 class. Simulated GEANT4 silicon target structure depth (20μm) corresponds to the depth of silicon and passivation layer used for TIARA simulation. In the reaction database, all n-Si reactions from simulation of $5 \cdot 10^8$ neutrons incident perpendicularly to the target surface are recorded (both elastics and non-elastic interactions) for which the ionizing products generate charge higher

Neutron process	Energy range	GEANT4 model	Dataset
Elastic	< 20MeV	G4NeutronHPElastic	G4NeutronHPElasticData
	> 20MeV	G4LElastic	-
Inelastic	< 20 MeV	G4NeutronHPInelastic	G4NeutronHPInelasticData
	[20MeV, 10GeV]	G4BinaryCascade	-
	[10GeV, 25GeV]	G4LENeutronInelastic	-
	[12GeV, 100TeV]	QGSP	-
Fission	< 20 MeV	G4NeutronHPFission	G4NeutronHPFissionData
	> 20 MeV	G4LFission	-
Capture	< 20 MeV	G4NeutronHPCapture	G4NeutronHPCaptureData
	> 20 MeV	G4LCapture	-

Table 4.5: List of the employed GEANT4 classes in the compilation of the n-Si reaction databases.

than 0.5 fC in silicon.

We assume that perpendicular incidence approximates well the accelerated experiments. When the charge generated by secondary products is inferior to 0.5fC, the ion strike cannot cause a bit-flip because the critical charge values for the most sensitive FFs for this technological node are in the range of several fC. The boundary of 0.5fC had to be considered because of the important number of elastic reactions for which the secondary silicon atom kinetic energy is extremely low (0.5fC corresponds to ≈40keV) and thus cannot induce a bit-flip. Additionally, for each reaction, its position is recorded together with all secondary ionizing products (except electrons and pions), their energies, and momentum. The main characteristics of the different databases are summarized in Table 4.6.

Neutron source	Total number of events[1]	Total number of secondary products[2]
14 MeV	75049	101545
50 MeV	68642	105741
100 MeV	49961	90808
150 MeV	37380	81985
JEDEC	66364	93715
TRIUMF	61077	84509

[1]Elastic + inelastic events
[2]Silicon recoil nuclei (E > 40keV) + secondary ions

Table 4.6: Basic Information of the databases generated from the irradiation of a silicon target (1cm x 1cm x 20μm) with $5 \cdot 10^8$ neutrons.

4.2 Nuclear event analyses

Figure 4.18 through Figure 4.21 present the detailed analysis of the G4-extracted databases contents for different neutron energy spectra. The proportion of secondary ions in different n-Si reaction databases as a function of secondary atom is presented in Figure 4.18 (the elastic scattering has not been accounted for). The analogous results were presented in [150] and stay in perfect agreement with our G4 simulation. The secondary ion products are a strong function of energy spectrum: for 14 MeV neutron source, the only products that appear in the data base are Hydrogen, Helium, Magnesium, Aluminum and Silicon. The only reaction that we did not observe and that energy threshold is inferior to 14 MeV is $_{21}$Ne+$_{2}\alpha$ with threshold equal to 12.99 MeV [150]. With neutron spectra energy increase further secondary atoms can be created as Fluor, Beryllium and Phosphor created from silicon (30Si) capturing the incident neutron and decaying by beta emission.

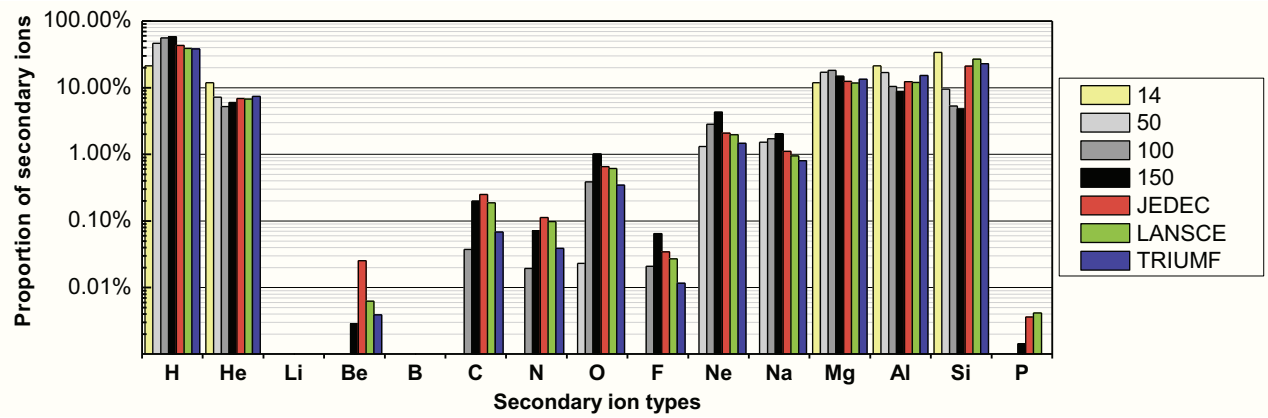

Figure 4.18: Proportions of secondary ions (excluding ion elastic scattering) in the G4 compiled databases for the considered neutron spectra: mono-energetic (14, 50, 100, 150 MeV) and atmospheric-like (JEDEC, TRIUMF and LANSCE).

Figure 4.19 presents the shower distribution as a function of number of ion in the shower. These results take into account both inelastic as well as elastic scattering. The 14 MeV neutron source provokes reactions with the multiplicity up to 2 secondary particles, the 50 MeV source up to 4, TRIUMF spectrum. The shower multiplicity as well as apparition of some atoms in Figure 4.18 can be directly liked with the cut-off energies of the that are different for TRIUMF producing the beam from irradiation of lead absorber with protons up to 500 MeV and LANSCE that used a spallation of heavy metal target by 800 MeV protons.

In Figure 4.20, the ratio of reaction type is shown for different sources. Generally, for atmospheric like neutron spectra, the elastic scattering is

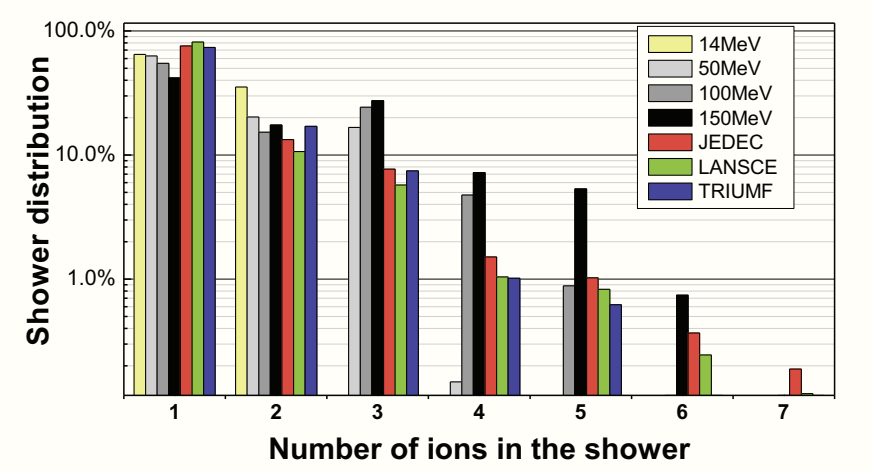

Figure 4.19: Particle shower distribution as a function of particle shower multiplicity. Elastic recoil events are taken into account in this distribution with a multiplicity of one.

the dominant part because of high fluxes of relatively low-energy neutrons that cannot cause a nuclear reaction since the incident neutron energy is lower than the nuclear reaction energy threshold. The inverse situation is observed for mono-energetic neutrons for which nuclear reactions are dominant.

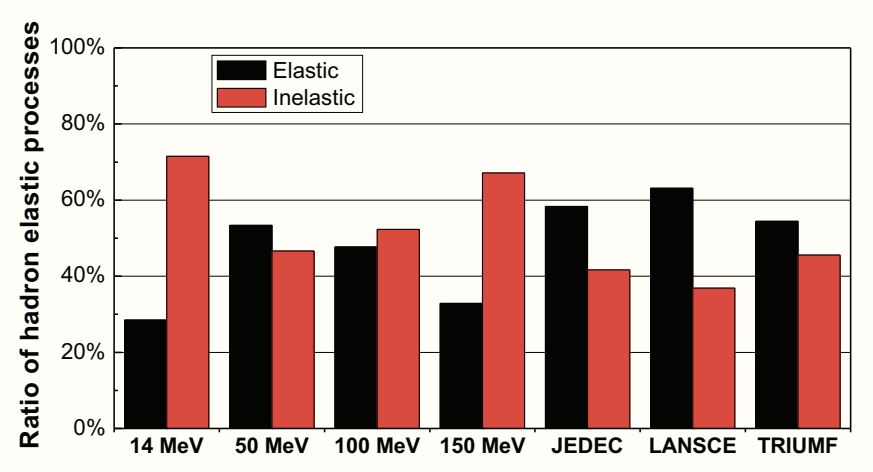

Figure 4.20: Percentages of elastic and inelastic processes for different neutron spectra.

Figure 4.21 presents percentages of secondary ions as a function of energy and as a function of secondary atom for all mono-energetic and continuous neutron spectra databases. In addition, 1 MeV database plot has been added in order to better explain high percentages of low energy silicon atoms for TRIUMF, JEDEC and LANSCE that, as already mentioned before, are produced by high fluxes of low energy neutrons

which are subjected only to elastic reactions. These fluxes are the highest for LANSCE (see. Figure 4.17) therefore <1 MeV Si contribution is the highest. On the other hand for both JEDEC and TRIUMF, the percentage of high energy ions (1-10 MeV) is much higher than for LANSCE (≈35% vs. ≈27%).

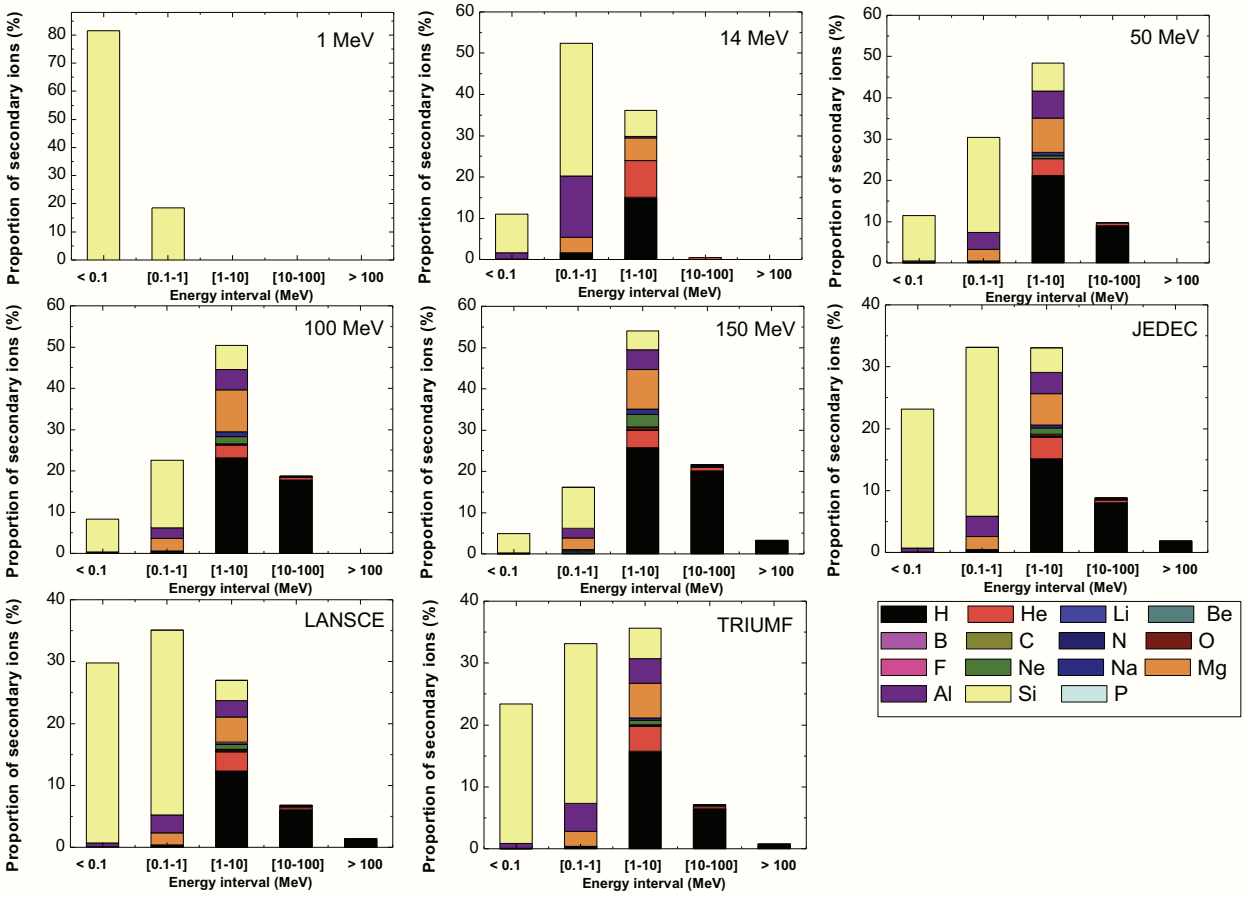

Figure 4.21: Energy histogram for the secondary ion cocktails (from Figure 4.18) produced by n-Si interactions for the different neutron sources.

4.3 Influence of different neutron energy spectra on neutron SER

This section describes TIARA simulations carried out with different continuous and mono-energetic neutron spectra that are compared with experiments performed at TRIUMF and at PSI radiation facilities. According to JESD89 specification [117], Soft Error Rate testing can be performed using atmospheric-like neutron spectra or alternately, using mono-energetic neutron or proton sources. JESD89 [117] specifies four neutron energies allowing the extraction of neutron device cross-sections and the SER by convolving the differential neutron energy spectrum with the experimental data:

$$SER = 1024 \cdot 1024 \cdot 10^9 \cdot (3.86 \cdot \rho(14MeV) \cdot 3.86 \cdot \rho(14MeV) \cdot 3.72 \cdot \rho(50MeV) \cdot 1.83 \cdot \rho(100MeV) \cdot 3.93 \cdot \rho(150MeV))$$

where ρ is the neutron cross section. TIARA simulations with all above mentioned spectra have been performed and are presented in Figure 4.22 together with experimental proton characterizations. As it can be seen, simulated neutron cross-sections are in good agreement with proton test results for energies above 50 MeV. The discrepancy between neutrons and protons for 14 MeV is expected for which the cross-sections cannot be considered similar. The difference of x7 that is observed in this study is similar to data presented in the literature [154] for SRAM memories.

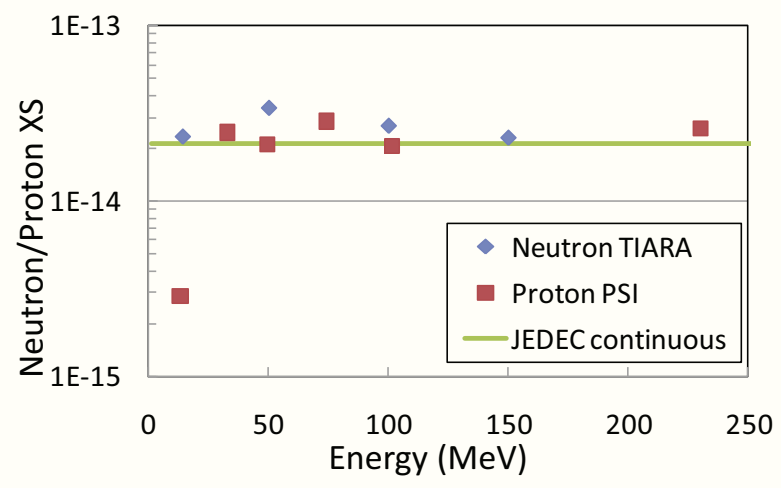

Figure 4.22: Simulated neutron cross-sections obtained using mono-energetic neutron sources compared to proton test results from experimental measurements at PSI. The continuous JEDEC cross-section from TIARA simulation has been superposed for comparison purpose.

Figure 4.23 shows experimental SER results for standard FF obtained using Equation 4.1 from mono-energetic proton testings performed compared with two TIARA neutron simulations: first, using reference JEDEC spectrum and second, SER computed using Equation 4.1. Experimental data show underestimation of 22% when compared to the reference JEDEC spectrum while SER obtained from mono-energetic Neutron simulation overestimates JEDEC value by 19%. The difference between SER from mono-energetic proton measurements and mono-energetic neutron simulations is caused by the differences between proton-Silicon and neutron-Silicon reactions [154]. As far as mono-energetic proton experiments and JEDEC are compared, several studies previously showed similar differences between discrete energy proton/neutron tests and continuous neutron spectra citeBaggio04, Dodd04. In [152], the experimental comparisons on 8 different devices show a

discrepancy range from -27% to +8% between atmospheric-like LANSCE spectrum and SER obtained from mono-energetic proton tests with an average error equal to -12%. In [153], the average underestimation is equal to 13%.

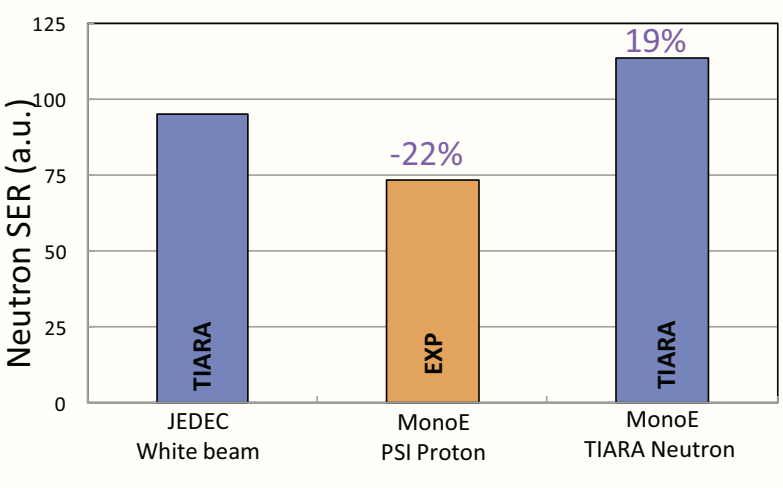

Figure 4.23: Simulated SER using reference JEDEC neutron spectrum, experimental SER obtained from proton PSI measurements and simulated SER obtained from studied mono-energetic neutron sources.

In Figure 4.24, TIARA simulation results for three atmospheric-like neutron spectra are compared with experimental measurements performed at TRIUMF radiation facility (for STD FF). TIARA simulation results and TRIUMF measurements are in very good agreement (3%). When comparing simulation for different neutron spectra, it is seen that TRIUMF results slightly overestimates the value estimated using JEDEC spectrum (8%) while LANSCE underestimates this value by 14%. These differences are caused by different secondary products for different database energies. As far as JEDEC and TRIUMF are compared, the secondary product energy spectra and product composition is similar, while for LANSCE, there are more elastic reactions caused by higher fluences for low energetic neutrons. Very similar trends have been recently reported by Slayman [151] by comparing SER from different radiation facilities with value expected from JEDEC neutron spectrum.

5 TIARA projections on future technologies

Finally, TIARA simulation capabilities to anticipate reliability of next CMOS technologies is illustrated in this section on SRAM memories downto 20nm technological node and RHBD FF designed in 32nm technology.

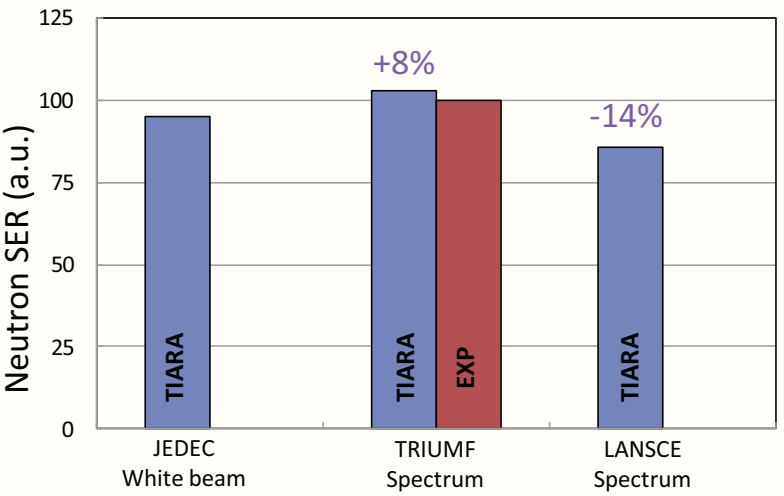

Figure 4.24: Simulated SER using the studied continuous neutron spectra compared to the experimental SER from measurements at FRIUMF.

5.1 32nm SRAM test vehicle and experimental measurements

A test chip was designed and manufactured by STMicroelectronics in bulk 32 nm low power CMOS technology with both twin- and triple-well process options. The die dimensions are $4.6 \cdot 5.2\ mm^2$ and its nominal supply voltage is equal to 1.0V. The test vehicle embeds more than 10Mbit of standard- and high-density, single- and dual-port SRAMs as well as representative standard devices from ST production libraries. It was originally designed and manufactured for validation and qualification of the process.

The heavy ion experiments were carried out at the RADEF [79] radiation facility in compliance with the ESA test specification ESCC Basic Specification No. 25100 [14]. The species used for these experiments were Nitrogen, Neon, Argon, Krypton, and Xeon. During the tests, the SRAMs were programmed with different test patterns and their static and dynamic heavy ion cross-sections were measured as a function of ion LET, temperature and supply voltage.

Figure 4.25shows the heavy ion cross-section for four types of tested devices: single-port high-density ($0.149\mu m^2$ bit-cell), single-port standard-density ($0.187\mu m^2$ and $0.244\mu m^2$ bit-cell), and dual-port register file ($0.310\mu m^2$ bit-cell). All four SRAM architectures exhibit similar heavy ion with variations not exceeding factor 3 between most sensitive and less sensitive of the memories. In contrary to the previous technologies (as 65nm SRAM cross-section presented in [83]) for which the high-density SRAMs were more sensitive to heavy ions, this measurements show that the bigger cell area, the higher cell sensitivity. Experimental

measurements were performed for power supply voltages ranging between 0.9V and 1.1V.

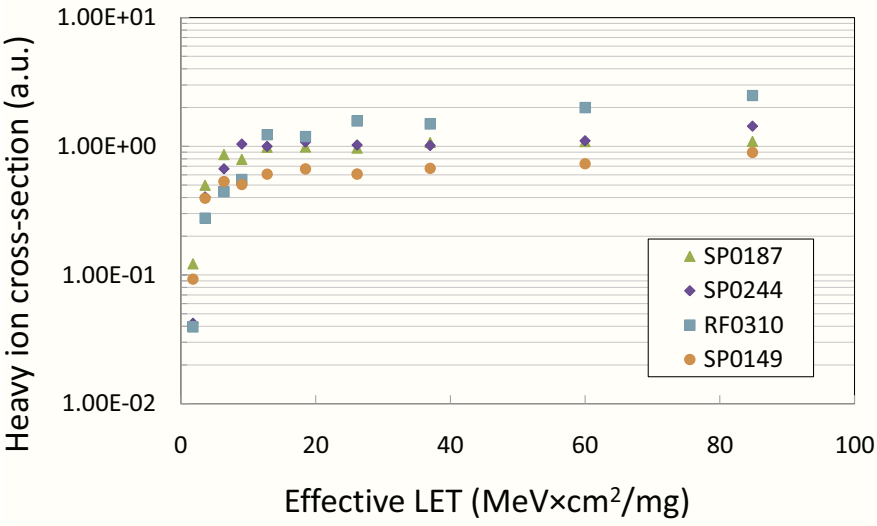

Figure 4.25: Experimental heavy ion cross-sections as a function of effective LET value for tested memory cuts: single- and dual-port bitells (bitcell areas from 0.149μm^2 to 0.310μm^2).

5.2 TIARA 32nm SRAM simulation and comparison with experiment

For TIARA simulations in this section, full SPICE simulations are used as the upset criteria, the obtained ion-induced current pulses for all transistors impacted by an ion strike are injected in the SRAM netlist in order to determine the upset occurrence. The ambipolar diffusion coefficients D for both p-substrate, N-well and the average carrier velocities via space charge regions of NMOS and PMOS drains, carrier lifetimes, the critical LET values for NMOS and PMOS transistor drains for previous technology nodes (Bulk CMOS 130nm down to Bulk CMOS 45nm technology) have been calculated using full 3D TCAD simulations of ion strikes from the Sentaurus Synopsys package [89]. For the 32nm technology, as the day of writing this dissertation, the doping profiles adjusted with the technology process were not available. Thus, all parameters have been analytically extrapolated for ST 32nm technology from the previous technological nodes.

The upset occurrence has been computed using full SPICE simulations with SRAM post-layout netlist with parasitic and transistor models from ST Bulk 32nm LP Process Design Kits (PDKs).

Figure 4.26 shows the comparison between experimental and simulated cross-sections as a function of the effective LET for high-density

single-port memory processed with twin well. Very good agreement at low LET values is observed (<20 $MeV \cdot cm^2 \cdot mg^{-1}$). For higher LETs (>20 $MeV \cdot cm^2 \cdot mg^{-1}$), the simulation slightly overestimates the experimental points (<50%). These cross-sections are plotted in events since large MCU events cannot be predicted without accurate bipolar amplification modeling. The overall good agreement between TIARA results and experimentally obtained data confirms the validity of extrapolated charge transport parameters (ambipolar diffusion coefficients, carrier collection velocities).

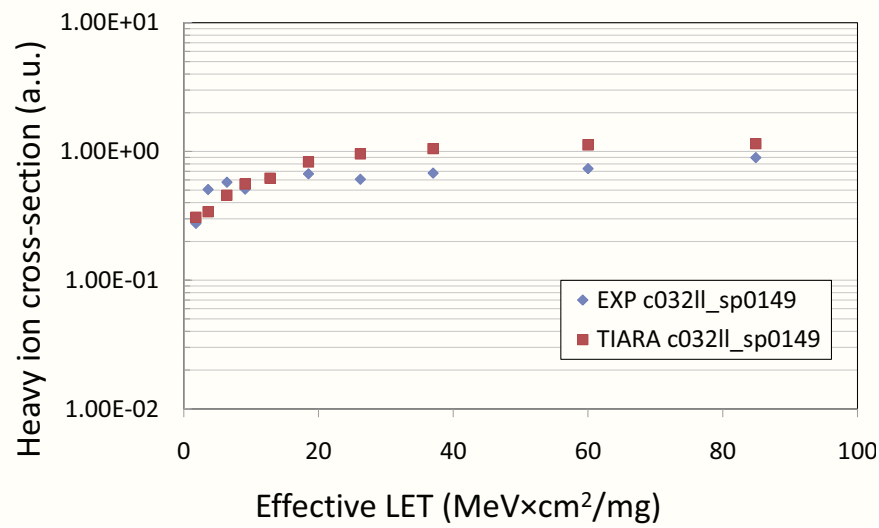

Figure 4.26: Agreement between simulated and experimental heavy ion cross-sections in events as a function of effective LET value for single-port high-density bitcell.

5.3 Anticipation of 20nm SRAM technology with TIARA

TIARA simulation platform architecture does not require calibration with the experimental tests in order to do simulations and benefits from the availability of all technological process data, calibrated transistor models and industrial designs. In the case of 20nm technology, the technological process is not yet stable but the studies presented in previous sections showed that analytical parameter extrapolation using prior technological nodes allowed for obtaining sufficiently accurate charge transport parameters for 32nm technology. The charge transport parameters have been thus extrapolated similarly for 20nm technology. The 20nm bit-cell geometry which bit-cell area is equal to $0.073\mu m^2$ has been obtained from GDS file and cell electrical response is modeled using the dedicated SPICE netlist with ST PDK models. The comparison between simulated SEU heavy ion cross-sections for 32nm and 20nm SRAMs in events, presented in Figure 4.27, show a decrease for 20nm when compared to previous technological node by 11-17%.

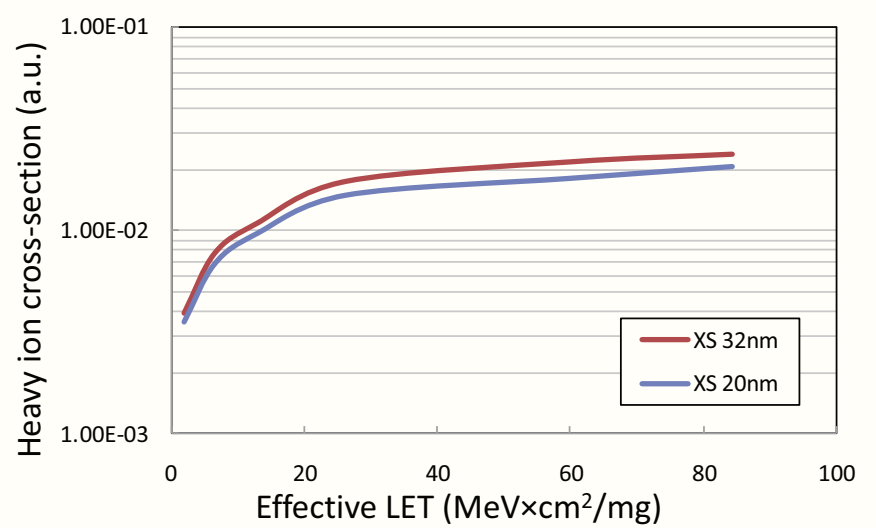

Figure 4.27: Comparison between TIARA-simulated heavy ion cross-sections for high-density SRAM memories in 32nm and 20nm CMOS technologies.

5.4 DICE FF robustness assessment in 32nm compared to 65nm technology

TIARA simulation capabilities accounting for charge sharing and hardening techniques by simulation-driven transistor placement on Dual-Interlocked Storage Cell (DICE) FFs manufactured in 65nm CMOS process were shown in section 3 and 4 of this chapter and have been validated with experimental measurements. In previous paragraph of this section, the comparisons between TIARA and experience confirmed the relevance of the modeling approach for 32nm CMOS technology. Based on these assumptions, TIARA simulations have been performed on DICE-like FFs designed in 32nm to evaluate if this architecture proposes satisfying hardening solution against radiation for this technological node.

TIARA simulations are based on the same set of charge transport parameters as SRAMs simulations, on GDS of a 32nm DICE-like FF designed using the ST design rules and a post-layout SPICE netlist with parasitics using the PDK transistor models. Figure 4.28 presents the heavy ion cross-sections for this new 32nm FF designed in Dual-Height Cell (DHC) technology and compared to TIARA simulations of the analogous RHBD FF manufactured in 65nm technology. All possible FF static configurations have been simulated, i.e. all combinations of clock and data signals. As it can be seen in Figure 4.28, for two out of four FF configurations 32nm FF is less sensitive than the 65nm FF and for one more sensitive. These differences are caused by design particularities and transistor placement within each structure. Nevertheless, the average

cross-section over all configurations gives very similar design sensitivity in both cases, thus confirming the effectiveness of DICE structure for this technology node.

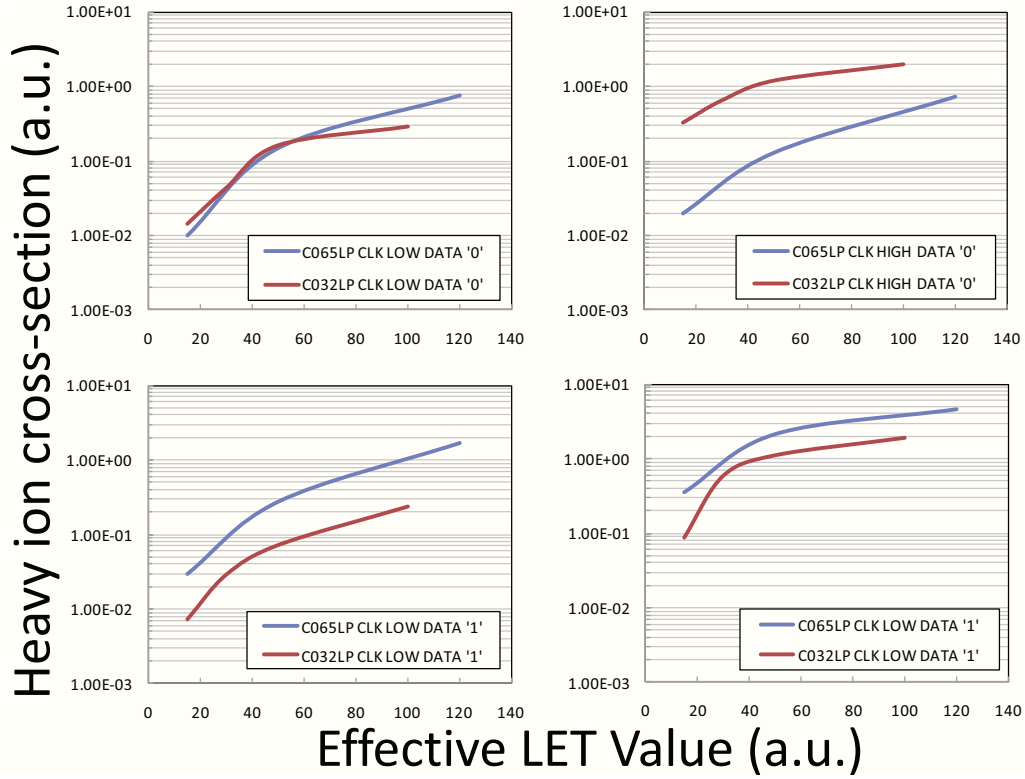

Figure 4.28: Comparison between TIARA-simulated heavy ion cross-sections as a function of effective LET value for all FF configurations for Dual-Height Cell DICE-like FF architectures designed in 65nm and 32nm CMOS technologies.

6 Conclusion

This chapter presented TIARA capabilities allowing for insights in SEE effects in highly integrated CMOS technologies:

- Studies of ever increasing with technology downscaling charge sharing showed that charge sharing is five times more important in one well than via well boundary. The boundary acts as a charge diffusion barrier. Based on this result, the cell hardening techniques by nodal separation were proposed.
- The evaluation of dual-height cell technology showed the increase in cell hardness by factor x21 on STMicroelectronics' designs without area overhead and was successfully compared to the values in literature.

- The in-depth analysis of neutron-induced upsets in standard- and radiation-hardened-by-design FFs revealed different mechanisms leading to bit-flips: dominant elastic scattering for standard FF while inelastic scattering for space redundancy-based FFs.
- Neutron measurement techniques and their impact on Soft Error Rate were evaluated for continuous atmospheric-like neutron spectra of LANSCE, TRIUMF and JEDEC and were compared with SER simulations from mono-energetic neutron sources. TRIUMF spectrum was found to be in the best agreement with JEDEC, while LANSCE and mono-energetic measurement techniques exhibit underestimation of respectively 14% and 32%.
- Finally, the SRAM heavy-ion sensitivity down to 20nm is anticipated and was found to be lower than for 32nm technology by sin15%. DICE effectiveness was assessed for 32nm CMOS technology and TIARA simulations showed similar sensitivity to heavy ion radiation to design in 65nm.

Conclusions

This work was focused on the development and industrial integration of a Monte-Carlo simulation platform named Tool suite for rAdiation Reliability Assessment (TIARA). TIARA was designed to be used from the early technology development phases without the necessity of calibration with experimental results. In addition, the platform benefits from the availability of all technological data that are in possession of a chip manufacturer as accurate process doping profiles, calibrated with silicon measurements transistor PDK models and numerous industrial designs. The major platform requirements include supporting simulation of any digital circuit architecture, supporting various technological nodes, modeling of space and terrestrial radiation environments, possibility of evaluation and validation of hardening techniques.

Innovative TIARA architecture described in detail in this work meets all above mentioned platform requirements. A modular platform architecture facilitates code maintenance and future developments. The environment module allowed for simulation of different radiation environments which consist of heavy ions, alphas, neutrons and protons. Transport models including the refined diffusion-collection equations and new drift current model were presented. New bit-flip occurrence criteria were developed and pioneering coupling solutions between TIARA and IC CAD environment were proposed. In addition, TIARA implementation on a distributed system and in graphics processing unit for massive simulation parallelism optimized run time to give a fast feedback on designed cell for hardening purposes.

TIARA was then extensively verified by comparisons with real time and accelerated experimental measurements for all radiation environments and very good agreement was found on a very large LET range showing the relevance of model assumptions. This validation was carried out on several technological nodes, using multiple test vehicles manufactured by STMicrolectronics and a wide set of cell architectures ranging from different SRAM bit-cells (5 architectures), through standard Flip-Flops (4 cells) to radiation-hardened-by-design circuits (2 designs). This has highlighted TIARA capacity to simulate any digital circuit if layout and spice netlist are available. Analysis of different strategies for modeling of the MCUs has lead to selection of the most adapted

models and showed good agreement with experimental tests for SRAM memories manufactured in twin well process option. In order to extend TIARA usage to simulation of triple-well process option, a model of parasitic bipolar amplification was proposed but is not yet fully validated with experimental data. Additional TIARA capabilities accounting for the analysis of the influence of temperature, power supply voltage and process corners were demonstrated on a 32nm SRAMs.

Moreover, TIARA's ability allowing for in-depth analyses and insights in SEE effects, that address the most actual challenges in design of reliable digital microelectronic circuits in highly integrated CMOS technologies, was shown. TIARA was used to simulate very complex RHBD FFs based on DICE latch with different radiation sources showing excellent agreement with experimental tests. Numerous layout hardening techniques as redundant node separation, the use of dual-height cell technology and different TIARA-driven transistor placements have been investigated in detail with a complete analysis of the mechanisms leading to the upsets confirming diffusion blocking properties of Nwell/Pwell junction. In addition, the extended analysis of neutron radiation influence showed much higher inelastic scattering contribution to the total upset rate of DICE-like structure contrary to the dominant elastic scattering for standard Flip-Flop. Moreover, the influence of different neutron test facilities with continuous and mono-energetic spectra on Soft Error Rate are discussed.

Finally, projections on future CMOS technologies were anticipated using the latest technological data available at STMicroelectronics. Simulations allowed to study the radiation sensitivity of 32nm CMOS technology to heavy ions: first, SRAM simulations were successfully compared with the experimental tests and then, TIARA hardness evaluation was carried out on DICE-based FF in 32nm CMOS and was compared to 65nm technology. DICE FF radiation hardness for both technologies was found to be similar. This proves that despite increased charge sharing, the use of dual-height cell technology and simulation-driven transistor placement allows for exploiting DICE concept in future technological nodes. The anticipation of 20nm CMOS SRAM sensitivity to heavy-ions was performed based on the latest SPICE models, cell geometry and analytical scaling of charge transport parameters.

Most importantly, TIARA simulation platform is extensively used in design of future rad-tolerant and rad-hard CMOS technologies. TIARA has contributed to evaluation and implementation of advanced hardening solutions that could not have been presented in this dissertation because of industrial confidentiality reasons. Furthermore, the integration with CAD environment has allowed to propose direct platform use to IC designers that can work independently on design and analyse cir-

cuit behavior under an investigated radiation scenario.

Future TIARA developments envisage further model implementations as already presented parasitic bipolar amplification validation with experimental measurements in order to be able to expand TIARA use to simulation of digital circuits manufactured with triple-well process option. In addition, the extension of TIARA use to perform the Error Correction Code (ECC) efficiency emulation from the error bitmaps of simulated MCU events in SRAMs could be done. These MCU error bitmaps can be mapped on multiple memory multiplexer solutions and the MUX/ECC efficiency can be assessed. TIARA further extensions to other circuit architectures as analog and mixed-signal IPs has already been initialized and is possible thanks to the modular architecture of TIARA. The developments encompass enhancing carrier transport and collection models to be predictive for the whole power supply range (as it was already done down to 0.35V). Then, TIARA will be able to provide the estimation of ion-induced current pulses in the complete analog/mixed-signal IP. The dedicated upset criteria defining if IP bahavior is in or out of specification should be considered on a case-by-case basis. Moreover, the neutron simulation of new technologies should account for verification of impact of new materials such as the use of oxygen or tungsten as it was shown by the Vanderbilt group. Similarly to the approach proposed by IBM, instead of simulating the whole planes of metals, and silicon dioxide, it would be interesting to obtain direct BEOL geometry from GDS file. From GDS data, the precise percentages of each material in this layer could be computed and using the GEANT4, a device structure composed of a mixture of BEOL materials could be created. From G4 simulation of such a structure, a nuclear G4 database could be constructed for TIARA SER simulation to finally analyse BEOL composition influence on SER.

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Publications

Conference Publications

- S. Martinie, J. L. Autran, S. Sauze, D. Munteanu, **S. Uznanski**, P. Roche, G. Gasiot, "Underground Characterization and Modeling of Alpha-Particle Induced Soft-Error Rate in CMOS 65nm SRAM," RADECS2011, Sevilla, Spain.

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- **S. Uznanski**, G. Gasiot, P. Roche, J. L. Autran, "Combining GEANT4 and TIARA for Neutron Soft Error Rate Prediction of 65 nm Flip-Flops," NSREC2011, Las Vegas, Nv, USA.

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Résumé

L'augmentation de la densité et la réduction de la tension d'alimentation des circuits intégrés rend la contribution des effets singuliers induits par les radiations majoritaire dans la diminution de la fiabilité des composants électroniques aussi bien dans l'environnement radiatif spatial que terrestre. Cette étude porte sur la modélisation des mécanismes physiques qui conduisent à ces aléas logiques (en anglais "Soft Errors"). Ces modèles sont utilisés dans une plateforme de simulation, appelée TIARA (Tool suIte for rAdiation Reliability Assessment), qui a été développée dans le cadre de cette thèse. Cet outil est capable de prédire la sensibilité de nombreuses architectures de circuits (SRAM, Flip-Flop, etc.) dans différents environnements radiatifs et sous différentes conditions de test (alimentation, altitude, etc.) Cette plateforme a été amplement validée grâce à la comparaison avec des mesures expérimentales effectuées sur différents circuits de test fabriqués par STMicroelectronics. La plateforme TIARA a ensuite été utilisée pour la conception de circuits durcis aux radiations et a permis de participer à la compréhension des mécanismes des aléas logiques jusqu'au noeud technologique 20nm.

Mot-clefs

Evénements Singulier, Aléa logiques, RHBD, CMOS, SRAM, Flip-Flop

Abstract

Aggressive integrated circuit density increase and power supply scaling have propelled Single Event Effects to the forefront of reliability concerns in ground-based and space-bound electronic systems. This study focuses on modeling of Single Event physical phenomena. To enable performing reliability assessment, a complete simulation platform named Tool suIte for rAdiation Reliability Assessment (TIARA) has been developed that allows performing sensitivity prediction of different digital circuits (SRAM, Flip-Flops, etc.) in different radiation environments and at different operating conditions (power supply voltage, altitude, etc.) TIARA has been extensively validated with experimental data for space and terrestrial radiation environments using different test vehicles manufactured by STMicroelectronics. Finally, the platform has been used during rad-hard digital circuits design and to provide insights into radiation-induced upset mechanisms down to CMOS 20nm technological node.

Keywords

SEE, SER, SEU, RHBD, Monte-Carlo, CMOS technology, SRAM, Flip-Flop

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