Joint doctorate between the University of "*Modena e Reggio Emilia*" and the University of "*Bordeaux 1*"

Analysis of the physical mechanisms limiting performance and reliability of GaN based HEMTs

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by

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To my wife

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Curriculum Vitae

Education

February 2009	PhD in electronics engineering from the University of "Modena and Reggio Emilia",Italy and from the University of "Bordeaux 1", France.
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Publications

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Abstract

Abstract

This thesis reports the results of an extensive analysis of the physical mechanisms that limit the performance and reliability of gallium nitride (GaN) based High Electron Mobility Transistors (HEMT). In particular:

- High electric field degradation phenomena are investigated in GaN-capped AlGaN/GaN HEMTs by comparing experimental data with numerical device simulations. Under power- and OFF-state conditions, 150-h DC stresses were carried out. Degradation effects characterizing both stress experiments were as follows: a drop in the dc drain current, the amplification of gate-lag effects, and a decrease in the reverse gate leakage current. Numerical simulations indicate that the simultaneous generation of surface (and/or barrier) and buffer traps can account for all of the aforementioned degradation modes. Experiments also showed that the power-state stress induced a drop in the transconductance at high gate–source voltages only, whereas the OFF-state stress led to a uniform transconductance drop over the entire gate-source-voltage range. This behavior can be reproduced by simulations provided that, under the power-state stress, traps are assumed to accumulate over a wide region extending laterally from the gate edge toward the drain contact, whereas, under the OFF-state stress, trap generation is supposed to take place in a narrower portion of the drain-access region close to the gate edge and to be accompanied by a significant degradation of the channel transport parameters. Channel hot electrons and electric-field-induced strain-enhancement are finally suggested to play major roles in power-state and off-state degradation, respectively.
- Traps are characterized in AlGaN-GaN HEMTs by means of DLTS techniques and the associated charge/discharge behavior is interpreted with the aid of numerical device simulations. Under specific bias conditions, buffer traps can produce ‘‘false’’ surface-trap signals, i.e. the same type of current-mode DLTS (I DLTS) or gate-lag signals that are generally attributed to surface traps. Clarifying this aspect is important for both reliability testing and device optimization, as it can lead to erroneous identification of the degradation mechanism, thus resulting in wrong correction actions on the technological process.

- The physical mechanisms underlying RF current collapse effects in AlGaN-GaN high electron mobility transistors are studied by means of measurements and numerical device simulations. This work suggests the following conclusions: i) both surface and buffer traps can contribute to RF current collapse through a similar physical mechanism involving capture and emission of electrons tunneling from the gate; ii) surface passivation strongly mitigates RF current collapse by reducing the surface electric field and inhibiting electron injection into traps; iii) for surface-trap densities lower than 9×10^{12} cm^{-2}, surface-potential barriers in the 1–2 eV range can coexist with surface traps having much a shallower energy and, therefore, inducing RF current-collapse effects characterized by relatively short time constants.
- Current collapse effects are investigated in AlGaN/GaN HEMTs by means of measurements and numerical device simulations. According to pulsed measurements, the adopted devices exhibit a significant gate-lag and a negligible drain-lag ascribed to the presence of surface and buffer traps, respectively. Furthermore, illumination of the devices with two specific wavelengths can result in either a recovering of current collapse or a decrease in the gate current. On the other hand, numerical device simulations suggest that the kink effect can be explained by electron trapping into barrier traps and the subsequent electron emission after a critical electric-field value is reached.

Sommario

Questa tesi riporta i risultati ottenuti da un'ampia analisi dei meccanismi fisici che limitano le prestazioni e l'affidabilità dei transistor ad alta mobilità di elettroni (HEMT) al nitruro di gallio (GaN). In particolare:

- I fenomeni di degradazione ad alto campo elettrico nei GaN/AlGaN/GaN HEMT sono analizzati confrontando i dati sperimentali con i risultati delle simulazioni numeriche. Sono stati effettuati stress DC di 150 ore in condizioni di canale aperto e chiuso. Gli effetti di degradazione che hanno caratterizzato entrambi i tipi di stress sono i seguenti: una caduta nella corrente DC di drain, un'amplificazione degli effetti di gate lag, e una diminuzione della corrente inversa di gate. Le simulazioni numeriche indicano che la generazione simultanea di trappole in superficie (e/o barriera) e buffer può spiegare tutti i suddetti modi di degradazione. Le misure sperimentali hanno mostrato inoltre che lo stress a canale aperto ha causato una caduta della tranconduttanza solo ad alte tensioni V_{GS}, mentre lo stress a canale chiuso ha provocato una caduta della transconduttanza uniforme a tutte le tensioni V_{GS}. Questo comportamento può essere riprodotto con le simulazioni se, nel caso di stress a canale aperto, si assume che le trappole si accumulano lungo un'ampia regione che si estende lateralmente dal bordo di gate verso il contatto di drain, mentre, nel caso di stress a canale chiuso, si suppone che la generazione delle trappole abbia luogo in una più stretta porzione della zona di accesso vicino al bordo di gate e che sia accompagnata da una degradazione significativa dei parametri di trasporto del canale. Infine si propone che gli elettroni caldi del canale e l'aumento di strain indotto dal campo elettrico siano alla base delle degradazioni osservate dopo gli stress a canale aperto e chiuso rispettivamente.
- Le trappole in AlGaN-GaN HEMTs sono caratterizzate usando le tecniche di DLTS e il relativo comportamento di carica/scarica é interpretato con l'aiuto delle simulazioni numeriche. Sotto particolari condizioni di polarizzazione, le trappole di buffer possono produrre falsi segnali da trappole di superficie, ossia lo stesso tipo di segnali I-DLTS e forma d'onda di gate lag attribuiti generalmente alle trappole di superficie. Chiarire questo aspetto è molto importante sia per le prove di affidabilità che per l'ottimizzazione dei dispositivi, in quanto può provocare una errata

identificazione del meccanismo di degradazione, portando ad azioni correttive sbagliate nell'ottimizzazione del processo tecnologico.

- I meccanismi fisici che originano il collasso di corrente RF negli HEMT AlGaN-GaN sono analizzati usando misure sperimentali e simulazioni numeriche. Questo lavoro suggerisce le seguenti condizioni: i) sia le trappole di superficie che quelle di buffer possono contribuire al collasso di corrente RF tramite un simile meccanismo fisico che coinvolge la cattura e l'emissione di elettroni provenienti dal gate; ii) la passivazione della superficie diminuisce fortemente il collasso della corrente RF tramite la riduzione del campo elettrico in superficie e la conseguente diminuzione dell'iniezione di elettroni dal gate alle trappole; iii) per densità di trappole di superficie minori di 9×10^{12} cm^{-2} , barriere di potenziale superficiale di 1-2 eV possono coesistere con trappole di superficie aventi energie relativamente basse e che provocano effetti di collasso di corrente RF caratterizzati da costanti di tempo relativamente corte.
- Gli effetti di collasso di corrente negli HEMT AlGaN-GaN sono studiati usando i risultati delle misure sperimentali e delle simulazioni numeriche. Basandosi sulle misure delle caratteristiche d'uscita impulsate, i dispositivi utilizzati mostrano un evidente gate-lag e un trascurabile drain-lag, attribuiti alla presenza di trappole di superficie e buffer rispettivamente. Inoltre, l'illuminazione dei dispositivi con due specifiche lunghezze d'onda può provocare, in un caso, il ripristino dal collasso di corrente e, nell'altro caso, una diminuzione della corrente inversa di gate. Le simulazioni numeriche suggeriscono che l'effetto kink può essere spiegato dalla cattura di elettroni nello strato barriera e dalla successiva emissione una volta raggiunto un certo livello di campo elettrico.

Résumé

Ce manuscrit présente les résultats d'une analyse exhaustive des mécanismes physiques qui limitent les performances et la fiabilité des transistors à haute mobilité d'électrons (HEMT) sur nitrure de gallium (GaN). En particulier :

- Les phénomènes de dégradation à fort champ électrique des HEMT sur GaN sont analysés en comparant les données expérimentales avec les résultats de simulations physiques. Des stresses DC de 150 heures ont été effectués en conditions de canal ouvert et de pincement. Les effets des dégradations qui ont caractérisé ces deux types de stresses sont les suivants: une chute de courant DC de drain, une amplification des effets de gate-lag, et une diminution du courant inverse de grille. Les simulations physiques indiquent que la génération simultanée de piéges de surface (et/ou barrière) et de volume peut expliquer tous les modes de dégradation décrits plus haut. Les mesures expérimentales ont également montré que le stress en canal ouvert a causé une chute de la transconductance seulement pour de fortes valeurs de la tension V_{GS}, alors que le stress au pincement a provoqué une chute de transconductance uniforme pour toutes les valeurs de V_{GS}. Ce comportement peut être reproduit par la simulation physique pourvu que, dans le cas de stress a canal ouvert, on considère que les piéges s'accumulent au long d'une vaste région qui s'étend latéralement du bord de la grille vers le contact de drain, tandis que, dans le cas du stress au pincement, on considère que la génération des pièges ait lieu dans une portion plus petite de la zone d'accès à proximité de la grille et qu'elle soit accompagnée par une grande dégradation des paramètres de transport du canal. Enfin on propose que les électrons chauds et l'augmentation de la contrainte par le champ électrique soient à l'origine des dégradations observées après les stresses a canal ouvert et au pincement respectivement.
- Les piéges dans les HEMT sur GaN ont été caractérisés en utilisant les techniques de DLTS et leur comportement associé de charge/décharge est interprété à l'aide des simulations physiques. Sous certaines conditions de polarisation, les piéges du buffer peuvent produire de faux signaux de piéges de surface, c'est-à-dire, le même type de signaux I-DLTS et ICTS attribués généralement aux piéges de surface. Clarifier cet aspect est très important à la fois pour les tests de fiabilité et pour l'optimisation des dispositifs, car il peut provoquer une identification erronée du

mécanisme de dégradation, et par conséquent induire une mauvaise correction des procédés technologiques.

- Les mécanismes physiques qui provoquent l'effondrement du courant RF dans les HEMT sur GaN sont analysés par le biais de mesures expérimentales et de simulations physiques. Ce travail propose les conditions suivantes : i) les piéges du buffer aussi bien que ceux de surface peuvent contribuer à l'effondrement du courant RF à travers un mécanisme identique qui impliquerait la capture et l'émission des électrons provenant de la grille; ii) la passivation de la surface diminue considérablement l'effondrement du courant RF par la réduction du champ électrique en surface et la diminution qui en découle de l'injection d' électrons de la grille vers les pièges ; iii) pour des densités de piéges de surface inférieures à 9×10^{12} cm^{-2} , des barrières de potentiel superficiels dans l'ordre de 1-2 eV peuvent coexister avec des piéges de surface ayant des énergies plus faibles et qui causent l'effondrement du courant RF caractérisé par des constantes de temps relativement courtes.
- Les effets de l'effondrement du courant dans les HEMT sur GaN sont étudiés en utilisant les résultats de mesures expérimentales et de simulations physiques. D'après les mesures pulsées, les dispositifs employés montrent un gate-lag considérable et un drain-lag négligeable qui peuvent être attribués à la présence de piéges de surface et de buffer respectivement. En outre, l'illumination des dispositifs avec deux longueurs d'onde spécifiques peut donner lieu à un recouvrement de l'effondrement du courant dans un cas, et à une diminution du courant inverse de grille dans l'autre cas. D'autre part, les simulations physiques suggèrent que l'effet « kink » peut être expliqué par la capture d'électrons par les piéges de la couche barrière suivie d'une émission après qu'un certain niveau de champ électrique soit atteint.

Introduction

Introduction

As will be described in the following, current collapse effects and the limited reliability of GaN HEMTs is at present the major factor still limiting the large-scale deployment of these devices in both switching and RF power applications.

Despite an increasing number of papers has been devoted to reliability aspects of GaN HEMTs, a well defined picture of the underlying physics is still lacking.

This work is aimed at investigating the different mechanisms underlying RF current collapse in passivated and unpassivated AlGaN-GaN HEMTs, giving an interpretation to the different degradation modes observed in GaN HEMTs after stress, gaining insight about the location of defect generation and the underlying physical mechanism, and providing a possible explanation of the kink effect. All this is done by means of the typical measurements and experimental techniques adopted for trap characterization in high electron mobility transistors, and two-dimensional numerical device simulations.

This work was carried out jointly between the University of Modena and Reggio Emilia and the University of Bordeaux1, within the framework of the PRIN-2005 project “High breakdown voltage FETs for high power and efficiency applications”, (funded by MIUR Italian Ministry of Education, University and Research, the University of Modena and Reggio Emilia and the “Fondazione Cassa di Risparmio di Modena”).

This thesis is organized in the following way:

In the first chapter an overview of the key topics concerning GaN-based HEMTs is presented.

Chapter 2 is about an investigation of high-electric-field degradation effects in GaN HEMTs. This work was performed in collaboration with the University of Padova (group of Meneghessso). The observed degradations after both off-state stress and open-channel stress are presented and possible scenarios that can explain these degradations are provided based on two-dimensional device simulations.

Chapter 3 describes the experimental results obtained by applying different trap characterization techniques to GaN HEMTs and the outcomes of the simulation study aimed at explaining the contradicting indications obtained for buffer trap effects. This work

was performed in collaboration with the University of Padova (group of Meneghessso) and the University of Bologna (group of Cavallini).

Chapter 4 provides the relationship between surface potential and surface-trap energy, and an analysis of the role played by both surface and buffer traps in RF current collapse, as well as the impact of surface passivation by means of measurements and two-dimensional device simulations. This work was performed in collaboration with the University of Padova (group of Meneghessso).

Chapter 5 presents a possible explanation of the so-called kink effect in GaN HEMTs. This work was performed in collaboration with Thales (group of Carisetti).

In chapter 6, the most important conclusions that can be drawn from the works described in this thesis are reviewed and some future works are mentioned.

Chapter I:

GaN based High Electron Mobility Transistors

1.1 Introduction

The need for high power, high frequency transistors is increasing steadily, commensurately with the huge demand for wireless telecommunications. More power, more frequency bands, better linearity and improved efficiency are driving the current development of RF semiconductor devices capable of handling all these specifications at a reasonable price.

Over the past years, semiconductor device researchers have proposed many competing devices and technologies in order to satisfy the growing demands for high power, high frequency, high temperature, high linearity and high efficiency communication systems in commercial as well as in military applications.

Si transistors, GaAs high electron mobility transistors (HEMTs) and heterostructure bipolar transistors (HBTs), SiGe HBTs and SiC metal semiconductor field effect transistors (MESFETs) have established a well-reputed position in these areas.

However, in recent years AlGaN/GaN high electron mobility transistor (HEMT) technology has attracted a lot of interest for these applications. It has emerged as a very promising, long-term contender to other viable technologies for high power solid-state amplifiers. Many active research groups are intensively working and reporting worldwide on AlGaN/GaN high electron mobility transistors.

Silicon LDMOS was covering about 90% of high-power RF amplification applications in the 2GHz+ frequency range; the remaining 10% market share was addressed by GaAs pHEMT technology. However, this equilibrium is on the way to being turned around by the introduction of wide-bandgap (WBG) materials and related RF devices such as silicon carbide (SiC) MESFETs and gallium nitride (GaN) HEMTs [1].

GaN devices offer an impressive list of added-values over the solutions currently in use:

- Higher efficiency:
  - lower operating costs,
  - improved module power density and hence size,
  - reduced cost of ownership.
- Higher bandwidth and linearity:
  - more versatile devices,
  - fewer devices to cover the entire frequency spectrum,
  - cost saving at the development stage.

- Higher bias voltage:
  - lower current level for the same power output,
  - fewer losses from the joule effect, leading to cost savings in thermal management.
- Higher junction temperature:
  - more robust devices, leading to improved expected lifetime and mean time to failure,
  - reduced cooling system demands, leading to cost savings at the system level.

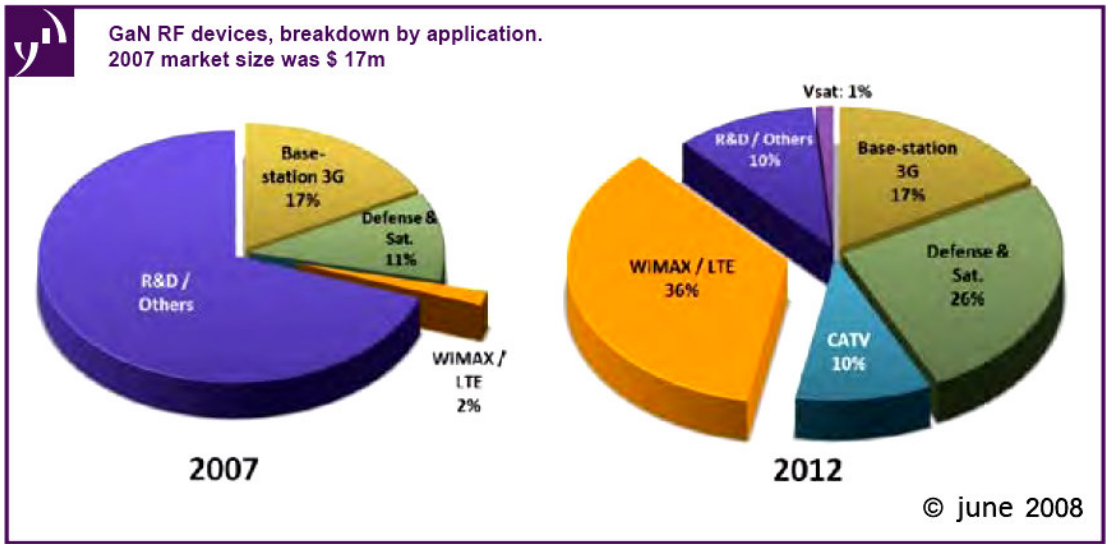

Figure 1.1: Current and expected market distribution of GaN devices [1].

These GaN devices are now challenging the dominant position of silicon in an industrial playground in which a Power Amplifier (PA) market size of ~$900M is forecasted for 2008.

Military applications were the first to use WBG devices, especially with the SiC MESFET being developed through projects broadly financed by DARPA in the US. Then in 2006, Eudyna jointly announced with NTT that a first 3G network using GaN HEMTs had been deployed in Tokyo for test purposes.

New commercial offerings from CREE, RFMD and Nitronex followed, targeting both base-station (3G, Wi-MAX...) and general purpose applications. In parallel, R&D for space applications remains very strong and the first products are expected to be implemented in the next few years. Recent announcements show that key players are more and more focusing on WiMAX/LTE markets, defocusing on the current 3G/3G+ market for which

they claim that the time-to-market for WBG devices is now over. CATV is also announced as a key market driver for GaN HEMT usage.

Remote radio head configuration will help GaN penetration in RF base stations. With standard architecture (where the amplifier is at the base of the radio tower), a large part of the signal is lost on the cable link (typically about 3dB of losses). However, in the remote radio head (RRH) configuration, RF equipment can be relocated from a cabinet to a remote location, where signals can be transmitted as close as possible to the antenna. It is therefore assumed that RRH systems will increasingly be used in future thanks to its high efficiency. Typical RRH power ranges from 20W to 50W, which match Wi-MAX and future LTE requirements perfectly. With strong penetration of WiMAX/LTE applications, it is expected that the market size for GaN RF transistors could reach a level of about $100M by 2010. The duality between WiMAX and LTE technologies should not widely impact this growth [1].

The battle will take place not only at a performance and reliability level but also at the cost level. Thus, innovative GaN-based substrate makers have a great role to play to help decrease device prices.

Nitride electronics could also become a viable solution for a field of applications where no one solid-state technology has been able to emerge, that are radar and satellite-communications links. These systems need a high power-amplification in a frequency spectrum ranging from hundreds of megahertz to tens of gigahertz, and in order to meet these requirements they still use travelling-wave tube, an ancient technology and one of the few remaining bastions of vacuum-tube electronics. The reason is that none of the available semiconductors can afford the frequencies and the power levels involved. The introduction of GaN transistors would probably bring advantage to these systems, conferring on them the advantages of the solid-state electronics, such as reliability and portability.

1.2 Basics of AlGaN/GaN HEMTs

1.2.1 Principle of HEMT operation

The HEMT is a three terminal device (see Figure 1.2), operation principle of which is similar to that of the MOSFET. In these devices, instead of having an oxide layer, a wide-bandgap material (i.e., AlGaN in case of AlGaN/GaN HEMT) separates the gate from the channel. The conductive channel is formed at the heterointerface in the form of a two dimensional electron gas (2DEG). The main advantage of having a 2DEG channel is the possibility of increasing the conductivity by increasing the carriers concentration without suffering the mobility degradation effects due to the impurity scattering. Experimentally, the existence of the 2DEG can be evaluated by measuring the temperature dependence of the carrier mobility and carrier concentration using low temperature Hall measurements. Results obtained by Hall measurements support the existence of this two dimensional electron gas by showing the temperature mobility invariability at temperatures below 100K, which is the characteristic temperature for the optical phonon scattering to be pronounced [2].

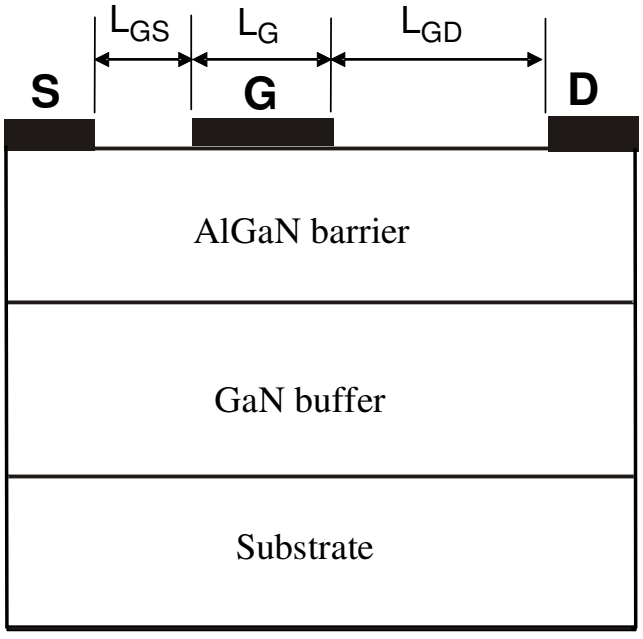

Figure 1.2: Standard structure of AlGaN-GaN HEMT devices.

The control of 2DEG carrier concentration in AlGaN/GaN HEMT is achieved by changing the Al composition of the $Al_xGa_{1-x}N$ barrier. It has been demonstrated that the increase of the Al content results in an approximately linear change in the 2DEG density (n_s) at a rate of $dn_s/dx \approx 5.45x10^{13}cm^{-2}$ [2].

A schematic draw of a HEMT based on the AlGaN/GaN heterostructure is shown in Figure 1.2. Source and drain contacts are placed directly on the AlGaN layer. Contact to the 2DEG is created through the thermal annealing as will be discussed later.

The band diagram of the HEMT device, with a triangular potential well is showed in Figure 1.3. Applying a positive voltage to the drain, current transport along the 2DEG will start, because of the potential drop between the source and the drain. The magnitude of the current is controlled by the voltage applied to gate contact V_G. Increasing V_G into the negative values forces the 2DEG to deplete under the gate region until the channel is pinched-off (see Figure 1.3).

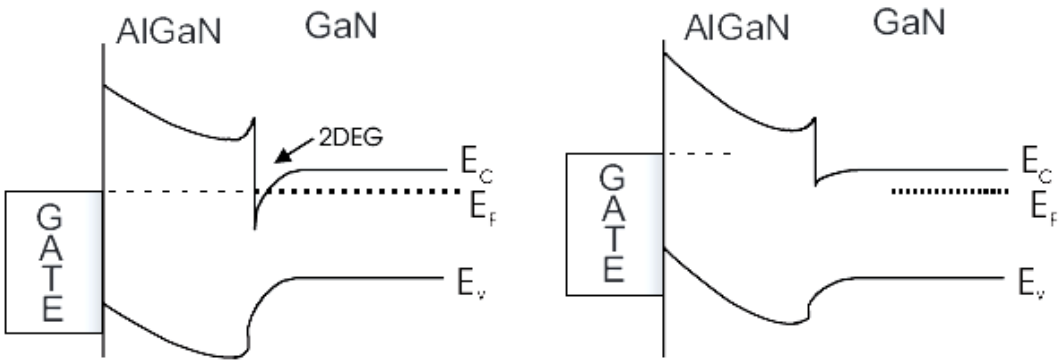

Figure 1.3: Band diagram of the AlGaN/GaN HEMT at zero gate voltage (left) and by applying a negative gate voltage (right).

1.2.2 Structure and polarization effects in III-nitrides

The group III-nitrides AlN, GaN, and InN can crystallize in the following three crystal structures: wurtzite, zinc-blende, and rock-salt. However, at ambient conditions the wurtzite structure is the thermodynamically stable phase consisting of two interpenetrating

hexagonal close packed lattices, which are shifted with respect to each other ideally by $3/8 \cdot c_0$ [3], where c_0 is the height of the hexagonal lattice cell. The chemical bonds of III-nitride compounds such as GaN are predominantly covalent, which means that each atom is tetrahedrally bonded to four atoms of the other type.

Because of the large difference in electronegativity of Ga and N atoms, there is however a significant ionic contribution to the bond which determines the stability of the respective structural phase. The unit cell of the wurtzite lattice is hexagonal with a basis of four atoms, two of each kind. There is no inversion symmetry in this lattice along the [0001] direction or c-axis, which by convention is the direction shown by a vector pointing from a Ga atom to the nearest neighbor N atom.

The lack of inversion symmetry means that, when defining an atom position on a close-packed plane with coordinates (x,y,z), it is not invariant to the position (-x,-y,-z) since inversion results in replacement of group III atoms by nitrogen atoms and vice versa. As a result of the lack of inversion symmetry all atoms on the same plane at each side of a bond are the same. Hence, wurtzite GaN crystals have two distinct faces, commonly known as Ga-face and N-face.

Figure 1.4 shows the atomic arrangement in Ga-face and N-face GaN crystals. Figure 1.4 also shows the parameters that define the wurtzite lattice. These are the edge length of the basal hexagon (a_0), and the height of the hexagonal lattice cell (c_0). The subscript "0" indicates that these values are those of the equilibrium lattice. In an ideal wurtzite crystal the c_0/a_0 ratio equals 1.633 and [4].

Because of the different metal cations, the bond lengths and the resultant c_0/a_0 ratios of AlN, GaN, and InN are different. Table 1.1 shows an overview of these lattice parameters of wurtzite III-nitrides at 300 K [3].

From Table 1.1 it is clear that GaN is closest to the ideal wurtzite structure, followed by InN and AlN. This fact is very important because the degree of non-ideality is a significant factor in determining the strength of polarization in III-nitrides.

Parameter	Ideal	AlN	GaN	InN
a_0 (Å)	-	3.112	3.189	3.54
a_0 (Å)	-	4.982	5.185	5.705
$c_0\backslash a_0$ (experimental)	-	1.601	1.6259	1.6116
$c_0\backslash a_0$ (calculated)	1.633	1.619	1.6336	1.6270

Table 1.1: Lattice parameters of wurtzite III-nitrides at 300 K [16].

The involvement of nitrogen, which is the smallest and the most electronegative Group V element, makes the III-nitrides special among the other III-V compounds as this has a strong effect on their properties. Because of the $1s^2 2s^2 2p^3$ electronic configuration of the N atom, or rather the lack of electrons occupying the outer orbitals, the electrons involved in the metal nitrogen covalent bond will be strongly attracted by the Coulomb potential of the N atomic nucleus. This means that this covalent bond will have stronger ionicity compared to other III-V covalent bonds. This ionicity, which is a microscopic polarization, will result in a macroscopic polarization if the crystal lacks inversion symmetry.

As mentioned before, the wurtzite III-nitrides do not have inversion symmetry along the [0001] direction. This fact in combination with the strong ionicity of the metal-nitrogen bond results in a strong macroscopic polarization along the [0001] direction.

Although this effect also exists in the [111] direction of zinc-blende crystals such as GaAs and InP, it is much less pronounced because of the smaller ionicity of the covalent bond. Since this polarization effect occurs in the equilibrium lattice of III-nitrides at zero strain, it is called spontaneous polarization [3].

In addition to the ionicity of the covalent bond, the degree of non-ideality of the crystal lattice also affects the strength of spontaneous polarization. In III-nitrides, although the covalent bond parallel to the c-axis is strongly ionic and is primarily responsible for the spontaneous polarization, the other three covalent bonds in the tetrahedral structure are also equally ionic. The resultant polarization from these other three bonds is actually aligned in the opposite direction and serves to counteract the polarization of the other bond. As the c_0/a_0 ratio decreases, c_0 decreases and a_0 increases, these three covalent bonds will be at a wider angle from the c-axis and their resultant compensation polarization will decrease.

As a result the macroscopic spontaneous polarization will increase. Table 1.2 shows the c_0/a_0 ratio and the spontaneous polarization for AlN, GaN, and InN. It can be seen that as the lattice non-ideality increases, c_0/a_0 ratio moves away from 1.633 of the ideal lattice, the value of spontaneous polarization (P_{SP}) increases from GaN to InN to AlN [3]. In the other hand, as can be seen in Figure 1.4, the directions of spontaneous polarization in the N-face GaN Wurtzite structure and Ga-face GaN Wurtzite structure are opposite.

Parameter	Ideal	AlN	GaN	InN
c_0/a_0	1.633	1.6010	1.6259	1.6116
P_{SP} (C/m^2)	-	-0.081	-0.029	-0.032

Table 1.2: Influence of lattice non-ideality on the value of spontaneous polarization in III-nitrides [3]

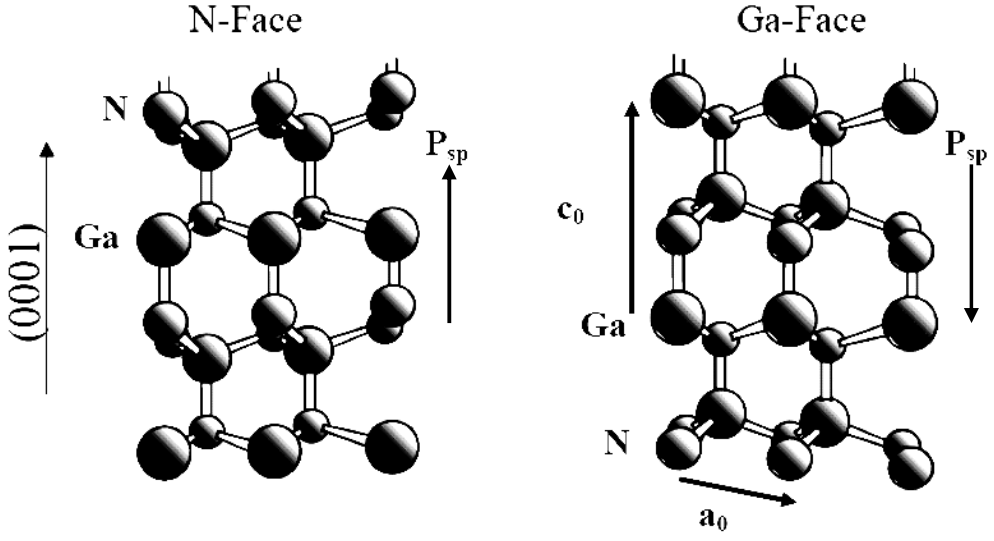

Figure 1.4: The directions of spontaneous polarization in the N-face GaN Wurtzite structure and Ga-face GaN Wurtzite structure.

If the ideality of the III-nitride lattices is changed externally, then due to the strong ionicity of the metal-nitrogen covalent bond there will be large changes in the polarization of the crystal.

One way to change the ideality of the crystal lattice is through strain. If stress is applied to the III-nitride lattice, the ideal lattice parameters c_0 and a_0 of the crystal structure will change to accommodate the stress. Hence, the polarization strength will be changed. This additional polarization in strained III-nitride crystals is called piezoelectric polarization [3]. For example, if the nitride crystal is under biaxial compressive stress, the in-plane lattice constant a_0 will decrease and the vertical lattice constant c_0 will increase. Hence, the c_0/a_0 ratio will increase towards 1.633 of the ideal lattice and the total polarization strength of the crystal will decrease because the piezoelectric and spontaneous polarizations will act in the opposite directions. It is clear that if tensile stress is applied to the crystal, the total polarization will increase because the piezoelectric and spontaneous polarizations in that case act in the same direction [5].

The value of piezoelectric polarization in III-nitrides is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). As spontaneous polarization in III-nitrides is always negative, it can be concluded that for layers under tensile stress, spontaneous and piezoelectric polarizations are parallel to each other, and for layers under compressive stress the two polarizations are anti-parallel.

Figure 1.5 shows the directions of the spontaneous and piezoelectric polarization vectors for an undoped Ga-face $Al_xGa_{1-x}N/GaN$, hereafter indicated as AlGaN/GaN, heterostructure where the AlGaN layer is under tensile stress. Meanwhile, the piezoelectric polarization will not be occurred in the thick GaN buffer layer because the lattice mismatch effect between GaN and substrate has been released by the defects or dislocations in the bottom of GaN buffer layer. Therefore the strain-induced piezoelectric polarization in thick GaN buffer can be ignored [6].

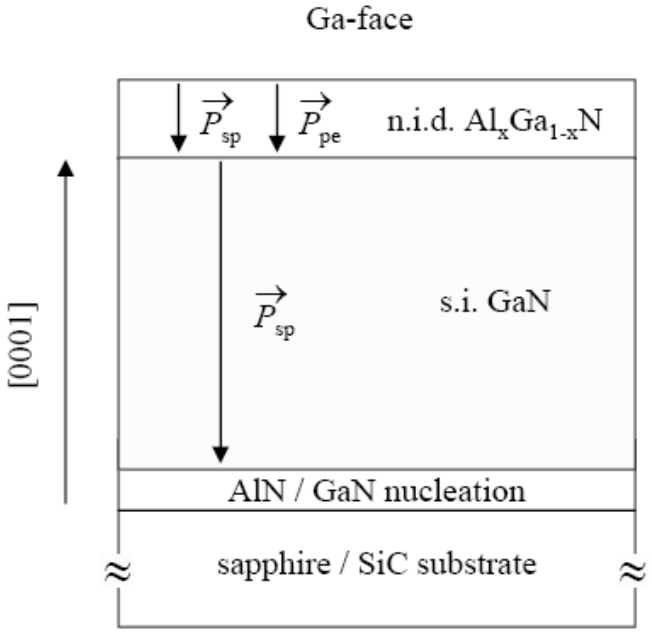

Figure 1.4: Directions of the spontaneous and piezoelectric polarization vectors for an undoped Ga-face AlGaN/GaN heterostructure where the AlGaN layer is under tensile stress.

1.2.3 Common substrates used in AlGaN/GaN HEMTs

Sapphire is the most frequently used substrate for the growth of GaN. Like Si, it can be grown using the Czochralski method. Sapphire is electrically isolating but has a poor thermal conductivity, which limits the power handling capability of devices. Furthermore, it has a large lattice mismatch with GaN resulting in high dislocation densities (10^{10}/cm^2) in the epitaxial film.

Usually, GaN is grown on the c-plane of sapphire. This results in c-plane oriented films but with the [0001] plane of GaN rotated by 30° with respect to the sapphire. This rotation reduces the lattice mismatch from 30% to 13.9%. Due to this rotation, the cleavage planes of both materials are not aligned. Obtaining smooth cleaved surfaces, e.g. needed for laser fabrication, is therefore very difficult. Due to the large lattice mismatch at growth temperature, GaN films can not be grown strained to lattice match the sapphire. One would expect the film to deposit fully relaxed.

Because the thermal expansion coefficients of sapphire are larger than those of GaN, compressive strain is induced upon cooling down. Usually, a compressive strain of 0.7GPa remains at room temperature for films of 1-3μm thick [7]. Both doping and nucleation layer thickness are known to influence the stress.

Films deposited by MOVPE on c-plane sapphire are normally Ga-face regardless of the nucleation layer. With MBE the polarity can be chosen. An AlN nucleation layer will give Ga-face polarity whereas a GaN layer will result in N-face polarity. However, without a proper nucleation layer and/or substrate treatment, epitaxial films of mixed polarity may be deposited.

As far as SiC substrate is concerned, there are over 250 different polytypes. These polytypes reflect one-dimensional variations of the stacking sequence of closely-packed biatomic planes. For epitaxial growth of GaN, the 4H and 6H polytypes are commonly used. ”H” stands for hexagonal crystal symmetry and the numbers refer to the number of layers of Si and C atoms before the atomic arrangement repeats. SiC is mostly grown using sublimation techniques like the modified Lely process [8].

SiC is a polar material and it is available in both polarities. Generally speaking, Si-terminated SiC results in Ga-face polarity of the GaN film and C-terminated SiC gives N-face polarity [9].

Although the lattice mismatch is only 3%, it is still large enough to cause high dislocation densities on the order of $10^9 - 10^{10}/cm^2$, similar to GaN films grown on sapphire. Reasons for this are the roughness of the SiC substrates (1nm root mean square (RMS) compared to 0.1nm for sapphire) and the damage introduced during the polishing process, e.g. etching remnants and scratches. Different pre-treatments like wet/dry etching or annealing can be used to alleviate these effects. Furthermore, GaN and AlN nucleation layers are used to improve the quality of the epitaxial film.

Because the thermal expansion coefficients of SiC are smaller than those of GaN, most epitaxial films will be under tensile strain. However, the amount of strain and sometimes even its sign, can strongly be influenced by adjusting the nucleation layer.

One advantage of SiC is its high thermal conductivity. This makes SiC an excellent choice for high-power applications. It does however come with a high price. Semi-insulating, n- and p-type substrates are available.

The reasons for trying Si as a substrate are obvious. Si substrates are cheap, have a high degree in crystal perfection and are available in very large sizes. It also introduces the possibility of combining GaN and Si devices on the same wafer. However, the lattice and thermal mismatch is very large.

Decent performance can be obtained with devices on Si(1 1 1) [10] but more work is needed to approach the results obtained on sapphire or SiC. If the growth problems can be overcome, Si is a very attractive candidate.

Due to its moderate thermal conductivity of 1.5W/cmK, devices on Si will not likely achieve the same power densities as devices on SiC. Furthermore, obtaining low background doping in Si substrates is rather difficult. However, the low costs of using Si substrates may prevail.

From all of the substrates mentioned so far, AlN is the best match to GaN. Not only the lattice constants match at room temperature, they are also matched at the growth temperature of GaN. Epitaxial layers of GaN grown on AlN substrates have shown low defect densities on the order of $10^4 - 10^5/cm^2$, which is about four orders of magnitude smaller than layers grown on SiC [13]. In addition, the thermal conductivity of AlN approaches that of SiC making it an excellent substrate for power devices. Apart from being a prime candidate for GaN heteroepitaxy, AlN could be used for optoelectronic devices. Its band gap of 6.2eV promises the development of deep-UV light sources. AlN is usually grown by sublimation techniques using 6H-SiC as a seed material or not using a seed at all (self-seeding). Due to the high temperatures involved (2300K) and the highly reactive Al species, designing a durable reactor is complicated. Cracking induced by the difference in thermal expansion coefficients between AlN and the SiC, or the crucible in case of self-seeding, can be significant [11]. A high-pressure approach, in which AlN is grown from a solution of atomic nitrogen in liquid aluminum, is also pursued [12].

In Crystal-IS^2, an incubator of the Rensselaer Polytechnic Institute, substrates as large as $1cm^2$ with defect densities on the order of $500/cm^2$ have been demonstrated.

It needs no explanation that the availability of low cost AlN substrates could accelerate the development of the III-nitride material system. However, obtaining a low background doping may prove to be difficult due to the high reactivity of aluminum with oxygen.

1.2.4 Ohmic and Shottky Contacts

Most ohmic contacts on AlGaN/GaN heterostructures are based on Ti/Al metallization schemes. The most frequently reported are the Ti/Al/Ti/Au, Ti/Al/Ni/Au and Ti/Al/Pt/Au schemes. Each of the metals in these stacks has its own specific role.

Titanium, the first metal in all cases, is believed to: i) serve as an adhesion layer to provide good mechanical stability [13], ii) dissolve the native oxide on the AlGaN surface [14, 15], iii) create nitrogen vacancies by reacting with nitrogen atoms in the AlGaN. This process renders the surface highly doped, which enables electrons to tunnel through the thin barrier [13, 15].

Aluminum supposedly: i) reacts with Ti to form an Al_3Ti layer that prevents the underlying Ti layer from oxidizing [13, 14], ii) serves as a diffusion barrier for the metals on top of Al as they form high Schottky barriers [15].

The Ni and Pt layers should prevent the diffusion of Au to the Al layer. This Au layer is added to improve the conductivity of the metal stack. However, when Au and Al react, they could form the so-called ”purple plague”, a highly resistive layer. One of the most important reasons for adding metals on top of Al is to prevent this layer from spreading out. Usually, the ohmic contacts are annealed at very high temperatures (> 800°C), well above the melting point of Al (660°C). If no metals are put on top of Al, the line definition of the contact cannot be controlled.

In [11], the following mechanism for ohmic contact formation during the annealing process is proposed. First, reactions start between Ti and Al at relatively low temperatures (200−300°C) with the formation of an Al_3Ti phase according to the binary phase diagram. If Al and Ti were the only metals involved, this would require an Al/Ti thickness ratio of 2.82. If this ratio is smaller, there is an excess of Ti available to react with the AlGaN. This reaction probably starts at 400°C and involves:

- The dissolution of the native oxide present at the surface.
- Subsequent outdiffusion of nitrogen to form nitrogen vacancies.
- The formation of Ti-Al-N interfacial phases.

Decomposition of the AlGaN probably starts at temperatures above 850°C causing degradation of the ohmic contact and the crystal structure itself.

From the discussion it is clear that several reactions take place at different temperatures.

To get reproducible results, it is therefore important to accurately control the heat treatment both in temperature variations and in time. Rapid thermal annealing (RTA) is the technique most suited to meet these requirements.

Schottky contacts are an important building block for HEMT devices. The energy barrier height is a key parameter of the junction, controlling both the width of depletion region in the semiconductor and the electron current across the interface. Barrier height is defined as the energy difference between the semiconductor conduction-band edge at the interface and the Fermi level in the metal.

In data published by various researchers, a large variation in the barrier height for standard metals deposited onto $Al_xGa_{1-x}N$ ($0<x<0.3$) can be found. The spreading appears probably as a result of various factors, like the presence of several transport mechanisms, different defects present in the material, the effectiveness of surface cleaning prior to metal deposition, local stoichiometry variations and variations in the surface roughness. To get a large Schottky barrier height for rectifying metal contacts, which is imperative for low leakage current, metal with large work functions such as Au, Pt, Ni have been explored. Pt deposited on n-GaN exhibits nearly ideal Schottky behavior with 1eV resulting barrier height. Nickel with its large work function gives barrier heights of about 0.66-1eV [15].

Thermal stability of Schottky contacts is the next very important point for practical device operation. The thermal limits of most metals are between 300-600°C, namely 400°C for Pt, 575°C Au and 600°C for Ni [16].

In [17], it has been shown that thermal annealing at 500°C for 5min is more effective with Ni/Pt/Au than with Ni/Au and Pt/Au to obtain a high quality Schottky contact. AlGaN/GaN HEMTs were fabricated using Ni/Pt/Au gate contacts; a reduction of the gate leakage current by as much as four orders of magnitude was successfully recorded by thermal annealing without degrading the transconductance of the transistor.

To determine how a metal-semiconductor barrier is formed, we first need to know about the properties of the semiconductor itself. The GaN material system behaves quite differently compared to more conventional semiconductors like Si or GaAs due to the high polarization fields that exist in these materials. Several experimental techniques are available with which the barrier height and ideality factor can be determined from measurements:

- The current-voltage method.

- The capacitance-voltage method.
- The internal photo-emission method.

The latter technique is the most effective and accurate one.

1.3 Factors limiting the HEMT performance

Current collapse in AlGaN/GaN HEMTs has been one of the most exciting topics in recent years. This is basically an observation in which the output power achieved from a device at microwave frequency of interest is considerably smaller than the expected one based on DC characterization. The presence of surface and epitaxy related defects, traps or deep levels inthe device structure are responsible for this observation.

The charge transfer process in these levels is too slow to follow high frequency signal therefore the electrons get trapped into them [18]. This disturbs the balanced charges in the 2DEG and reduces the number of electrons available for current conduction. As a result of this the drain current reduces with an increase in knee voltage, thereby limiting the device power output. Hence this current collapse problem is a major obstacle in boosting up the overall device performance.

1.3.1 Current collapse related to buffer-traps

It is a significant reduction in the drain current observed when the drain voltage is changed abruptly and it is referred to as drain-lag .

In [19], it has been shown that the same phenomenon occurs in GaN MESFETs. In addition to illumination, performing the measurements at elevated temperatures also decreased the current collapse. The origin of this effect was thought to be hot-electron trapping in the GaN buffer layer.

In [20], a spectroscopic technique was used to determine the properties of the traps responsible for current collapse in GaN MESFETs. The drain source current was measured in the dark and under illumination by monochromatic light and the response function was calculated. In [21], the same authors have shown that this response function is proportional to the photoionization cross-section of the trap if the transistor is operated in the linear regime and the measurements are carried out at low optical excitation. By also measuring

the current difference as a function of light intensity, two distinctive traps (1.8eV and 2.85eV below the conduction band) could be isolated in the GaN buffer. Similar trap levels were also found in [22].

Using the photoionization technique, it was shown that the traps causing the current collapse in AlGaN/GaN HEMTs have the same energy levels as those in GaN MESFETs [23]. This further indicates that these traps were located in the buffer layer.

Current collapse measurements on AlGaN/GaN HEMTs revealed that the effect was more pronounced in devices that had a semi-insulating buffer instead of a conductive one [18]. In addition, surface treatments, e.g. passivation with SiN_x, did not influence the current collapse. It was argued that the highly resistive nature of the buffer layer could be caused by traps that are also responsible for the current collapse.

In [24], the correlation between the growth pressure of the buffer layer, carbon incorporation and the density of the deepest trap (2.85eV) has been shown. Growing the buffer layer at relatively low pressures (< 50Torr) increased carbon incorporation. Preliminary work has shown that carbon may act as a deep acceptor and could consequently compensate donors in n-type material [25].

Secondary ion mass spectroscopy (SIMS) measurements indicated a strong correlation between the concentration of the deepest trap (2.85eV) and the carbon concentration in the buffer layer. The concentration of the lowest trap (1.8eV) increased more gradually with lower growth pressures. This was believed to be related to the higher dislocation densities that occur at lower growth pressures [24].

In AlGaAs/GaAs HEMTs, current collapse is often observed at low temperatures. This effect was attributed to electron trapping in DX-centers in the Si-doped AlGaAs layer [26]. In AlGaN/GaN HEMTs, oxygen is known to cause DX-center-like defects in the AlGaN layer [27].

Using deep-level transient spectroscopy (DLTS), traps in AlGaN/GaN structures with an activation energy of 0.28eV were extracted [28]. However, the authors concluded that this value is too small to explain the current collapse phenomenon.

1.3.2 Current collapse related to surface-traps

A number of terms in literature are used to describe this phenomenon like DC-to-RF dispersion, current slump, current compression, current collapse and gate lag. Some of these terms are also used to describe charge trapping in the buffer layer, which makes it sometimes difficult to discriminate between the two.

In [29], a correlation between the measured RF output power and the drain-source current response during a gate lag measurement was demonstrated. In a gate lag measurement, the drain-source voltage is kept at a constant value, while a pulse is applied to the gate. Usually, this pulse is set to drive the transistor from below pinch off to the on-state (e.g. V_{GS} = 0V). By changing the value of V_{DS} and the maximum voltage of the gate-source pulse, one can reconstruct the I-V characteristics. As demonstrated by the authors, this type of measurement can provide a good indication of the power capabilities of a device.

In [30], a large-signal current swing measurement was used to show drain source current compression in AlGaN/GaN HEMTs. This measurement is much like a gate lag measurement, but in this case a sinusoidal voltage is applied to the gate instead of a pulse. The maximum drain-source current swing showed a transition frequency in the kHz range. In addition to the current swing, the transconductance and gate capacitance (capacitance with drain and source shorted) showed similar behavior. A reduction as much as 50 percent could be seen at high frequencies. The same measurement technique was used in [31] to show that this transition frequency can differ by many orders of magnitude for different devices ranging from 10^{-4} to 10^{10} Hz.

Slow drain-source current transient responses were observed in [32] after the device had been stressed for several minutes by applying different gate-source voltages with zero drain-source bias. After applying the stress, the device was biased at V_{GS} = 0V and V_{DS} = 0.1V and the drain-source current response was measured. A very slow transient response was measured on the order of minutes. The magnitude of current reduction increased with the magnitude and time of the applied gate-source bias stress prior to the measurement.

In [33], it has been shown that by passivating HEMTs with a 350nm SiN_x layer, the microwave output power of these devices could be increased by as much as 100 percent. The transconductance, maximum drain-source current, and breakdown voltage increased 10, 20, and 25 percent, respectively, while the pinch off voltage showed only a marginal

shift of -0.25V. The SiN_x layer caused an increase in the gate-drain capacitance, which in turn led to lower values for the small-signal gain, f_T and f_{max}. Similar findings were reported in other publications [34, 35].

Using gate lag measurements, it has been shown that the maximum current of an unpassivated device can be as low as 10 percent of the value that is obtained after passivation [18].

In [36], a large-signal current measurement in which the transistor was driven into saturation and pinch off was performed. The drain-source current waveform showed a decreasing amplitude with time. This decay was attributed to the formation of a virtual gate caused by electron trapping in surface states in the region between gate and drain.

These electrons could be injected from the gate metal, a process which is facilitated by the large electric field at the drain-side edge of the gate. Trapped electrons deplete the channel limiting the full current swing that can be obtained. Applying a higher drain source bias led to a faster formation of the virtual gate and a smaller current swing, while UV illumination cancelled the formation of the virtual gate. The steady-state electron population of the virtual gate is determined by the time constants of the trapping and de-trapping processes, the lateral transport of electrons to the traps, and the frequency of the applied signal. If the applied frequency is well above these constants, large-signal measurements will show a limited current swing, while small-signal measurements may not reveal anything. The latter is the reason why good f_t and f_{max} values have been reported for devices suffering from this effect.

In [37], a scanning Kelvin probe microscopy (SKPM) [38] was used to investigate the surface potential during bias stress measurements. Changes in the bare surface barrier height (equal to changes in the surface potential with a negative sign), can be monitored both in time and space using this technique. If the surface is involved in causing the decrease in 2DEG, the charge dipole across the AlGaN barrier layer will be affected since that is directly related to the 2DEG density at the AlGaN/GaN interface. A change in the charge dipole across the AlGaN barrier, however, will change the position of the conduction band at the surface with respect to the reference Fermi level in the bulk. Drain-source current transients were recorded at V_{DS} = 1V and V_{GS} = 0V. Prior to the measurement, the device was stressed (V_{DS} = 20V and V_{GS} below pinch off) for 2min. The drain-source current showed a slow recovery to the pre-stress values. Simultaneous SKPM

measurements showed a direct correlation between the drain-source current transient and the transient observed in the surface potential. Furthermore, the changes in surface potential were mostly located in the gate-drain area. This further substantiates the possibility that electrons occupy surface states in the gate-drain region thereby forming a virtual gate. It was argued that since there was no current flowing during the bias stress, electrons from the gate are injected into the surface states. This process is facilitated by the high electric fields that exist under pinch off conditions. Measurements indicated that indeed most of the voltage difference drops within 0.2μm from the gate [37]. Performing the measurements under UV illumination did not show the formation of a virtual gate. Measurements done at elevated temperatures or measurements done on devices passivated with SiN_x, showed a significant reduction in the magnitude of the transient. The authors argue that the same effect is responsible for the reduced RF power output often encountered in AlGaN/GaN HEMTs.

Although many groups have reported significant improvements in device performance after passivating with SiN_x, there is no general framework yet by which this effect can be explained.

In [39], DLTS measurements were carried out on unpassivated AlGaN/GaN HEMTs to show the presence of two traps. After passivation, the DLTS signal belonging to the most dominant trap was reduced significantly. This implicates that the effect of SiN_x is to reduce the surface state density or at least the density of the trap causing the DLTS signal.

Other authors argued that the nature of the interface states changes or that Si incorporates as a shallow donor [36]. The positive counter charge of the channel electrons may even have moved into the passivation layer, where it becomes fixed [40].

However, this same passivation layer could introduce trap levels that has been identified in causing power slump in AlGaAs/GaAs power HEMTs [41]. The passivation layer could also prevent the attachment of ionic adsorbates to the surface [36]. The charge of these adsorbates could also lead to the formation of a virtual gate.

Not only SiN_x has proven to be a suitable candidate for passivation. Other materials like scandium oxide (Sc_2O_3) and magnesium oxide (MgO) have also shown promising results [42]. SiN_x has the disadvantage that it contains atomic hydrogen, which could diffuse into the AlGaN layer or gate metal over extended periods of device operation. These other materials do not have this problem [43].

Chapter II:

Investigation of High-Electric-Field Degradation Effects in GaN HEMTs

2.1 Introduction

The poor reliability under high-electric-field operation is probably the major factor still hampering large-scale penetration of GaN HEMTs into the RF power markets where these devices offer unquestioned performance advantages over all other competing technologies. For this reason, GaN-HEMT reliability has started being addressed by an increasing number of works [44-58]. The reliability implications of several aspects related to either epitaxial structure or processing have been addressed, including surface passivation [44-47], barrier thickness [49,50], Al mole fraction in the AlGaN barrier [53], pre-passivation plasma treatments [51], insulated gate [54], field-plate gate [49,50,54]. Mechanisms invoked to explain degradation effects include: negative-charge accumulation into surface traps due to electron tunneling from the gate under off-state and pulsed short-term stresses [44]; hot-electron trapping in the AlGaN barrier and trap generation at the AlGaN-GaN interface after 1-h open-channel stress [45]; trapping of gate-injected electrons in the AlGaN layer plus hot-hole trapping and trap generation in the AlGaN layer and at the AlGaN-GaN interface after 1-h high-reverse-current stress [45]; hot-electron trapping at surface and barrier traps under RF stress [53,55]; thermal-induced modification of the Schottky contact after open-channel DC stress [63]; trap generation induced by hot electrons after 10-340 h open-channel DC stresses [51]; trap generation within the drain-access region after 150-h [52,57] and 3000-h [56] on- and off-state DC stresses; generation of defects and traps within the barrier drain access region as a consequence of electric-field-induced strain enhancement and subsequent relaxation [58].

In spite of these research efforts and recent progresses, a well defined picture of the physical mechanisms limiting the high-electric-field reliability of GaN HEMTs is still to be achieved, so that trying to gain insight about the possible degradation effects and related mechanisms is still a worthwhile effort. In view of this, useful information can be inferred from numerical device simulations, allowing the impact of different degradation mechanisms to be evaluated quantitatively and the suitability of plausible degradation scenarios to be tested against the results of stress experiments.

In this chapter, a detailed experimental study of the degradation modes induced by DC high-electric-field stress on GaN-capped AlGaN-GaN HEMTs is reported. Stress experiments were conducted (i) in power-state conditions, i.e. at open channel (V_{GS}=0 V)

and high drain-source voltage (V_{DS}=16 V), (ii) in off-state conditions, i.e. with the channel pinched off (V_{GS}=-6 V) and high V_{DS} (V_{DS}=32 V). Acceptor-trap generation within the gate-drain access region is invoked to explain the degradation modes common to both stress conditions, i.e. DC drain-current (I_D) drop, gate-lag amplification and reverse gate current (I_G) decrease. Moreover, relying on the different impact of the two stress types on the transconductance (g_m) vs V_{GS} curve, it was speculated that trap generation should take place in a wide portion of the gate-drain region during power-state stress resulting in large drain-access-resistance increase and gm drop under open-channel conditions at high V_{GS}, while the decrease in channel mobility should contribute to off-state-stress degradation leading to g_m peak drop.

Device simulations are adopted with the aim of validating the above hypotheses about high-electric-field degradation of the GaN-AlGaN-GaN HEMTs under study. More particularly, the goals of these simulations are: (i) to gain insight about the way trap generation in the different device layers affects the device DC and transient behavior; (ii) to investigate the impact of the lateral extension of trap generation within the drain access region and the degradation of channel transport parameters on the g_m vs V_{GS} curve; (iii) to infer indications about the physical mechanisms underlying the observed degradation modes.

2.2 Pre-stress characteristics of the devices

The devices were grown on semi-insulating SiC substrates by MOVPE without any passivation. Both intentionally undoped and doped heterostructures were obtained. Undoped structures consist (from bottom to top) of 3 μm of GaN followed by 30 nm of undoped $Al_{0.28}Ga_{0.72}N$ and by 3 nm of undoped GaN. Doped structures are identical to the undoped ones, except that the AlGaN layer is formed by 10 nm of $Al_{0.28}Ga_{0.72}N$ doped with Si at the concentration of $5\cdot10^{18}$ cm^{-3}, sandwiched between two $Al_{0.28}Ga_{0.72}N$ undoped spacers (the bottom one is 10-nm thick while the top one is 5-nm thick). The ohmic contacts were obtained by deposition of a Ti/Al/Ni/Au (35/200/40/100 nm) multilayer, followed by rapid-thermal annealing at 850°C for 30 s in an N_2 ambient ($5\cdot10^{-3}$ mbar overpressure). A uniform contact resistance of 0.3 Ω·mm was measured from TLM patterns. The Ni/Au Schottky contact was patterned by e-beam lithography. Room-

temperature, Hall-effect measurements yielded a sheet carrier density of $7 \cdot 10^{12}$ cm^{-2} and $9.7 \cdot 10^{12}$ cm^{-2} and an electron mobility of 1930 $cm^2/V \cdot s$ and 1660 $cm^2/V \cdot s$ for undoped and doped structures, respectively. Devices considered here have a gate length L_G=0.3 µm, a gate width W_G=100 µm and a drain-source spacing L_{DS}=3 µm. DC and pulsed characterizations prior to stress were carried out on 10 undoped samples and 10 doped samples.

Figure 2.1 shows typical DC drain-current (I_D) and gate-current (I_G) vs drain-source-voltage (V_{DS}) characteristics measured at a gate-source voltage (V_{GS}) of 0 V from doped and undoped HEMTs having L_G=0.3 µm. A larger I_D is observed in the doped devices, owing to the higher two-dimensional electron gas (2DEG) concentration. Doped devices have also a larger gate-leakage current, which can be attributed to the higher gate-drain electric field resulting in enhanced gate electron injection.

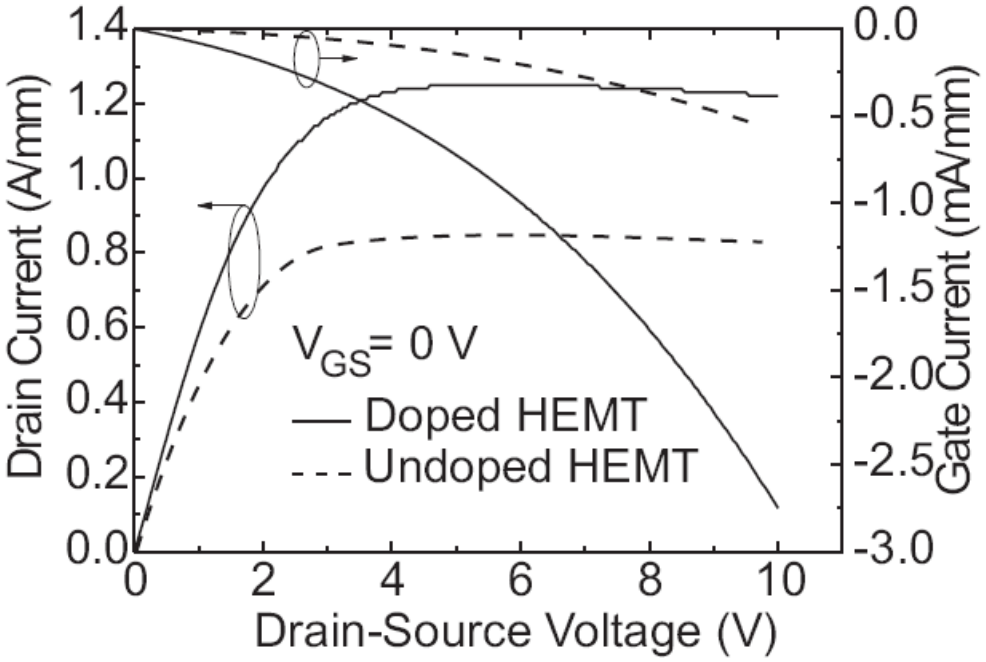

Figure 2.1: Static drain I_D and gate I_G currents as a function of drain–source voltage V_{DS} at the gate–source voltage V_{GS} of 0 V for a doped and an undoped sample.

A complete set of static measurements from undoped HEMTs yielded a saturation drain current (I_{DSS}) of 0.8±0.05 A/mm at V_{GS} =0 V, a peak extrinsic transconductance (g_m) of 220±15 mS/mm at V_{DS} =6 V, and a threshold voltage (V_{TH}) of -4±0.2 V. Doped devices

exhibited, in agreement with Hall measurements, higher values for I_{DSS} and g_m peak (namely, I_{DSS}= 1.2±0.09 A/mm and g_m=270±20 mS/mm) as well as a more negative V_{TH} (namely, V_{TH}=-5.8±0.3 V). As shown in Figure 2.1, both types of devices are characterized by relatively-high gate-leakage currents (in the order of mA/mm).

To assess the impact of dispersion effects in these devices, gate-lag measurements were carried out. In particular, the device was pulsed in the following way: a fixed drain voltage V_{DD} was applied to the drain through a 50-Ω resistor, while the gate voltage was pulsed from off-state to different open-channel values. The measurement setup consisted of an Agilent HP8110A pulse generator for gate pulsing and a Tektronix TDS680 oscilloscope (1GHz band, 5 GS/sec) for drain-voltage recording.

Figure 2.2 shows pulsed output I-V characteristics for a doped and an undoped HEMT, compared with the corresponding DC curves. Pulsed characteristics were obtained from the gate-lag measurements (described above) by averaging the last ten I_D samples from sixteen distinct 50 ns pulses.

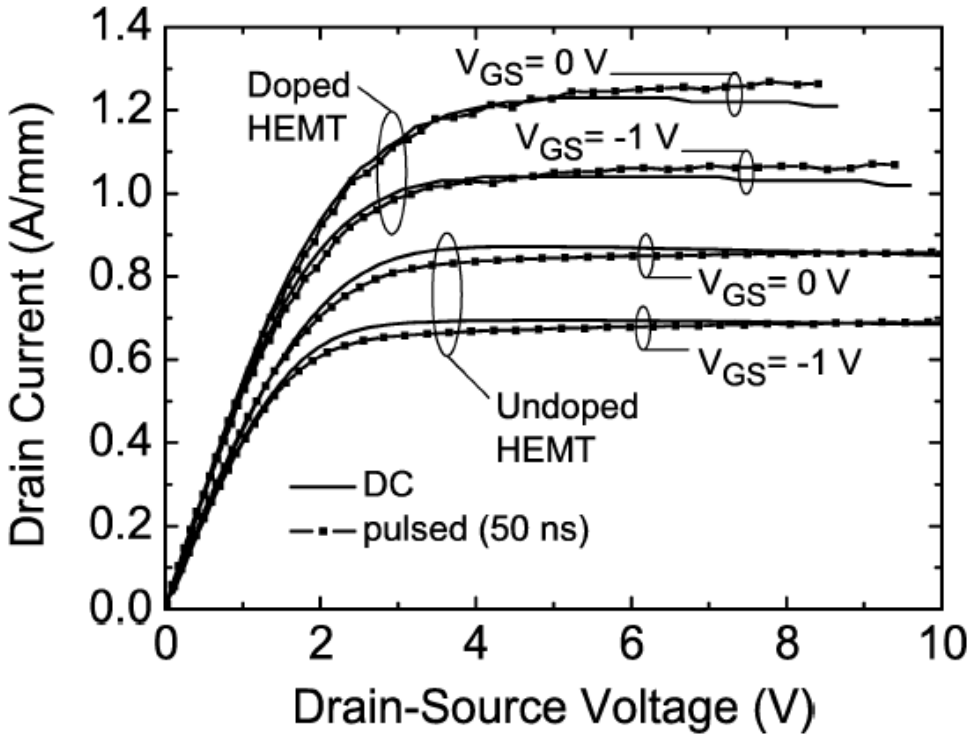

Figure 2.2: DC and pulsed output characteristics at two gate–source voltages V_{GS} for a doped and an undoped sample. For pulsed measurements, V_{GS} is pulsed from −6 V to the final V_{GS} value, and the pulsewidth is 50 ns.

As can be noted in Figure 2.2, very small differences exist between pulsed and DC curves both for the doped and the undoped device. The amount of current collapse can be quantified in terms of the ratio of the drain current measured at the end of the pulse width (I_{Dpulse}) over the corresponding static drain current (I_{DC}). The dependence of the I_{Dpulse}/I_{DC} ratio upon the applied pulse width is reported in Figure 2.3. Data symbols correspond to average values obtained from 10 samples (for each device type), with errors bars indicating the maximum device-to-device variation observed. Clearly, the undoped devices show a minimum I_{Dpulse}/I_{DC} ratio of ~ 95% (corresponding to a current collapse of ~ 5%) down to a pulse width of 50 ns. Doped samples do not show any current collapse at all. The nearly-ideal behavior exhibited by these devices under pulsed operation is actually confirmed by load-pull RF power measurements, yielding an output-power density of 4.82 W/mm at 2 GHz from a doped HEMT biased at V_{DS}=21 V [59].

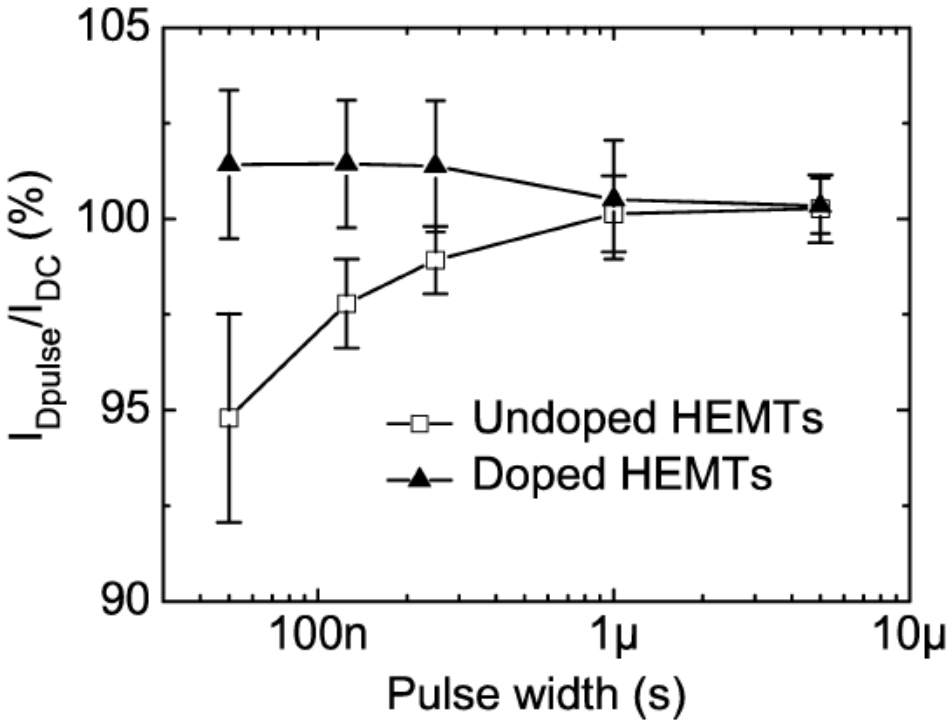

Figure 2.3: Ratio between the drain–current measured at the end of the pulse width I_{Dpulse} and the corresponding static drain–current I_{DC} as a function of pulse width for doped and undoped samples (V_{GS} pulsed from −6 to 0 V, V_{DD} = 12 V). Symbols are average values, whereas error bars represent data intervals for ten measured devices.

Other authors have proposed that the introduction in the epitaxial structure of a thin, n-doped GaN cap layer can effectively reduce the impact of dispersion effects by compensating the negative polarization charge at the GaN-AlGaN interface and/or by screening the channel 2DEG from surface states [60,61]. In the devices considered here, the GaN cap layer is undoped. As a matter of fact, the same beneficial effect of n-type doping can be accomplished by donor-like traps present in the unintentionally-doped GaN cap layer. The substantial immunity from dispersion effects characterizing the GaN/AlGaN/GaN HEMTs under study comes indeed at the price of a relatively-high gate-leakage current, see Figure 2.1.

2.3 High-electric-field stress tests

A high-electric-field stress campaign was carried out on the devices under study, in order to evaluate their long-term stability. When the HEMT works in open-channel conditions, both thermally-induced and hot-electron-related degradation can occur. Under off-state conditions, instead, the electric field between gate and drain is large but the low current level prevents self-heating. In order to separate these two possible sources of degradation, both open-channel and off-state stresses were applied. For open-channel stress, V_{DS} and V_{GS} were set to 16 V and 0 V, respectively, while for off-state stress, V_{DS} was set to 32 V and V_{GS} to -6 V. During the stress, DC and gate-lag measurements were taken at logarithmic time intervals. For gate-lag measurements, V_{GS} was pulsed from -6 V to 0 V with V_{DS} kept at 12 V, using the same setup adopted for unstressed devices. Stress experiments were carried out on 10 samples (5 for open-channel and 5 for off-state stress tests). All of the tested devices exhibited the degradation effects described in the following. Results shown in the following refer, in particular, to doped samples, as these have better starting characteristics, both in term of maximum I_D and current-collapse immunity. The same qualitative effects were however observed also in undoped HEMTs.

2.3.1 Open-channel stress degradations

Figure 2.4 shows typical DC output characteristics measured before and after 150 hours of open-channel hot-electron-stress. As can be noted, the I_D drop induced by the stress is

maximum at high V_{GS} (i.e. under open-channel conditions) and low V_{DS} (i.e. in the linear region of the I-V curves). This kind of behavior is generally attributed to the increase in the drain access resistance (R_D), resulting from electron trapping in the gate-drain channel access region, at the device surface and/or in the layers underneath the channel [62]. The impact of the R_D increase is actually higher at higher V_{GS}, as a consequence of the reduced channel resistance and the increased voltage drop across the access region. In the saturation region, then, the high longitudinal electric field almost completely masks the effect of the increased access resistance; this explains the reduced I_D degradation observed at high V_{DS}.

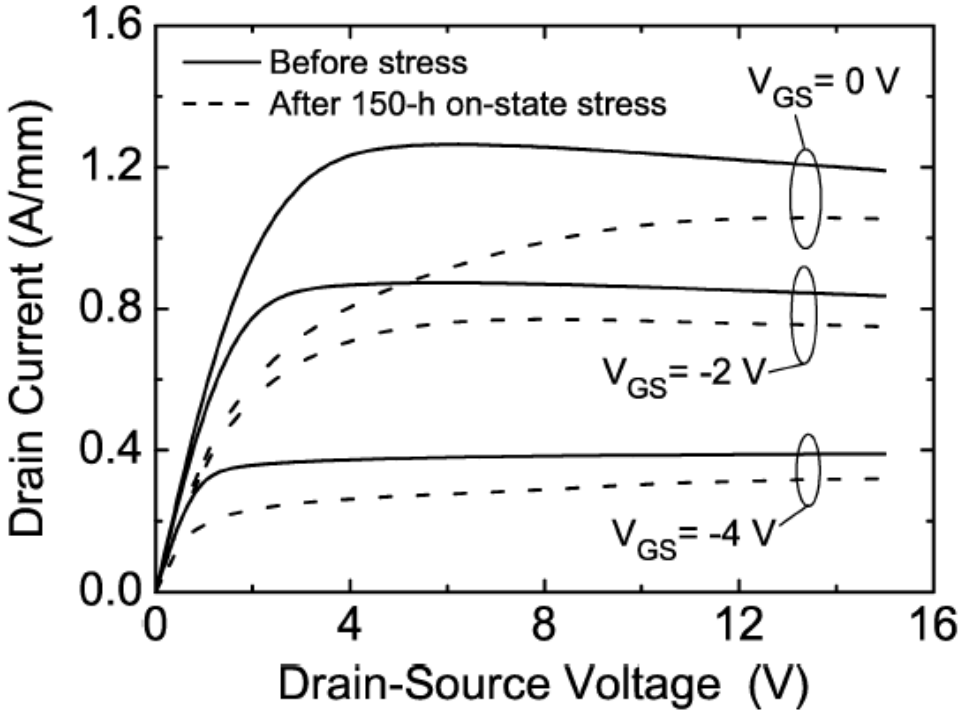

Figure 2.4: Static drain–current I_D versus V_{DS} curves measured before (solid) and after (dashed) 150 h of Open-channel stress. The sample is a doped HEMT.

Figure 2.5 illustrates the impact of 150 hours of open-channel stress on the low-frequency transconductance (g_m) vs V_{GS} curves. Three degradation modes appear after the stress: i) a positive shift of the threshold voltage (V_{TH}), ii) a small decrease in the g_m peak, and iii) a drastic drop of gm at high V_{GS}. The latter effect can be correlated with the reduction of I_D at high V_{GS} seen in Figure 2.4, both effects pointing at an increase in the drain access resistance as the dominating degradation mechanism. The small decrease in I_D at low V_{GS} and high V_{DS} (Figure 2.4) can now be almost entirely ascribed to the V_{TH} shift (Figure 2.5).

As will be shown later (Figure 2.9), this V_{TH} shift is not present after off-state stress. This fact suggests that it can be originated (i) by thermally-induced gate-contact degradation [76], (ii) by electron trapping under the gate electrode (that is suppressed under off-state stress because of the negative V_{GS} applied) [53], or by a combination of effects (i) and (ii).

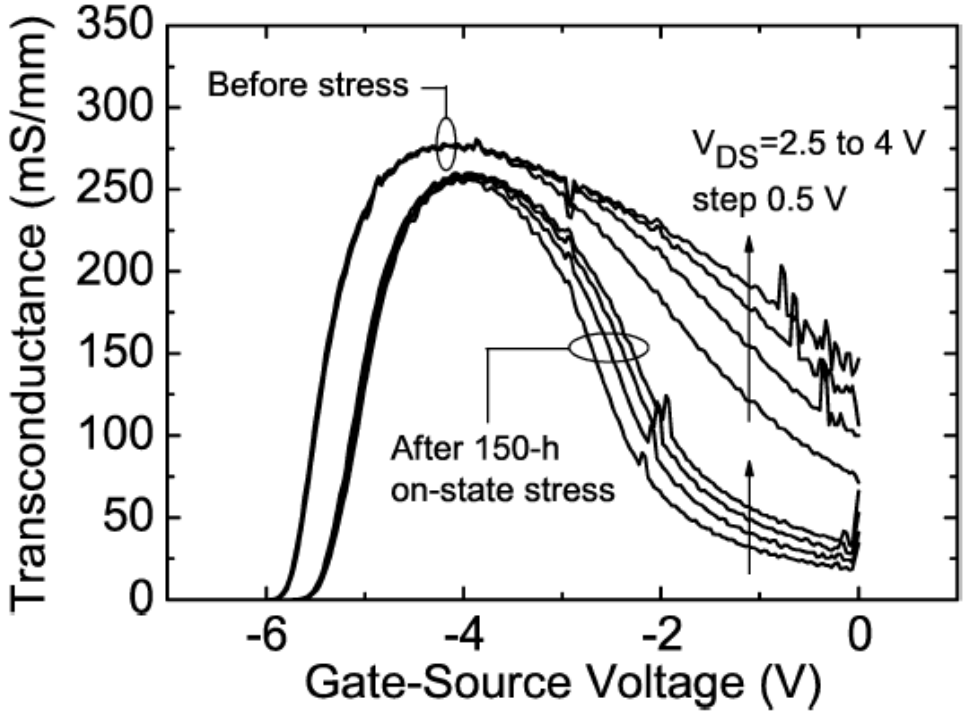

Figure 2.5: Transconductance g_m measured as a function of gate–source voltage V_{GS} before (solid) and after (dashed) 150 h of Open-channel stress. The drain–source voltage V_{DS} is varied from 2.5 to 4 V with a step of 0.5 V. The sample is a doped HEMT.

Significant gate-lag effects appear after the stress, as demonstrated by Figure 2.6 where pre- and post-stress $I_D(t)$ turn-on transients are compared. As can be noted, in the stressed device the prompt I_D response (about 0.45 A/mm from the expanded plot in Figure 2.6(b)) is appreciably compressed with respect to the static I_D value (about 0.9 A/mm, see dashed line with V_{GS}=0 V in Figure 2.4). Moreover, a slow transient with a time constant in the order of several seconds shows up after the stress. This behavior can be explained by assuming that, as a result of hot-electron stress, traps are generated at the gate-drain surface. These traps must have a significantly large activation energy and/or they must be fed by a "slow" conducting mechanism (like hopping), in order to explain the long time constants governing gate-lag transients in stressed devices.

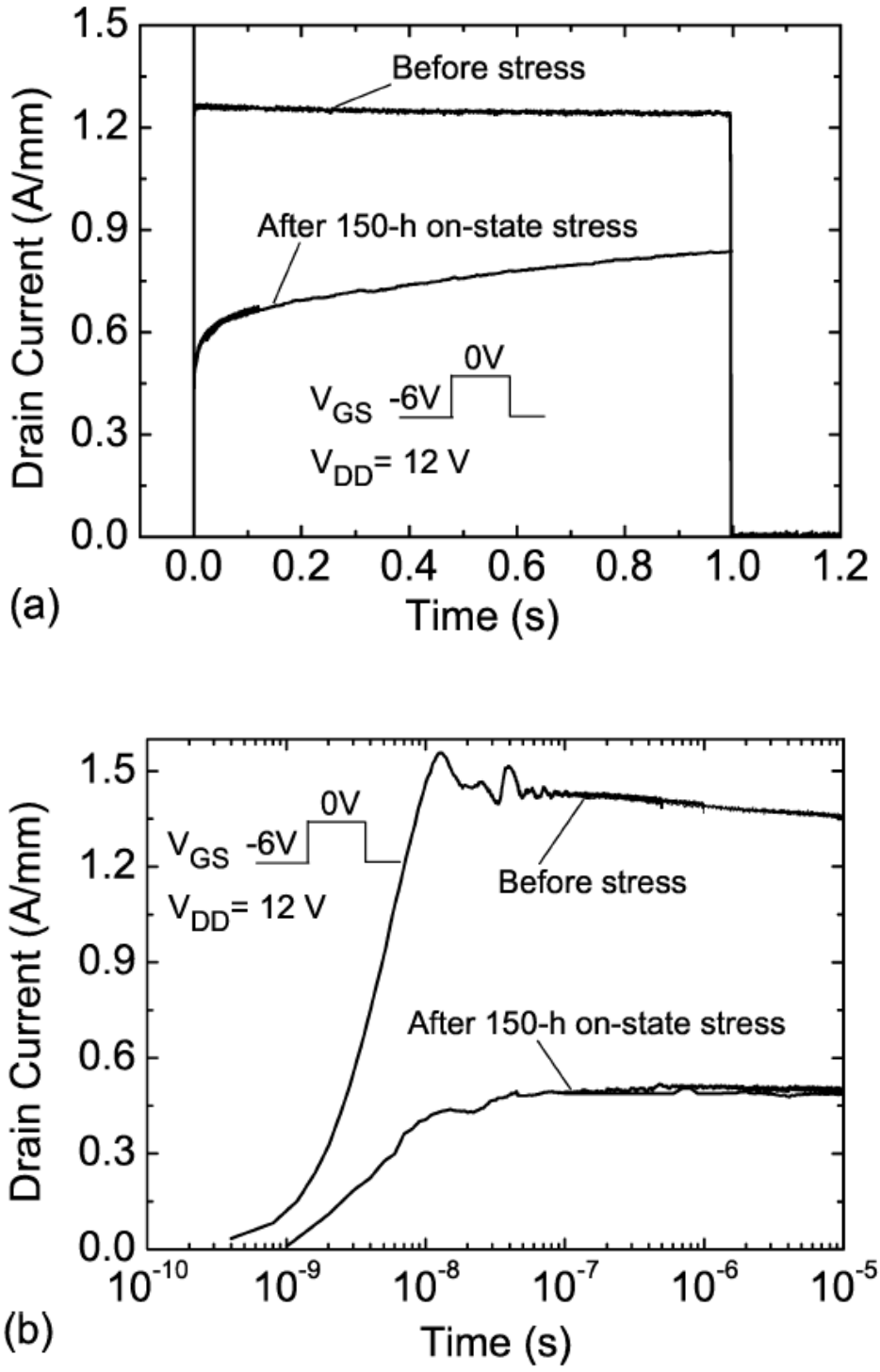

Figure 2.6: (a) Drain–current versus time waveforms following a V_{GS} step from −6 to 0 V at V_{DD} = 12 V before and after 150 h of Open-channel stress. (b) Expanded plot of the short-time region of the I_D pulse on a logarithmic time scale. The pulse rise time is 10^{-8} s. The sample is a doped HEMT.

Interestingly, a drastic decrease in I_G is observed as a result of stress. This is illustrated by Figure 2.7, showing I_G vs V_{GS} curves measured before and after the open-channel stress (150 hrs). Two phenomena can contribute to this I_G drop: (i) a decrease in the surface conductance between gate and drain and (ii) a reduction of the gate-drain electric field lowering the electron injection from the gate. Both (i) and (ii) are consistent with the hypothesis of damaged gate-drain surface invoked to explain all other degradation modes. The first effect can actually derive from the generation of deeper acceptor-like traps, compensating the pre-existing, relatively-shallow donor levels and thus lowering the surface free electron density between the gate and drain contacts. The second one can be induced by the reduced positive ionized charge. This can increase the gate barrier thickness and relax the electric-field peak at the drain-end edge of the gate contact, resulting in gate-leakage reduction. The latter mechanism is, in many respects, similar to the "breakdown walkout", a well-known effect of hot-electron stress observed in GaAs-based FETs and attributed to the increase in the surface-trap density [64]. The same effects could also be induced by electron trapping and accumulation into pre-existing deep levels at the surface.

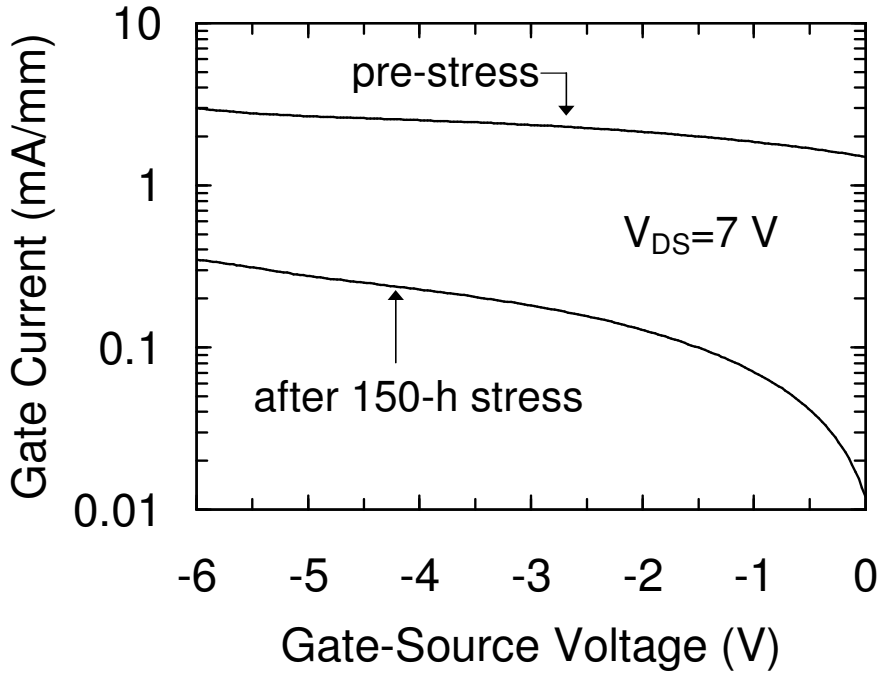

Figure 2.7: Experimental DC reverse-gate-current vs gate-source-voltage characteristics at a drain-source voltage (V_{DS}) of 7 V, before and after 150 hours of DC operation at V_{DS}=16 V and V_{GS}=0 V (power-state stress).

Figure 2.8 summarizes some of the above-described degradation modes, showing their evolution as a function of stress time. As can be noted, degradation is already appreciable after 1 hour and occurs mostly within the first 5-10 hours of stress.

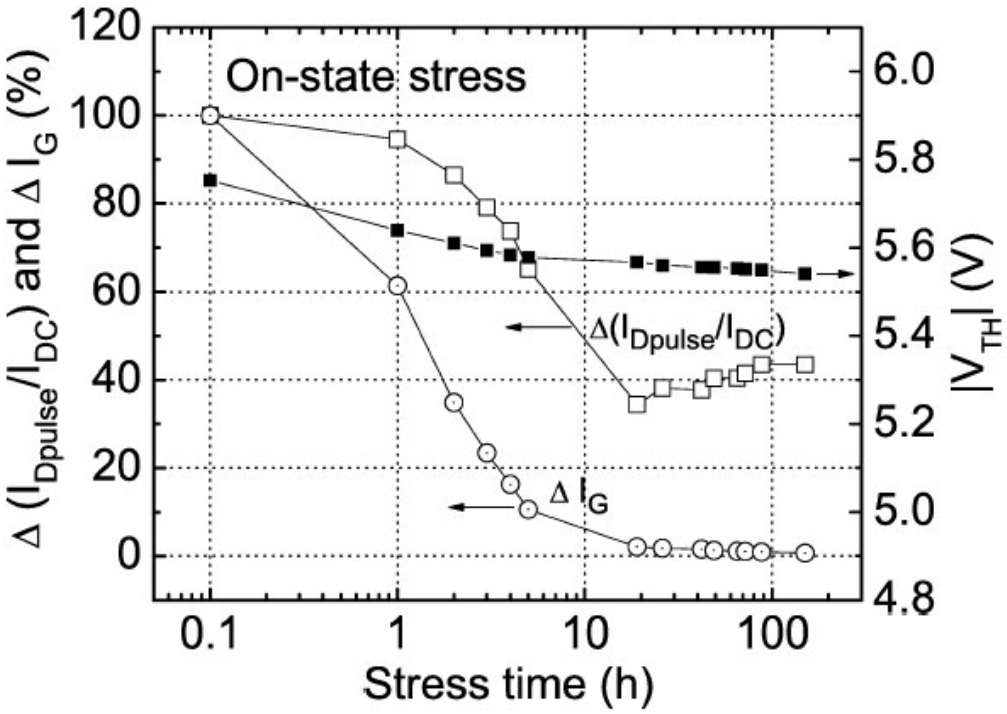

Figure 2.8: I_{Dpulse} /I_{DC} change $\Delta(I_{Dpulse}$ /$I_{DC})$, gate–current change ΔI_G, and absolute value of threshold voltage $|V_{TH}|$ as a function of Open-channel stress time. The I_{Dpulse} /I_{DC} ratio is measured for a 1-μs pulse width. I_G is measured at V_{GS} = 0 V and V_{DS} = 7 V. The sample is a doped HEMT.

2.3.2 Off-state stress degradations

Degradation modes observed after off-state stress are in most respects similar to those induced by open-channel stress: I_D and g_m drop, gate lag and the associated current collapse rise, I_G decreases. Two significant differences are however detected: (i) no V_{TH} shift is observed and (ii) g_m degradation is more pronounced in correspondence of the gm peak, whereas it is smaller at high V_{GS}.

Both aspects (i) and (ii) can be appreciated in Figure 2.9, showing g_m vs V_{GS} curves before and after 150 hours of off-state stress. As anticipated, the absence of V_{TH} shift suggests that its presence under open-channel stress is due to some thermal degradation process, most

likely to gate-contact degradation, and/or to electron trapping under the gate electrode. As far as effect (ii) is concerned, this can be explained analogously to what proposed for Si MOSFETs in [65], i.e.: a) during off-state stress, the main effect influencing the g_m vs V_{GS} curve is the degradation of the channel electron mobility, leading to the collapse of the g_m peak; b) during open-channel stress, the increase in R_D dominates, resulting in g_m collapse at high V_{GS} values. It is actually reasonable to assume that, under off-state stress, electrons mainly damage the part of the gate-drain access region located close to the gate contact, where the gate-drain electric field peaks. Traps generated in the GaN buffer, in particular, can reduce the 2DEG mobility, explaining effect a). During open-channel stress, instead, hot-electron damage extends in principle throughout the gate-drain access region, as channel electrons are also accelerated by the longitudinal field. If the damage actually concentrates far from the gate contact, its main consequence is the R_D increase, thus explaining effect b).

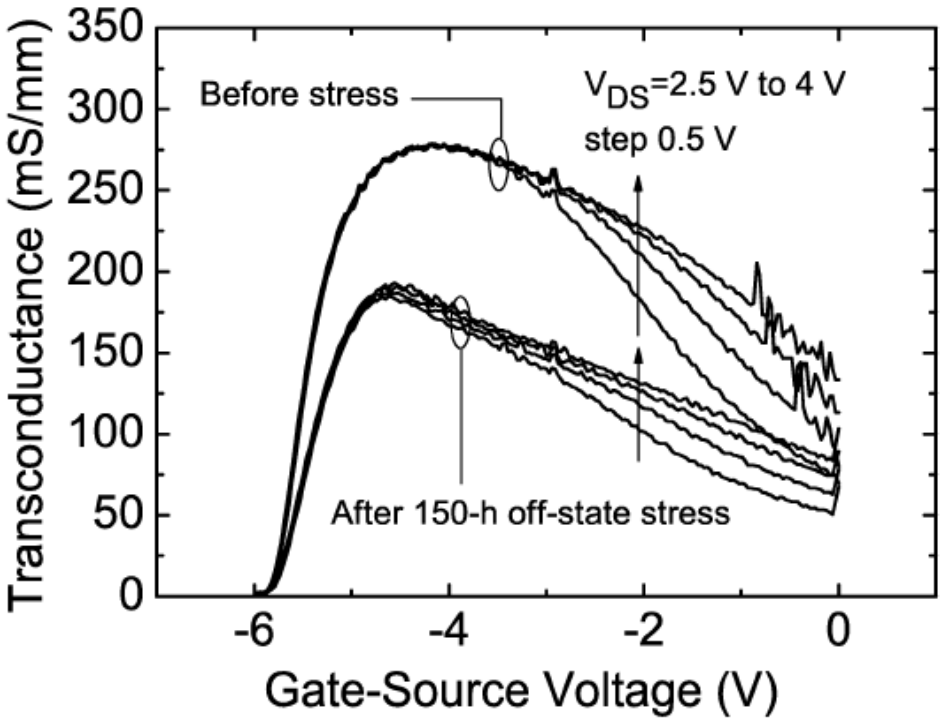

Figure 2.9: Transconductance g_m measured as a function of V_{GS} before and after Off-state stress. The drain–source voltage V_{DS} is varied from 2.5 to 4 V with a step of 0.5 V. The sample is a doped HEMT.

Figure 2.10 illustrates the time evolution of off-state-stress degradation. With respect to the open-channel-stress data shown in Figure 2.8, besides the fact that V_{TH} does not change significantly, we can note that the drop in I_{Dpulse}/I_{DC} (and the correlated I_G decrease) begins only after 6 hours of stress and is, in all, less severe than that induced by open-channel stress. This suggests that the degradation of the gate contact can contribute to the I_G decrease during the open-channel stress, summing up to the effect of surface damage and leading to enhanced I_{Dpulse}/I_{DC} degradation as well.

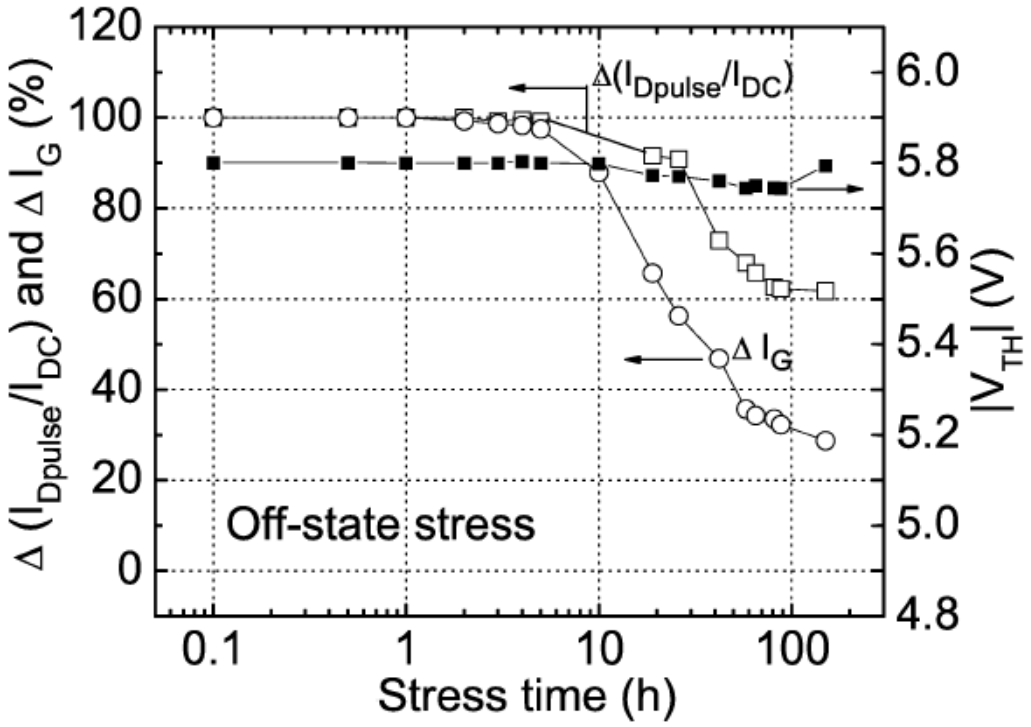

Figure 2.10: I_{Dpulse}/I_{DC} change $\Delta(I_{Dpulse}/I_{DC})$, gate–current change ΔI_G, and absolute value of threshold voltage $|V_{TH}|$ as a function of Off-state stress time. Measurement conditions for I_{Dpulse}/I_{DC} and I_G are adopted from Figure 2.8. The sample is a doped HEMT.

A feature that is common to both on- and off-state stress experiments is that all degradation effects saturate over time (see Figures 2.8 and 2.10). In [53] a similar behavior has been observed for I_D and g_m degradation after DC stress and it has been attributed to hot-electron accumulation into deep traps, which, upon being completely filled out, can not be occupied by other electrons. It must also be considered that, regardless of whether electron accumulation into pre-existing deep levels or generation of new acceptor traps take place during stress, the effect is an increase in the negative charge along the surface between gate

and drain contacts (or, better, a reduction in the positive charge associated with surface donors). This in turn leads to a broadening of the gate-drain electric-field distribution and to a consequent decrease in the electric-field peak. As a result, as stress proceeds, it becomes less and less probable that electrons have the energy to create additional damage, thus providing another possible explanation for the saturation of degradation effects.

2.4 Simulation study of possible degradation scenarios

2.4.1 Device simulations approach

Two-dimensional numerical simulations were carried out, using a commercial drift-diffusion code (Dessis8.0, Synopsys Int. Ltd). The Schottky barrier height was set to 0.9 eV. Low-field electron mobility and electron saturation velocity in the GaN channel were set to 1660 $cm^2/V \cdot s$ (in agreement with Hall measurements) and $1.2 \cdot 10^7$ cm/s, respectively. GaN and $Al_{0.28}Ga_{0.72}N$ bandgap were set to 3.42 eV and 3.98 eV, respectively, while the AlGaN-GaN conduction-band discontinuity was set to 0.45 eV [6]. The gate current was modeled as the combination of thermoionic emission plus tunneling (field emission) injection across the gate barrier and drift-diffusion transport within the semiconductor layers. Other tunneling mechanisms, beside field-emission injection, can actually contribute to I_G [66-68]. However, assessing the exact physical mechanism underlying gate current goes beyond the scope of the present work. As will be shown later, the limitation of the adopted gate-current model translates into some discrepancies between simulated and experimental I_G vs V_{GS} characteristics. Nevertheless, any model incorporating a mechanism of electric-field-dependent injection would produce qualitatively-equivalent results obtained from this work. Deep-level-trap dynamics was accounted for by including, for each distinct trap level, one trap-balance equation, describing, within the framework of standard Shockley-Read-Hall theory, the transient behavior of trap occupation without any quasi-static approximation. Figure 2.11 shows the simulated cross section, except for the AlN nucleation layer and the SiC substrate which were not included in the simulation domain. Three-dimensional (3-D) effects were neglected. They can arise from non-uniformities along the device width, resulting in the generation of hot spots and focusing degradation into a limited portion of the device [69].

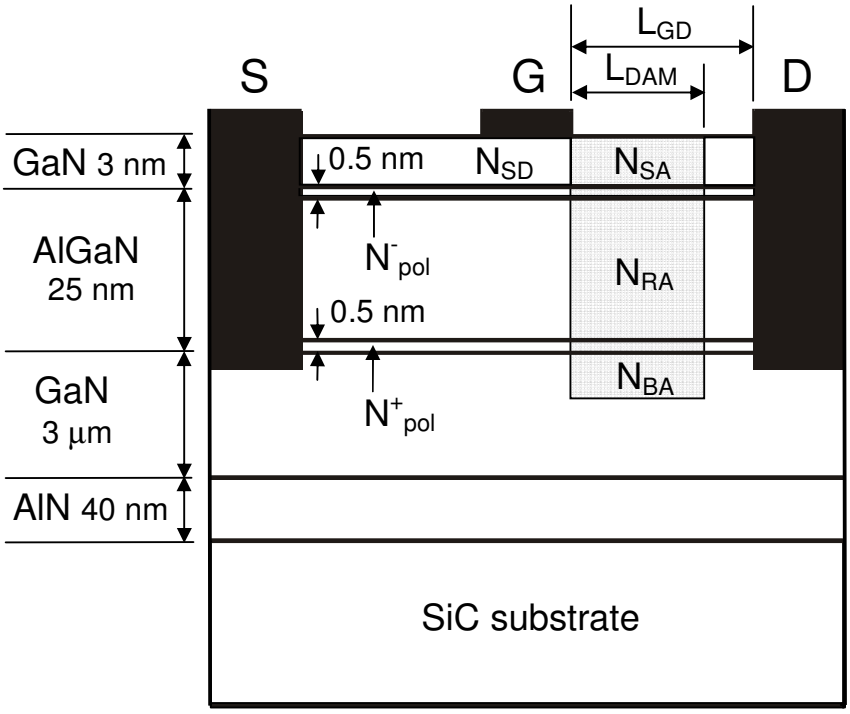

Figure 2.11: Device cross section (not to scale). Symbols are defined in the text.

To account for polarization charges at the two AlGaN-GaN heterointerfaces, positive fixed charges with a sheet density $N^+_{pol}=1x10^{13}$ cm^{-2} were placed at the bottom AlGaN-GaN interface (uniformly distributed over a 0.5-nm thick region), while negative fixed charges having an equal sheet density $N^-_{pol}=1x10^{13}$ cm^{-2} (and similarly distributed over a 0.5-nm region) were accounted for at the top GaN-AlGaN interface (see Figure 2.11). In agreement with the surface-donor theory [70], donor-like traps (N_{SD}) were assumed to be distributed throughout the GaN cap (see Figure 2.11). Despite conclusive arguments have not been reported in the technical literature about its validity in actual devices, this theory is able to explain the formation of the channel 2DEG in GaN HEMTs [70]. The positive charge associated with ionized donor traps tends in fact to compensate the negative polarization charge at the cap-to-barrier GaN-AlGaN interface, this translating into electron density increase at the barrier-to-buffer AlGaN-GaN interface. In actual devices, both surface traps at the exposed GaN surface and volume distributions of near-surface traps [66, 71] can be present. The assumed donor-trap distribution within the GaN cap must therefore be regarded as a simplified way to include the effect of both surface and near-surface defects. A good agreement between experimental and simulated

characteristics (see Figure 2.12) is achieved by assuming the following values for the donor-trap density (N_{SD}) and energy (E_{SD}): N_{SD} = 7.5x10^{12} cm^{-2}, E_{SD} = 0.1eV (from the conduction-band-edge).

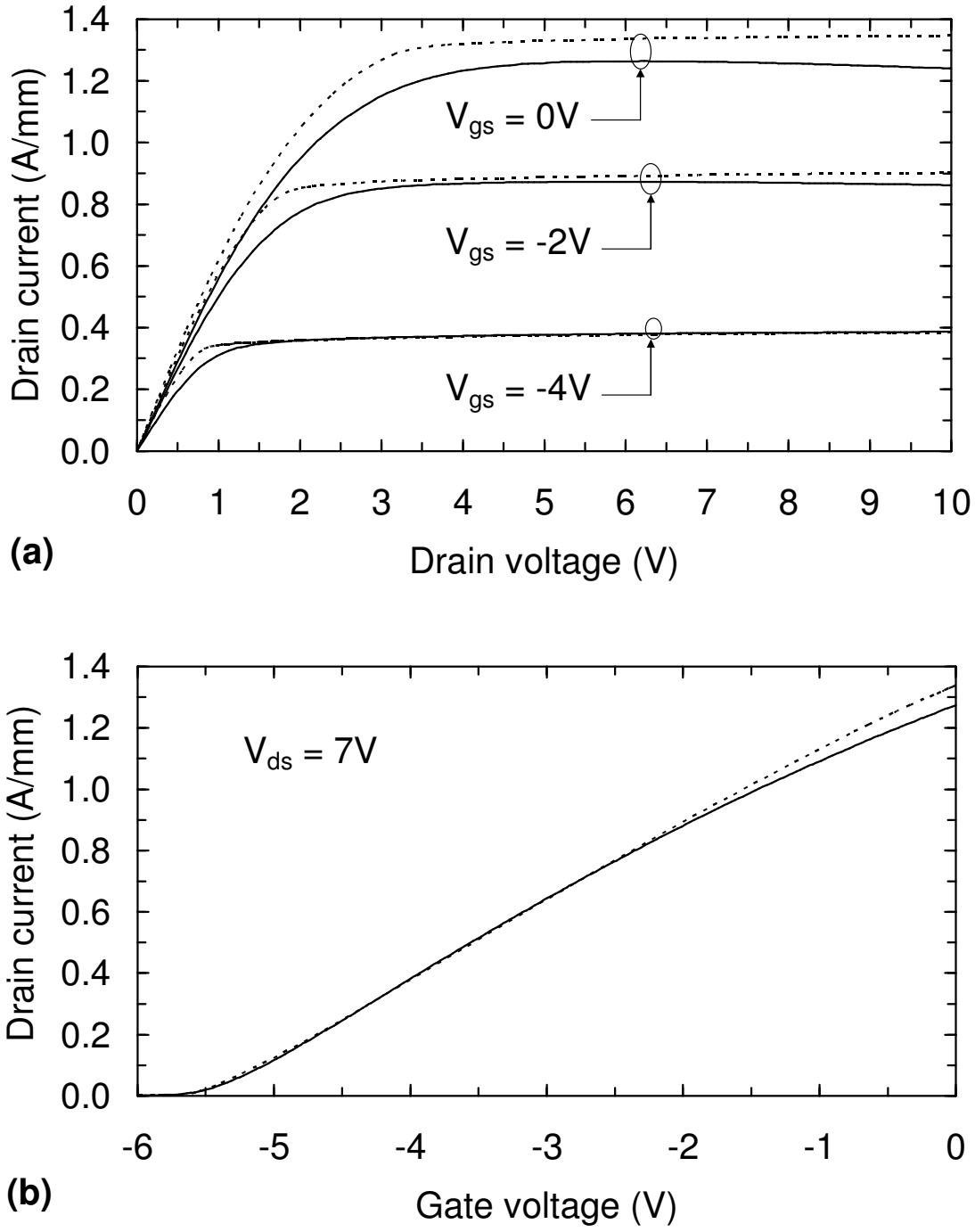

Figure 2.12: Experimental (solid) and simulated (dotted) output (a) and input (b) characteristics in the device under study prior to stress.

The discrepancy between simulated and experimental I_D at high V_{GS} can be attributed to several factors (that are neglected within simulations), including self-heating effects, drain and source contact resistances, and mobility degradation at high 2DEG densities.

The relatively-shallow energy of 0.1 eV for the donor traps in the cap is, in particular, at the origin of the negligible current-collapse effects and the large reverse gate currents exhibited by the devices under study prior to stress. As a matter of fact, the gate-lag mechanism suggested by the simulations agrees with the concept of "virtual gate" as proposed in [36] and can be understood with the aid of Figure 2.13, showing the (free) electron density [Figure 2.13(a)] and the ionized-donor-trap density [Figure 2.13(b)] along the cap gate-drain region at V_{GS} =-5 V and V_{GS}=0 V for two different values of E_{SD} (E_{SD}=0.1 eV and E_{SD}=0.3 eV). When the device is biased at a negative and large-in-modulus V_{GS}, significant gate electron injection takes place, concentrated, due to the positive V_{DS} applied, at the drain-end of the gate contact. Part of injected electrons flows laterally through the GaN cap. As a consequence, the electron density within the cap access region is relatively large [see curves for V_{GS}=-5 V in Figure 2.13(a)]. Electron trapping takes place, reducing the ionized-trap-density [see curves for V_{GS}=-5 V in Figure 2.13(b)]. Of course, the deeper the donor-trap energy, the smaller the (free) electron and the ionized donor-trap densities (compare curves for E_{SD}=0.1 eV and E_{SD}=0.3 eV at V_{GS}=-5 V). When V_{GS}=0 V, electron injection from the gate is instead negligible and the negative polarization charge at the cap-to-barrier interface efficiently depletes the cap layer. The density of free electrons in the cap is small [see curves for V_{GS}=0 V in Figure 2.13(a)], thus suppressing electron capture. Correspondingly, donor traps are completely ionized [see curves for V_{GS}=0 V in Figure 2.13(b)]. As V_{GS} is stepped from a negative value to 0 V, electrons must therefore be emitted by traps, giving rise to a turn-on transient whose amplitude and time constant depend on the trap energy. Emitted electrons flow to the drain contact through the cap (where they are vertically confined by the cap-to-barrier potential barrier). The smaller E_{SD}, the higher the electron emission rate and therefore the shorter the turn-on transient. Moreover, a smaller E_{SD} results into a higher ionized-donor-trap density for the same initial V_{GS}. This reduces the total number of electrons that need to be emitted during the turn-on transient to recover steady-state conditions, thus leading to gate-lag amplitude reduction. For E_{SD}=0.1 eV, gate-lag effects are predicted to be negligible, in agreement with experimental results.

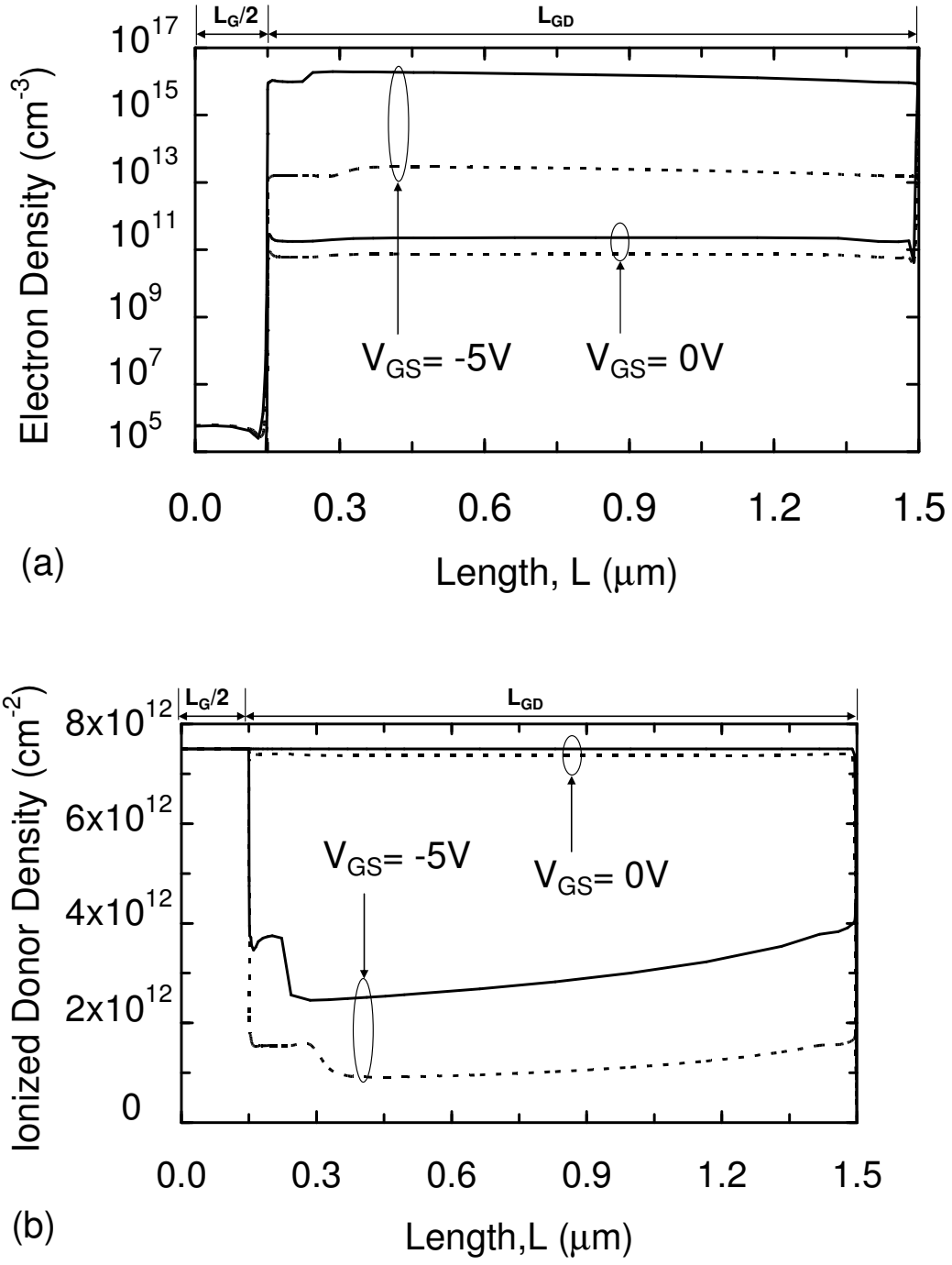

Figure 2.13: Simulated electron-density (a) and ionized-donor-density (b) distributions within the cap layer as a function of device length for V_{GS}=-5 V and V_{GS}=0 V at V_{DS}=7 V. Solid and dashed curves are obtained by assuming E_{SD}=0.1 eV, and E_{SD}=0.3 eV, respectively. Only the drain-side half of the device is shown and the length (L) zero is assumed at the gate midpoint.

On the other hand, the large positive charge associated with ionized donor traps shrinks the gate potential barrier, giving rise to large electron injection from the gate under reverse gate bias. Although quantitative discrepancies with experiments can arise owing to the simplified gate-current model adopted, the above effect can explain the excess gate leakage currents observed in these devices.

The value of 0.1 eV for E_{SD} allowed for a semi-quantitative matching between experimental and simulated gate-lag waveforms and DC reverse gate currents in unstressed devices. It should, however, not be regarded as an accurate extraction of the energy depth of surface-donor traps in these devices. Approximations inherent in the adopted simulation scheme can actually affect the accuracy of E_{SD}. These include: (i) the possibility that multiple trap energy levels and/or a continuum of energy states exist within the cap and/or at the device surface; (ii) the uncertainty on the trap cross sections (that were set to a typical value of 10^{-15} cm^2 in our simulations); (iii) the influence of self-heating effects (that were neglected in our simulations) on the rise time of gate-lag waveforms; (iv) the contribution of possible, non-bulk properties of the GaN cap and/or of nonideal transport mechanisms at the device surface.

With the aim of explaining degradation effects shown earlier, several different degradation scenarios were taken into consideration and are described in the following subsections. Trap generation was initially assumed to take place over the whole drain access region, extending from the drain-end of the gate contact to the drain contact. Five different scenarios (*degradation scenarios A to E*) were considered, differing for the device layer(s) where stress-induced traps are assumed to accumulate. Stress-induced traps were, in all cases, assumed to be acceptor-like traps, that are negatively charged when occupied by electrons. Only in this case, a growing density of traps results into a decreasing 2DEG density at the barrier-to-buffer interface, thus explaining I_D and g_m drops that are always observed as a result of high-electric-field stress. The effect of reducing the lateral extension of the trap-generation region was then analyzed, with the aim of validating the hypothesis that a different localization of the stress-induced trap generation within the drain access region can be at the origin of the different g_m degradation effects observed in these devices as a result of the two stress bias conditions adopted. The effect of channel mobility and saturation velocity degradation was finally taken into account.

2.4.2 Degradation scenario A (Surface-trap generation)

Gate-lag effects are generally attributed to surface traps [72]. The amplification of gate-lag amplitude is a commonly observed degradation effect, that is considered a signature of trap generation within the drain access region [46,51,58,72]. Since both open-channel and off-state stresses were found to produce amplification of gate-lag effects, in a first attempt to explain the observed degradation phenomena, acceptor-like traps were placed at the gate-drain surface only. Traps were actually distributed over the 3-nm GaN cap layer, where the pre-existing donor-like traps were assumed to be present as well. Under this hypothesis and with reference to Figure 2.11, the cap acceptor-trap density per unit area (N_{SA}) is different from 0, whereas both barrier (N_{RA}) and buffer (N_{BA}) acceptor-trap densities are zero. The length of the trap-generation region (L_{DAM}) was assumed to coincide with the whole gate-drain spacing (L_{GD}). This degradation scenario will hereafter be referred to as *degradation scenario A*.

Figures 2.14(a) and 2.14(b) show simulated I_D vs time waveforms in response to a turn-on V_{GS} step (V_{GS} stepped from -5 V to 0 V at V_{DS}=7 V) for pre-stress conditions and under the post-stress scenario A. In Figure 2.14(a), E_{SA} is varied, while N_{SA} is kept constant at the value of $3x10^{12}$ cm^{-2}. In Figure 2.14(b), N_{SA} is varied, whereas E_{SA}=0.6 eV. As can be noted from Figures 2.14(a) and 2.14(b), the degradation scenario A is actually able to explain gate-lag amplification with respect to pre-stress conditions. Owing to trapping of gate-injected electrons, acceptor-like traps get negatively ionized when V_{GS} is negative and large in modulus, leading to 2DEG density decrease in the drain access region. Traps emit electrons as V_{GS} is stepped to high values, giving rise to the slow recover of 2DEG density and I_D values, thus explaining gate lag and the associated current-collapse effect. As shown in Figure 2.14(a), E_{SA} must, in particular, be assumed to be ≈0.6 eV, in order for gate-lag effects to be characterized by a time constant in the order of 1 s, acceptably matching that governing experimental I_D vs time transients after stress. Considerations similar to those already stated about the accuracy of the adopted E_{SD} value apply to the accuracy of E_{SA}, as well. In particular, neglecting self-heating effects in the simulations results in the underestimation of the E_{SA} value yielding a time constant in agreement with experiments. As a matter of fact, approximately the same time constant of about 1 s would be obtained by assuming E_{SA}=0.7 eV at the channel temperature of 358 K that can be estimated for the final, dc conditions of Figure 2.14, by relying on data reported in [73,74].

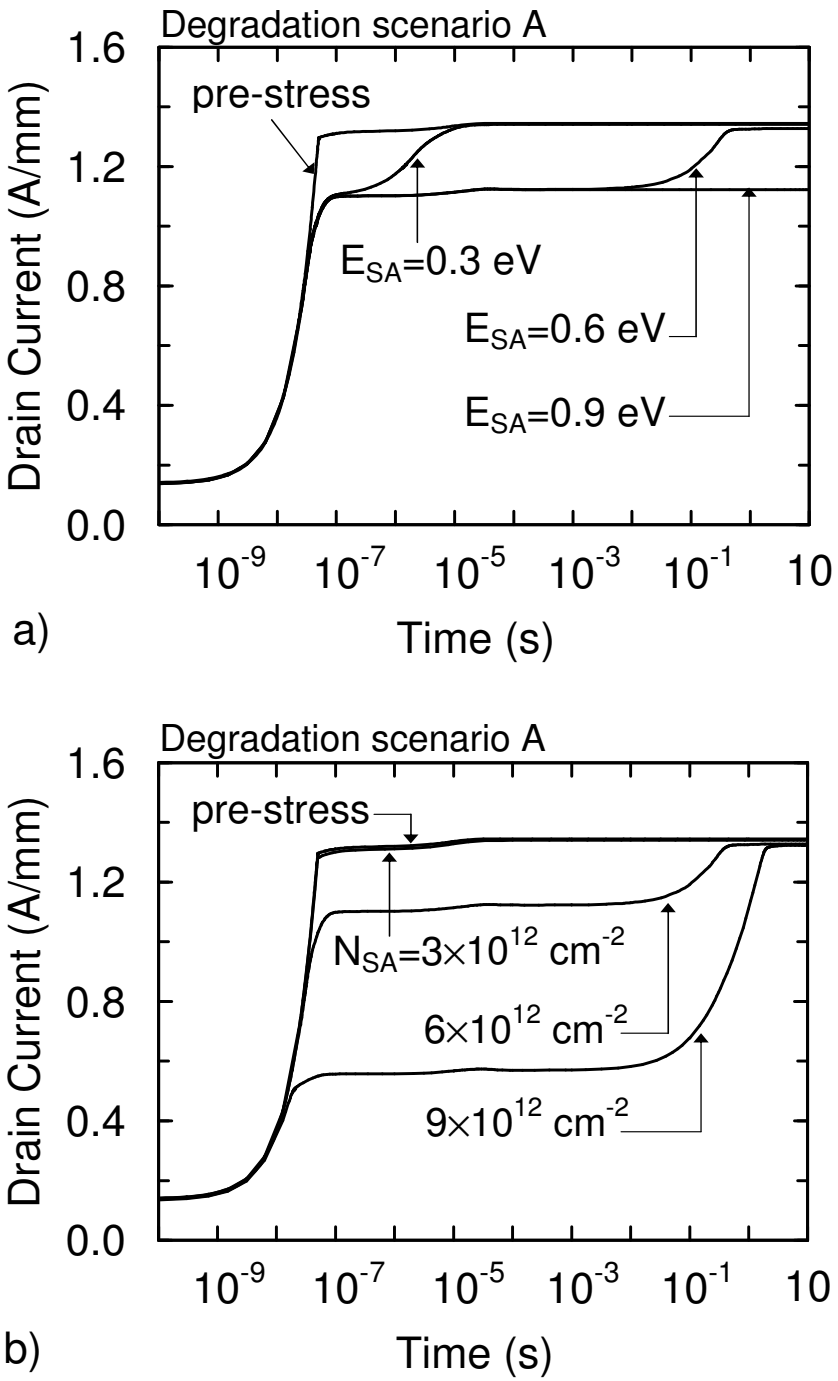

Figure 2.14: Simulated drain-current vs time waveforms in response to a turn-on gate-source-voltage (V_{GS}) step (V_{GS} stepped from -5 V to 0 V at a V_{DS}=7 V) for pre-stress conditions and the degradation scenario A. In (a) the energy with respect to conduction band (E_{SA}) of the acceptor traps in the cap is varied, while the trap density (N_{SA}) is kept constant at the value of 3x10^{12} cm^{-2}. In (b) N_{SA} is varied, whereas E_{SA}=0.6 eV.

N_{SA} should then be ≈9x10^{12} cm^{-2} to achieve a current-collapse magnitude (i.e., the difference between the values assumed by I_D under final, DC conditions and immediately after the application of the V_{GS} step) comparable with that observed experimentally.

Figure 2.15 shows simulated DC I_G vs V_{GS} characteristics at V_{DS}=7 V for pre-stress conditions and for different N_{SA} values (with E_{SA}=0.6 eV). The simulated I_G is more dependent on V_{GS} than the experimental one and it is much smaller than the experimental one for V_{GS} values small in modulus. These discrepancies are attributed to enhanced surface conduction that could not be accounted for by simulations. Ionized acceptor traps tend to compensate the positive charge associated with surface donor traps. As suggested by inspection of internal potential and electric-field distributions, this leads to the broadening of the gate potential barrier and to the consequent decrease in the electric-field peak at the drain-end of the gate. This in turn results in gate electron injection reduction, thus explaining the drop of the reverse I_G at increasing N_{SA} shown in Figure 5. The degradation scenario A is therefore able to explain also the decrease in the reverse I_G observed after stress.

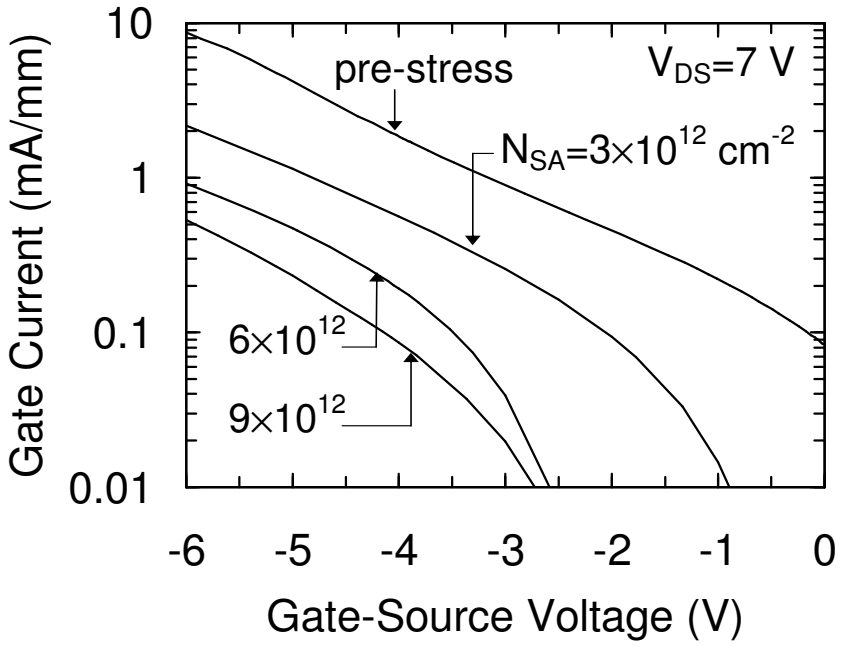

Figure 2.15: Simulated gate-current vs V_{GS} characteristics at a V_{DS} of 7 V for pre-stress conditions and the degradation scenario A for different cap acceptor trap densities (N_{SA}) and a trap energy of 0.6eV (from the conduction-band edge).

The simulated output characteristics are finally shown in Figure 2.16. The curves at V_{GS}=0 V are, in particular, reported for pre-stress conditions and for different N_{SA} values (with E_{SA}=0.6 eV). As can be noted, increasing N_{SA} up to $9x10^{12}$ cm^{-2} lowers only slightly the I_D curve. This means that the degradation scenario A is not able to explain the large I_D drop induced by stress. As a matter of fact, at high V_{GS}, gate electron injection is small and surface acceptor traps are therefore almost completely neutral. For this reason, the 2DEG density in the underlying channel access region and the DC I_D values are only marginally impacted by the N_{SA} increase.

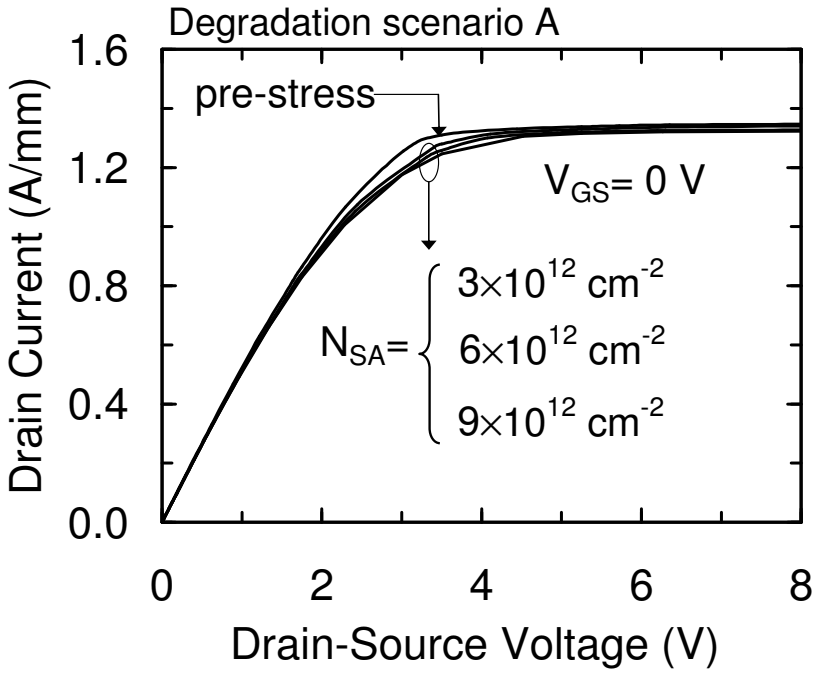

Figure 2.16: Simulated DC drain-current vs drain-source-voltage characteristics at a V_{GS} of 0 V for pre-stress conditions and the degradation scenario A for different cap acceptor trap densities (N_{SA}) and a trap energy of 0.6 eV (from the conduction-band edge).

2.4.3 Degradation scenario B (Barrier-trap generation)

As a second possible degradation scenario, acceptor traps were placed in the AlGaN barrier layer. With reference to Figure 1, $N_{RA} \neq 0$, $N_{SA} = N_{BA} = 0$, $L_{DAM} = L_{GD}$. This degradation scenario will be referred to as *degradation scenario B*.

Obtained results are qualitatively the same as for scenario A. Gate-lag amplification is reproduced by simulations and can be explained as the consequence of the capture and

emission of gate-injected electrons. Similarly, the reverse I_G is predicted to drop at increasing N_{RA}, as a consequence of gate potential-barrier broadening and attendant gate electron injection reduction. The DC I_D drop observed at high V_{GS} after stress can, however, not be matched by simulations. This happens because gate electron injection is small at high V_{GS} and almost all barrier traps are therefore neutral.

From a quantitative point of view, however, the barrier trap density per unit area (N_{RA}) must be increased by about one order of magnitude with respect to the N_{SA} values assumed under the degradation scenario A, to obtain the same current-collapse magnitude and reverse I_G drop. In this respect, simulations point out that only the acceptor traps closer to the gate contact are in fact reached by gate-injected electrons and become negatively charged under reverse V_{GS}.

2.4.4 Degradation scenario C (Buffer-trap generation)

Another possibility is that defect generation is induced in the GaN buffer layer. To explore this eventuality, acceptor-like traps were placed in the buffer drain access region. Traps were in particular distributed over a thin layer (3 nm) underneath the AlGaN-GaN heterointerface. With reference to Figure 1, $N_{BA} \neq 0$, $N_{SA} = N_{RA} = 0$, $L_{DAM} = L_{GD}$. This degradation scenario will be referred to as *degradation scenario C*.

Figure 2.17 shows simulated DC I_D vs V_{DS} characteristics at V_{GS}=0 V for pre-stress conditions and for different N_{BA} values. The buffer-trap energy was set to 0.33 eV (from the conduction-band edge) as extracted from low-frequency g_m dispersion measurements carried out on stressed devices. As can be noted, the DC drain current decreases significantly at increasing N_{BA}. Differently from surface or barrier traps, which require negative V_{GS} voltages and the attending large gate electron injection to get negatively charged, buffer traps are mostly ionized even at small V_{GS}, as a result of the large channel electron density. The DC drain current is, therefore, much more sensitive to the buffer-trap density than to the surface- or barrier-trap ones, compare Figures 2.16 and 2.17. For the same reason, buffer traps substantially behave as fixed negative charge during the turn-on transients induced by V_{GS} pulsing. As a result, they can not give rise to significant gate-lag effects.

Similarly to degradation scenarios A and B, finally, the degradation scenario C can account for the stress-induced reverse I_G drop, explaining it as the consequence of the gate-drain potential barrier broadening.

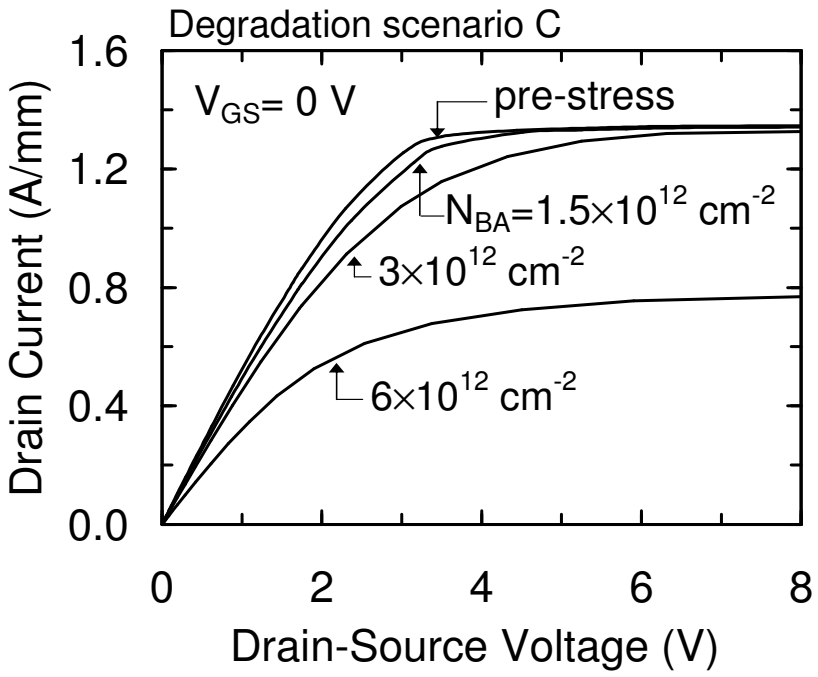

Figure 2.17: Simulated DC drain-current vs drain-source-voltage characteristics at a gate-source voltage (V_{GS}) of 0 V for pre-stress conditions and the degradation scenario C for different buffer acceptor trap densities (N_{BA}) and a trap energy of 0.33 eV (from the conduction-band edge).

2.4.5 Degradation scenarios D (Surface- and buffer-trap generations) and E (Surface-, barrier-, and, buffer-trap generations)

None of the degradation scenarios considered so far is able to account simultaneously for all degradation effects observed experimentally after either open-channel or off-state stress. More particularly, degradation scenarios A and B can reproduce both gate-lag amplification and reverse I_G drop, but they are unable to explain the DC I_D drop at high V_{GS}. The latter effect, as well as the reverse I_G drop, can, on the other hand, be justified by the degradation scenario C, that is however unable to account for gate-lag amplification. This led to the consideration of two additional scenarios, namely the simultaneous

generation of acceptor traps (i) in the cap and buffer layers (degradation scenario D) and (ii) in the cap, in the barrier, as well as in the buffer layers (degradation scenario E). With reference to Figure 2.11, $N_{SA} \neq 0$, $N_{BA} \neq 0$, $N_{RA}=0$ for the degradation scenario D, whereas $N_{SA} \neq 0$, $N_{BA} \neq 0$, $N_{RA} \neq 0$ for the degradation scenario E. In both cases $L_{DAM} = L_{GD}$.

Figures 2.18-2.20 show simulated gate-lag transients, DC reverse I_G vs V_{GS} curves, and DC output characteristics at $V_{GS}=0$ V, respectively. Specific trap parameters adopted are as follows. The cap (E_{SA}) and barrier (E_{RA}) trap energies were set to 0.6 eV (same as for degradation scenarios A and B), whereas the buffer trap energy (E_{BA}) was set to 0.33 eV (same as for degradation scenario C). Trap densities were assumed to be $N_{SA}=4.5\text{x}10^{12}\text{cm}^{-2}$ and $N_{BA}=3.75\text{x}10^{12}$ cm^{-2} for degradation scenario D, while $N_{SA}=2.25\text{x}10^{12}$ cm^{-2}, $N_{RA}=2.25\text{x}10^{13}$ cm^{-2}, $N_{BA}=3.75\text{x}10^{12}$ cm^{-2} for degradation scenario E.

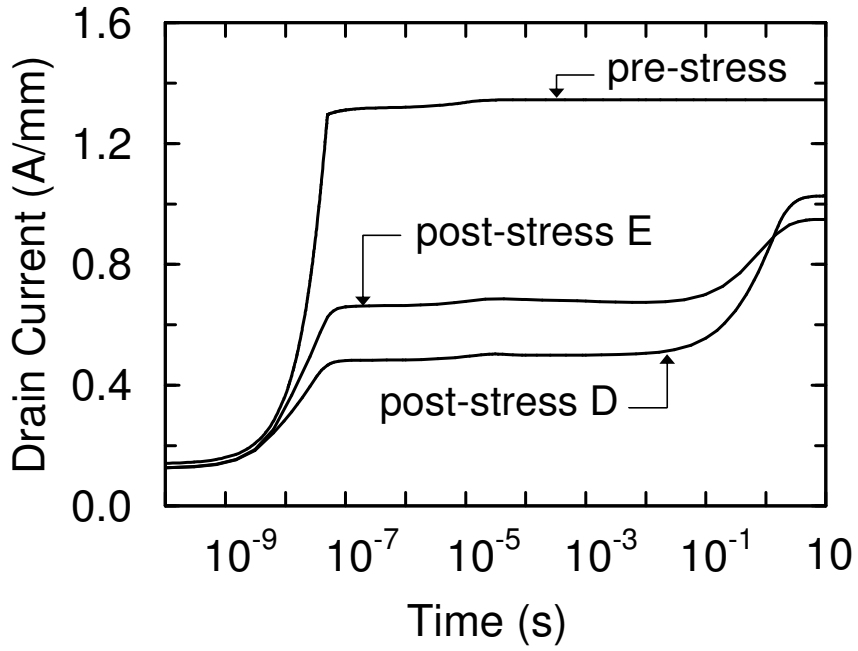

Figure 2.18: Simulated drain-current vs time waveforms in response to a turn-on gate-source-voltage (V_{GS}) step (V_{GS} stepped from -5 V to 0 V at a drain-source voltage $V_{DS}=7$ V) for pre-stress conditions and the degradation scenarios D and E.

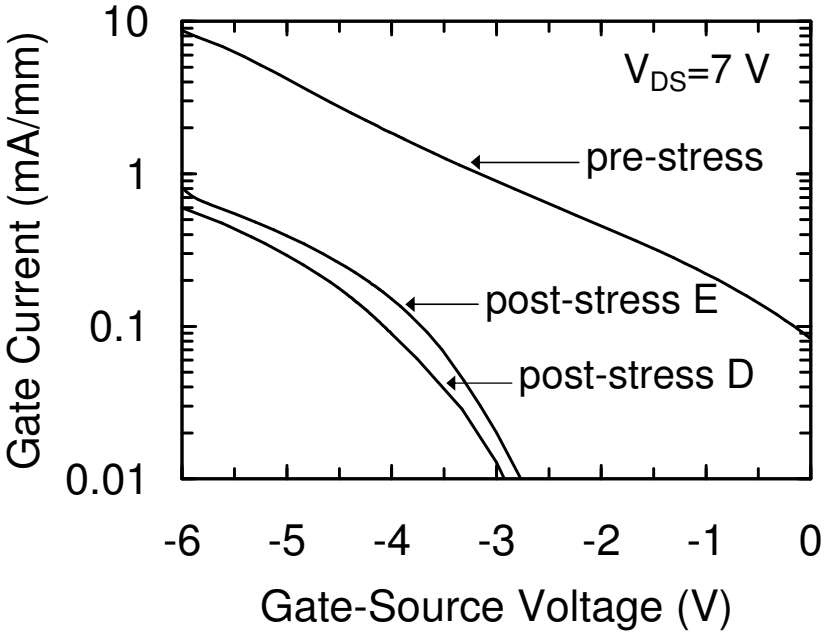

Figure 2.19: Simulated DC gate-current vs gate-source-voltage characteristics at a V_{DS} of 7 V for pre-stress conditions and the degradation scenarios D and E.

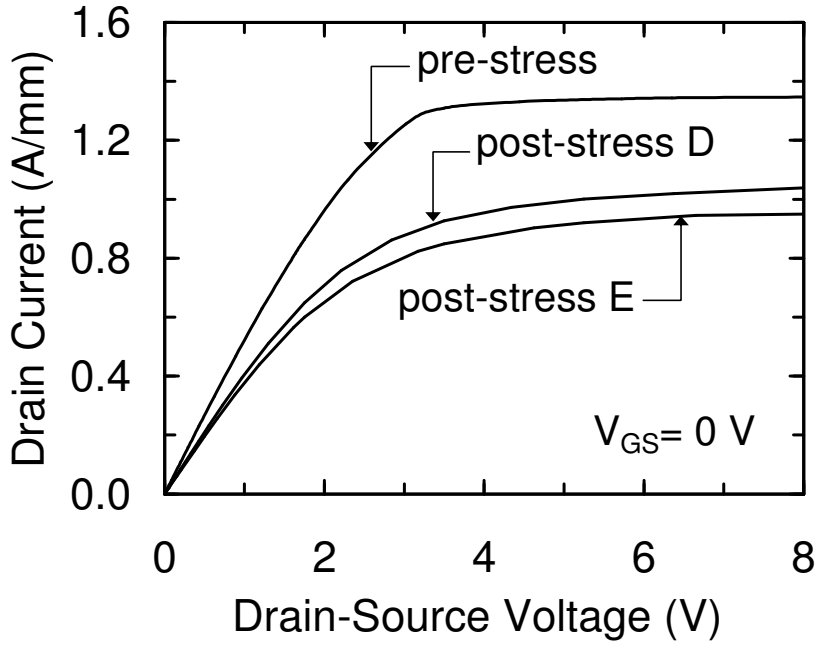

Figure 2.20: Simulated DC drain-current vs drain-source-voltage characteristics at a V_{GS} of 0 V for pre-stress conditions and the degradation scenarios D and E.

As anticipated earlier, N_{RA} must be about 10-x larger than N_{SA} to induce comparable effects. With the above values for trap densities, the combined effects of cap and barrier traps in the degradation scenario E are comparable with those associated with cap traps under the degradation scenario D. Similar degradation effects are therefore predicted by simulations reported in Figures 2.18-2.20 for the two degradation scenarios D and E. More importantly, both degradation scenarios D and E are able to reproduce all degradation modes observed experimentally, i.e. gate-lag amplification (see Figure 2.18), reverse I_G drop (see Figure 2.19), as well as DC I_D decrease (see Figure 2.20). Gate lag is mainly controlled by the acceptor traps in the cap (degradation scenario D) and in both cap and barrier layers (degradation scenario E). The DC I_D drop is instead mostly induced by acceptor traps placed in the buffer layer. All of the three acceptor-trap regions contribute, finally, to the reverse I_G drop.

2.4.6 Extension of the trap-generation region

It is reasonable to assume that DC stresses carried out under different bias conditions can result in differently located trap-generation regions, as a consequence of the distinctive electric-field pattern applied to the device during stress. Since we observed qualitatively-different g_m degradation effects after power-state and off-state stresses [see Figures 2.5 and 2.9], we were interested in assessing whether the extension of the trap-generation region has an impact on the g_m curve.

Figure 2.21 summarizes the results of this kind of analysis, showing simulated g_m vs V_{GS} curves at a V_{DS} of 7 V for pre-stress conditions and different widths (L_{DAM}) of the trap-generation region (see Figure 2.11). Acceptor traps were placed in the cap, in the barrier, as well as in the buffer. Trap volume densities and trap energies were the same as those assumed for the degradation scenario E. L_{DAM} was varied from $L_{GD}/16$ (corresponding to ≈84 nm) to L_{GD} (=1.35 μm). As can be noted, increasing L_{DAM} amplifies the g_m drop at high V_{GS}, without affecting appreciably the g_m peak. Increasing L_{DAM} actually increases the drain access resistance. The latter mostly impacts g_m in the high-V_{GS} range, where the resistance of the intrinsic channel is small and the voltage drop across the drain access region is large (the total drain-to-source voltage being fixed). Similar effects on the g_m vs V_{GS} curve are predicted by simulations, when the volume density of acceptor traps is increased for a given L_{DAM} value. In any case, the g_m peak is not appreciably affected by

either L_{DAM} or trap-density increase. Besides trap generation, ohmic-contact degradation can contribute to access-resistance increase and therefore to I_D and g_m degradation.

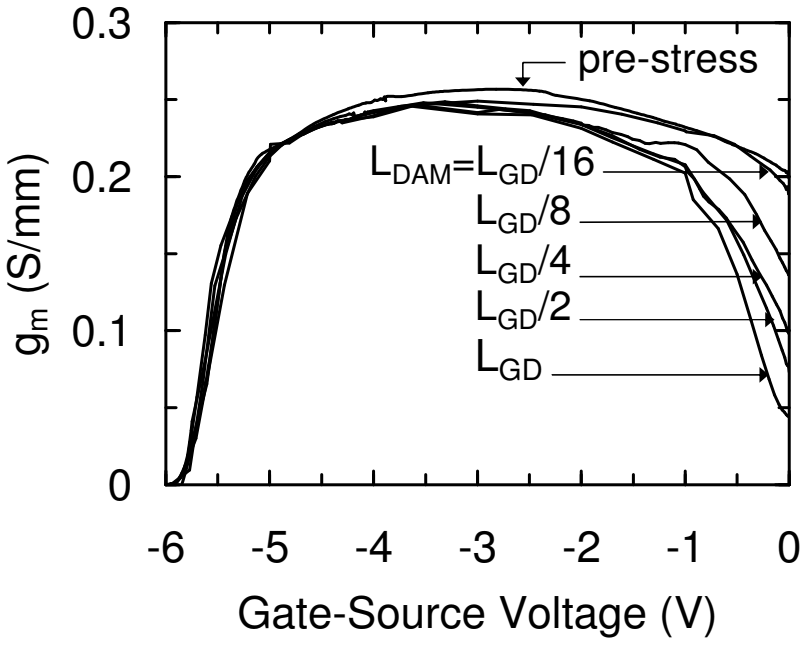

Figure 2.21: Simulated transconductance (g_m) vs gate-source-voltage curves at a drain-source voltage (V_{DS}) of 7 V for the pre-stress conditions and different lengths (L_{DAM}) of the trap-generation region. Acceptor traps are placed in the cap, in the barrier, as well in the buffer. The case for which $L_{DAM}=L_{GD}$ corresponds to the degradation scenario E.

A final remark about Figure 2.21 is that simulations do not reproduce the V_T shift observed experimentally after power-state stress, see Figure 2.5. Stress-induced positive V_T shifts were observed by other authors after on-state DC and RF stresses and were attributed to (i) thermally-induced modification of the gate-contact interfacial layer [63], or (ii) hot-electron trapping under the gate [45,55]. In spite of device-technology and stress-condition differences, we believe that effect (i) and/or (ii) can be at the origin of the V_T shift observed in the devices under study. In our simulations we did not change the Schottky barrier height for stressed devices and we did not include self-heating effect. For these reasons, simulations can not reproduce the V_T shift observed experimentally.

In spite of the quantitative discrepancies between experimental and simulated g_m curves, two important conclusions can be inferred from Figure 2.21: (i) the large g_m drop at high

V_{GS} characterizing open-channel stress (see Figure 2.5) is consistent with a relatively-wide L_{DAM} value, whereas, for off-state stress, trap generation must be concentrated within a narrower region in proximity of the gate edge, since, in this case, experiments show that the g_m curve drops uniformly over the entire V_{GS} range (see Figure 2.9); (ii) trap generation alone is unable to account for the observed g_m drop at low and intermediate V_{GS} values observed after off-state stress (compare Figures 2.9 and 2.21).

During power-state stress, channel hot electrons plausibly play a role, (i) by surmounting the AlGaN-GaN potential barrier and generating defects in the barrier and/or the cap, as well as (ii) by penetrating into the buffer and thereby inducing defects. In this regard, Figure 2.22 shows the longitudinal electric field along the barrier-to-buffer interface for the same bias conditions adopted during power-state stress (i.e. V_{GS}=0 V and V_{DS}=16 V). Only the drain-side half of the device is shown and the length (L) zero is assumed at the gate midpoint.

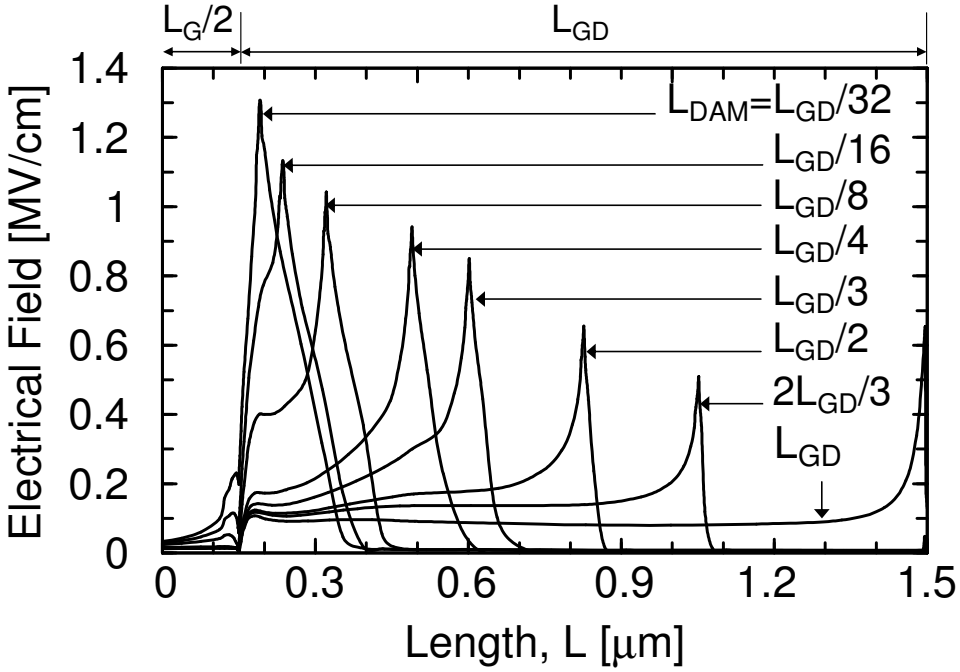

Figure 2.22: Longitudinal electric field along the barrier-to-buffer interface for the same bias conditions adopted during open-channel stress (i.e. V_{GS}=0 V and V_{DS}=16 V) for different L_{DAM} values. Only the drain-side half of the device is shown and the length (L) zero is assumed at the gate midpoint. Trap volume densities and energies are same as for degradation scenario E.

Electric-field distributions are reported for different L_{DAM} values (same trap volume densities and energies as for degradation scenario E). As can be noted, the electric-field peak lies always at the end of the trap-generation region (i.e., at $L=L_G/2+L_{DAM}$). Moreover, it decreases at increasing L_{DAM}.

Acceptor-trap density is assumed to be constant throughout the L_{DAM} region and zero outside. This approximation can impact the shape of the electric-field profile, leading, in particular, to an overestimation of the electric-field peak located at the end of the trap region. From Figure 2.22, indications can be inferred about the lateral extension of the trap-generation region induced by channel hot electrons under open-channel stress.

In unstressed devices, the longitudinal electric field (and, consequently, the electron energy) peaks close to the corresponding drain-end edge of the gate in the channel ($L=L_G/2=0.15$ μm in Figure 2.22). In the early phase of stress, hot electrons can therefore generate traps only within a narrow slice of the drain access region close to the gate edge. After a narrow trap-generation region is induced, the electric-field peak will move to higher L. Correspondingly, the trap-generation region will tend to extend laterally towards the drain contact. As shown by Figure 2.22, this will make the electric-field peak to shift further. This process can result in a trap-generation region extending significantly towards the drain contact [it can actually proceed as long as the peak electric field (that decreases at increasing L_{DAM}) is large enough to allow for hot-electron injection over the AlGaN-GaN barrier and into the buffer]. These considerations are in agreement with conclusions drawn from Figure 2.21 regarding the effect of power-state stress on the g_m curve.

Yielding more quantitative indications about the lateral extension of the trap-generation region is very difficult. It would require to use more complicated simulation approaches (like the hydrodynamic or the Monte-Carlo one) for evaluating the spatial and energy distribution of hot electrons, and, much more difficult, to have reliable models for predicting the rate of trap generation. In other words, it would require the degradation process itself (and not simply its effects on the device performance corresponding to different trap distributions) to be simulated.

2.4.7 Degradation of the Channel Transport Parameters

As already concluded from the analysis of Figure 2.21, trap generation alone is unable to explain the features of g_m degradation induced by off-state stress. By analogy with

degradation effects observed in Si MOSFETs [65], it was speculated that channel-mobility decrease could play a major role in off-state stress. To explore this hypothesis, we analyzed the impact on the g_m curve of a decrease in both low-field electron mobility (μ_n) and electron velocity saturation (v_{sat}) in the intrinsic channel. Figure 2.23 shows simulated g_m vs V_{GS} curves at a V_{DS} of 7 V for pre-stress conditions and different values of μ_n and v_{sat} percentage reduction. As can be noted, the g_m curve decreases almost rigidly at increasing μ_n and v_{sat} degradation. In agreement with conclusions drawn from Figure 2.21, acceptor traps were placed in a narrow region of the drain-access region ($L_{DAM}=L_{GD}/16\approx84$ nm) within the cap, the barrier, and the buffer (same trap volume densities and trap energies as for degradation scenario E), this preventing g_m from dropping predominantly at high V_{GS}.

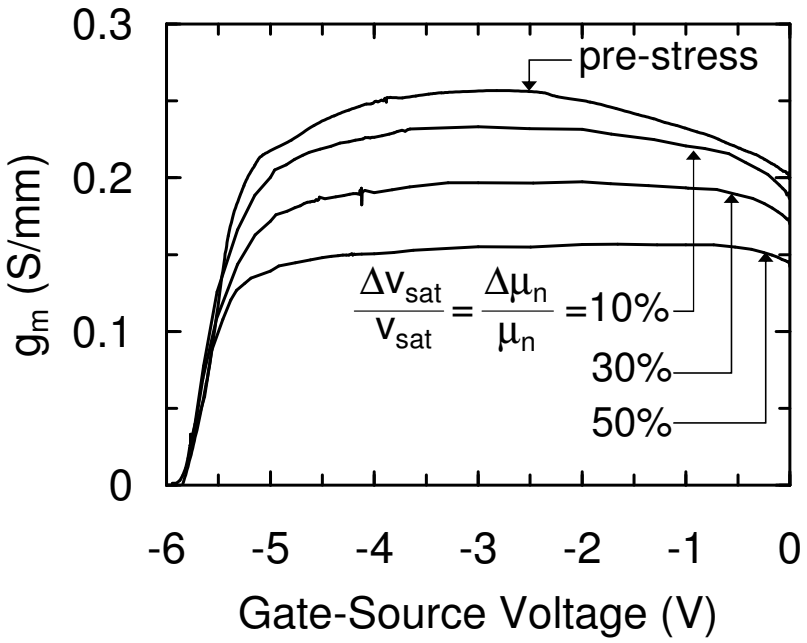

Figure 2.23: Simulated transconductance (g_m) vs gate-source-voltage curves for different values of electron-mobility and saturation-velocity degradation. Except for pre-stress conditions, acceptor traps are placed in the cap, in the barrier, and in the buffer, over a localized region of length $L_{DAM}=L_{GD}/16\approx84$ nm. Mobility and saturation velocity are changed within the intrinsic channel as well as in the localized trap-generation region.

The reduction in v_{sat}, makes g_m to decrease over the entire V_{GS} range where the device is on (owing to the high V_{DS} value, the impact of the μ_n reduction is much less relevant). Current-collapse effects were reported to be suppressed by UV illumination in [44] and [47]. This effect was attributed to trapped electron recombination with light-generated holes [44] or to photon-induced electron detrapping [47]. On the other hand, the g_m degradation after 12 h off-state DC stress was reported not to be recoverable by UV laser illumination in [46]. Our simulations suggest that g_m degradation observed after off-state stress might be induced by the decrease in μ_n and v_{sat}. These effects should not be recoverable under UV illumination similarly to what observed in [46].

In Figure 2.23, $\Delta\mu_n/\mu_n$ and $\Delta v_{sat}/v_{sat}$ were, for simplicity, assumed to be equal and they were varied from 0 to 50%. By comparing Figure 2.23 with Figure 2.9, one can roughly estimate that the degradation of channel transport parameters should be ≈30%, in order for simulations to qualitatively reproduce the degraded g_m curve obtained experimentally. As for the responsible physical mechanism, strain enhancement induced by the large vertical electrical field, followed by strain relaxation and consequent defect creation [58,62], is, in this case, likely to play a major role. The same mechanism can actually contribute to power-state degradation, as well.

In this regard, Figure 2.24 shows the vertical electric field profile at midgate (L=0) and two different positions within the drain access region (L=0.6 μm and L=1.2 μm) for both power-state-stress and off-state-stress bias conditions. As can be noted, the vertical electric field is (for any lateral position) about a factor of two larger in off-state than in open-channel conditions. On the other hand, since degradation phenomena were larger after the open-channel stress than after the off-state one, it is evident that strain-enhancement effects alone can not explain open-channel degradation, thus supporting the hypothesis that hot electrons contribute to open-channel stress effects. It must be considered that strain effects and consequent trap generation are expected to take place predominantly in the AlGaN barrier [58,62], so that, in this respect, degradation scenario E (accounting for barrier traps) appears to be more physical than degradation scenario D.

Always from Figure 2.24, it is noted that the vertical electric field is maximum under the gate (L=0), while it is smaller (and weakly sensitive to position) within the drain access region (L=0.6 μm and L=1.2 μm). This fact supports the conclusions (already drawn from the analysis of the g_m curve degradation) that off-state stress can impact the channel

transport properties and create traps mainly close to the gate contact. Besides strain-enhancement, gate-injected electrons can contribute to trap generation under off-state stress. Also this mechanism should lead to narrow trap-generation regions close to the gate contact, where the electric field is maximum. On the other hand, channel hot electrons created under power-state stress can, in principle, contribute to the degradation of channel transport parameters by generating defects and therefore increasing electron scattering. However, in our devices the decrease in the g_m peak after power-state stress is small, if compared with that observed after off-state stress. From this, we can conclude that degradation of transport parameters should be significant, in the devices considered here, especially under off-state stress.

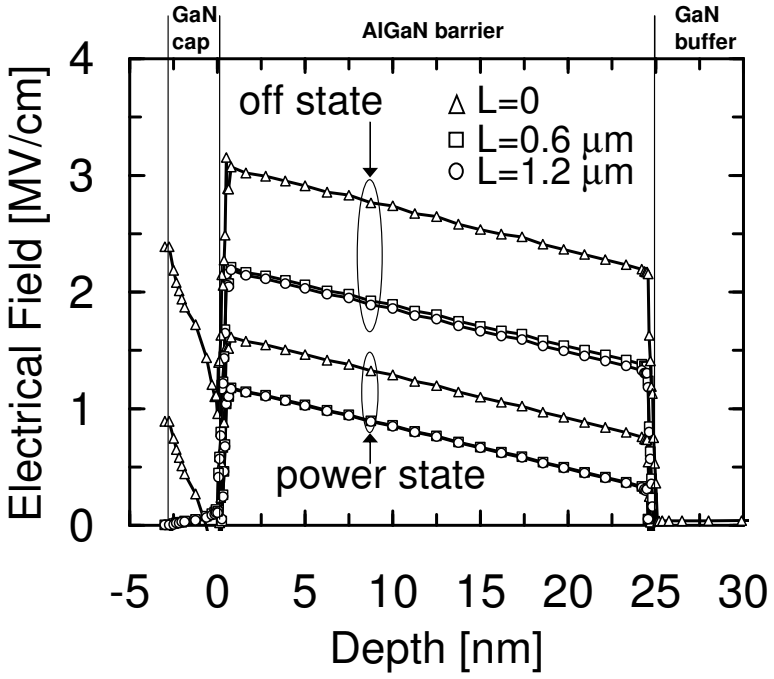

Figure 2.24: Vertical electric field at midgate (L=0) and two different positions within the drain access region (at 0.6 µm and 1.2 µm from the gate midpoint) for power-state (V_{GS}=0 V, V_{DS}=16 V) and off-state (V_{GS}=-6 V, V_{DS}=32 V) bias conditions.

Our results are not directly transferable to passivated devices. Surface passivation reduces the gate-drain electric field, thus impacting both pre-stress characteristics (gate lag and reverse gate current) and stress-induced trap generation. Degradation should therefore be less severe in passivated devices with respect to unpassivated ones for same stress bias and stress time [44-47]. Moreover, passivation and/or pre-passivation treatments can modify the physics of the device surface, by reducing the density of surface traps [63,64], by introducing positive charges [60], by passivating stress-generated traps or strengthening material bonds [51], or by inducing a discharge path for surface traps [65].

2.5 Conclusions

High-electric-field degradation phenomena were investigated in GaN-capped AlGaN-GaN HEMTs by comparing numerical device simulations with the results obtained from experiments. The latter consist of 150-hour DC stresses carried out under open-channel and off-state conditions.

Degradations effects observed after either stress type were: a drop in the DC drain current, the amplification of gate-lag effects, and a decrease in the reverse gate current. Moreover, experiments showed that the open-channel stress results in a transconductance drop that is concentrated at high gate-source voltages. On the other hand, off-state stress leads to a uniform decrease in transconductance for all gate-source voltages. Several degradation scenarios have been chosen amongst the larger number of applicable ones and they have been analyzed by means of 2-D numerical device simulations, with the aim of assessing their suitability to reproduce experimental data in the devices under study. Indications emerging from our analysis can be summarized as follows.

1) The stress-induced amplification of gate-lag effects can be ascribed to the generation of acceptor traps within the drain access region at the device surface and/or in the AlGaN barrier. The drop in DC drain current should rather be attributed to trap accumulation within the GaN buffer layer. The drop of reverse gate current can in principle be caused by acceptor-trap generation in either cap, barrier or buffer layers. As a result, the simultaneous generation of surface (and/or barrier) traps and of buffer traps can account for all of the degradation modes common to both stress types.

2) Under power-state stress, acceptor traps are implied to accumulate over a significant part of the gate-drain access region. Under off-state stress, trap generation should rather take place in a narrow slice close to the gate edge, but it should be accompanied by a significant degradation of the channel transport parameters.
3) Channel hot electrons are suggested to play a major role in determining electrical degradation under power-state stress. Strain enhancement and gate-injected electrons can instead contribute to degradation under off-state stress.

Chapter III:

Characterization and analysis of trap-related effects in GaN HEMTs

3.1 Introduction

Trap generation and the consequent amplification of RF current-collapse and power-slump phenomena are among the most deleterious effects originating from high-electric-field operation [58]. Trap characterization methods, such as deep-level transient spectroscopy (DLTS), and low-frequency transconductance (g_m) dispersion measurements are, therefore, key techniques for device-degradation monitoring and reliability assessment.

In this chapter, results are presented from a detailed trap-characterization study in GaN HEMTs and a consistent interpretation for the different traps detected is proposed, both in terms of localization within the device structure and of associated charge/discharge mechanism.

It is in particular shown that, under specific bias conditions, buffer traps can produce the same type of current-mode DLTS (IDLTS) signals that are generally attributed to surface traps. Clarifying this fact is crucial for both reliability testing and device optimization, as it can completely hinder a correct identification of degradation mechanisms.

3.2 Samples

Tested devices include short-gate HEMTs, FAT-HEMTs, as well as Schottky-diode test structures. All the devices have the same GaN/AlGaN/GaN epitaxial structure grown on semi-insulating SiC substrates by MOCVD.

The epitaxial multilayer consists (from bottom to top) of a 1 μm-thick undoped GaN buffer/channel layer, followed by a 30 nm-thick $Al_{0.22}Ga_{0.78}N$ barrier (20 nm of AlGaN doped with Si at the concentration of $5 \cdot 10^{17}$ cm^{-3}, sandwiched between two 5 nm AlGaN undoped spacers) and by a 3 nm-thick undoped GaN cap.

Ohmic contacts consist of a Ti/Al/Ni/Au structure annealed for 30 s at 900°C, while gate metallization is made of Mo/Au deposited by electronic evaporation.

A not-to-scale sketch of short-gate and FAT-HEMTs is shown in Figure 3.9. Short-gate HEMTs have a gate length (L_G) of 0.15 μm, and gate-source (L_{GS}) and gate-drain (L_{GD}) spacings of 0.7 and 2 μm, respectively.

FAT-HEMTs have L_G = 14 μm, L_{GS} = 0.7 μm, and L_{GD} = 2 μm. All structures are passivated with SiN (500 Å).

3.3 Trap characterization

3.3.1 Deep Level Transient Spectroscopy

Deep levels may behave as carrier traps or as generation-recombination centers if they are energetically located near to mid-gap. As traps they can capture the free carriers reducing their effective density.

It is clear that deep levels, although present in small quantities, can completely alter the electrical characteristics of a material. This allows them to be investigated using electrical measurements provided that the filling and emptying of the levels can be controlled.

Deep-Level Transient Spectroscopy is a basic, yet powerful high-frequency transient measurement technique which can be used to observe and quantify various properties of traps in semiconductors [76]. It is a capacitance thermal scanning method and can indicate the location and concentration of a trap, in addition to facilitating the measurement of activation energy, concentration profile and carrier capture cross-sections for each trap.

When a reverse bias is applied to a Schottky contact, the depletion width adjusts to its new position within the response time of the free electrons in the semiconductor lattice. However, after this immediate adjustment some of the full deep levels find themselves above the Fermi level where they slowly release their trapped charge at a characteristic emission rate:

$$e_{n,p} = \sigma_{n,p} \upsilon_{th,n,p} N_{C,V} \exp\left(-\frac{E_{a,n,p}}{k_B T}\right)$$

Where σ_n is the capture cross section for electrons; υ_{th} is the thermal velocity of electrons within the lattice; N_c is the density of states in the conduction band; and E_a is the activation energy of the traps.

For measurement purposes the transient may be produced in a controlled manner by applying a forward bias pulse to intentionally fill all the traps, and then returning to a quiescent reverse bias.

The filling pulses are repeatedly applied whilst the temperature is ramped at a constant rate. Because deep level emission is thermally activated, the time constant of the transient will change with temperature. The usual method of measuring the capacitance transient is the boxcar technique, the transient is measured conventionally between two sampling

points at times t_1 and t_2 (see Figure 3.1), the time period between the sampling points is referred to as the rate window.

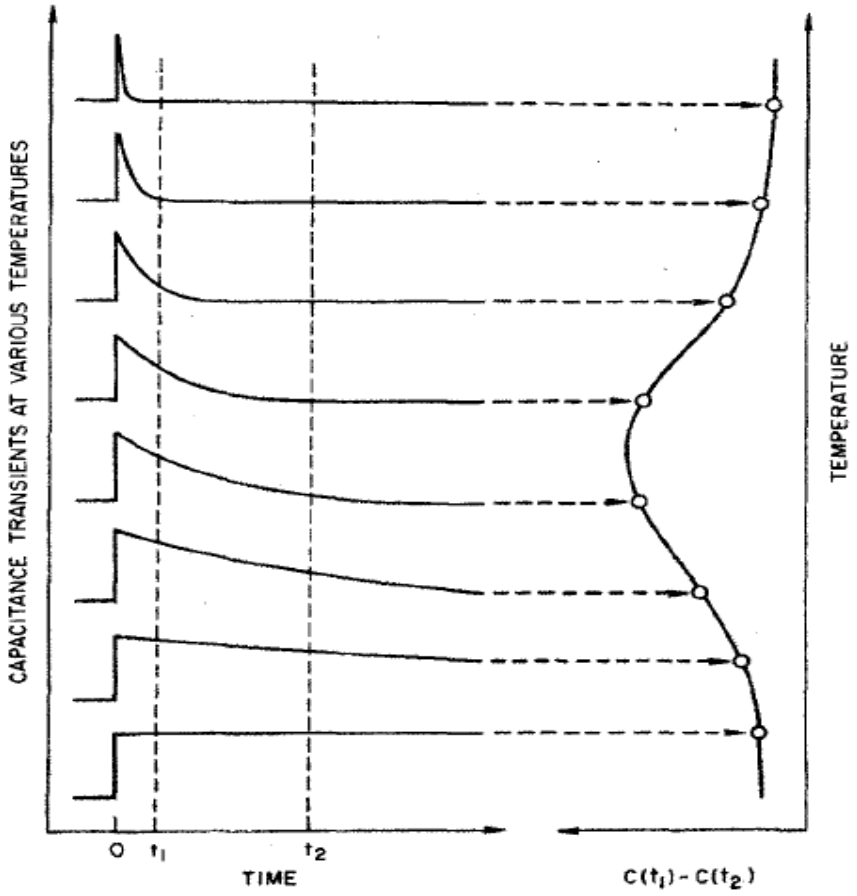

Figure 3.1: The temperature development of a capacitance transient observed through a rate window produces a DLTS peak [76].

As temperature increases, the shape of the transient changes in a manner characteristic of a particular trap. ΔC will be small at high temperature since all the traps are readily ionized, and small at low temperatures since few will be ionized. However, when the rate window matches the maximum thermal emission rate of the deep level, ΔC will be at a maximum. Hence an output of ΔC against temperature will show a DLTS peak that occurs at:

$$\frac{1}{e} = \tau_{\max} = \frac{t_1 - t_2}{\ln(t_1 / t_2)}$$

The temperature scan is repeated with a new rate window and so the peak occurs at another temperature. The activation energy is calculated from the temperature shift of the DLTS peak with different rate windows. The shift is used to construct an Arrhenius plot of the form:

$Ln[e_n/T^2]$ Vs 1000/T.

The latter is derived from the temperature dependence of the equation which describes e_n. Et is calculated from the slope of the Arrhenius plot.

Trap concentration is calculated from the height of ΔC, while the capture cross section is calculated from the y-axis intercept of the Arrhenius plot [77].

Current deep level transient spectroscopy (I-DLTS) is a powerful technique for deep-level characterization, which can directly be applied to modern, short-gate-length FETs, without requiring specific test structures (either diodes or FAT-FETs) with large gate areas, as instead needed by capacitance DLTS [78]. The I-DLTS technique consists of changing the equilibrium occupancy of the deep level states by successive voltage pulses applied to the gate. According to the bias applied between the source and the drain, electrons are moved and trapped by the different empty centres. When the voltage excitation is turned off, a transient current corresponding to the thermal emission of the traps is observed. The value of the transient current I(t) is measured at two sampling times t_1 and t_2 and the difference $I(t_1) - I(t_2)$ is continuously recorded as a function of temperature as it is used in place of ΔC in normal DLTS analysis [79].

3.3.2 DLTS results

Figure 3.2 shows the Arrhenius plot obtained from capacitance DLTS carried out on the FAT-HEMT devices. This plot points out the presence of three dominant trap levels. The shallowest is trap A with an energy level of 0.18 eV and a cross section of $4.5x10^{-19}$, trap B has an energy level of 0.5 eV and a cross section of $5x10^{-16}$. The deepest trap is trap C with an energy level of 0.76 eV and a cross section of $5x10^{-16}$.

On the other hand, Figure 3.3 represents the peaks obtained from I-DLTS applied on the FAT-HEMT devices. Both peaks obtained from V_{GS} steps (-3V to -1V) and (-2.5V to -4V) are shown, while V_{DS} = 1.5V in both cases. The peak of all traps A, B, and C is consistent with a hole-like peak [88].

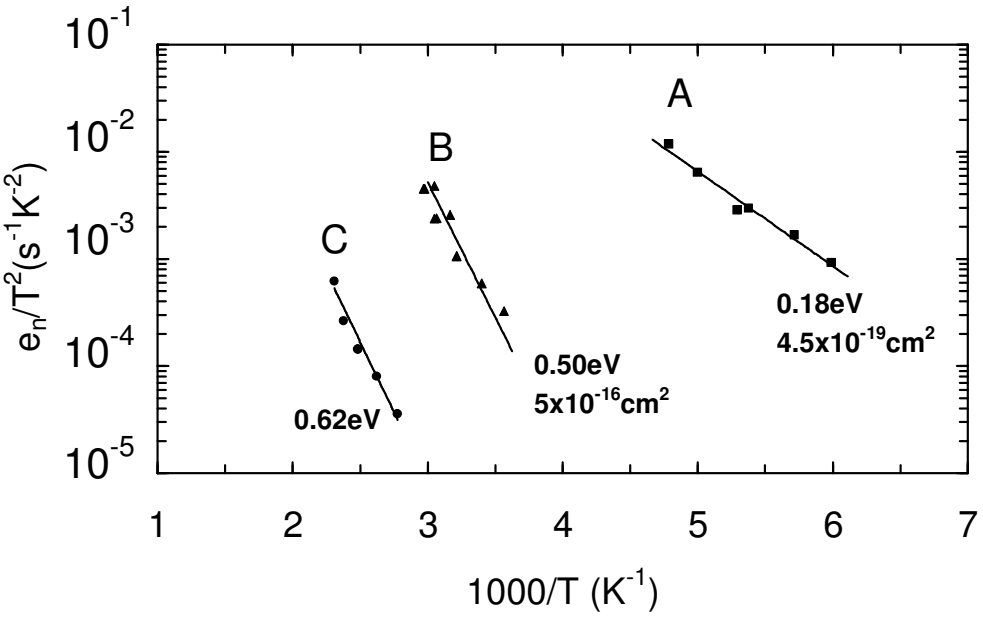

Figure 3.2: Arrhenius plot from DLTS measurements carried out on FAT-HEMTs.

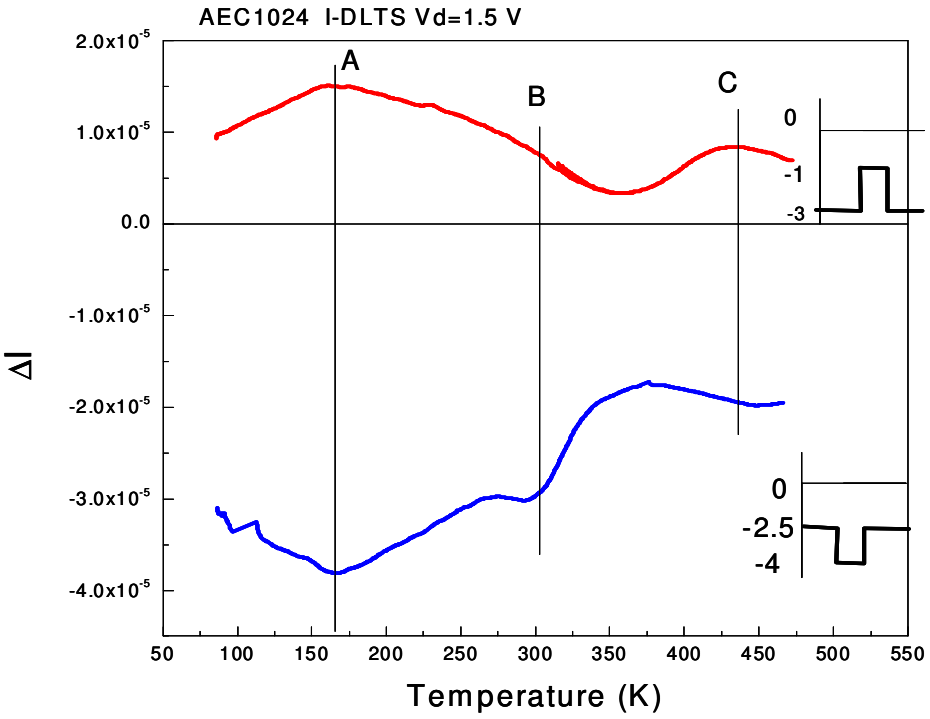

Figure 3.3: I-DLTS spectra from FAT-HEMTs, obtained by applying two V_{GS} pulses (-3V to -1V) and (-2.5V to -4V), with a V_{DS} of 1.5V

3.3.3 Gate lag measurements

Figure 3.4 shows the results from gate lag measurements carried out at different temperatures on the short gate HEMTs. V_{GS} is switched from -14V to -4V at a V_{DS} of 1.5V and the drain-current versus time waveform is measured at temperatures from 30°C to 70°C with a step of 10°C [56]. The experimental data have been fitted using three exponentials $i_D(t)=i_{D0}+ \Delta I_D[1-\exp(-t/\tau_{ON})]$ with three different constant times τ_{ON} (inset Figure 3.4). The three time constants calculated at different temperatures were plotted in an Arrhenius plot to extract the activation energy of the traps involved (see Figure 3.5). The three calculated values (0.25eV, 0.53eV, 0.6eV) are fairly in agreement with the values extracted by means of deep level transient spectroscopy (0.18eV, 0.56eV, 0.76eV) confirming a correct identification of the principal traps present in the devices.

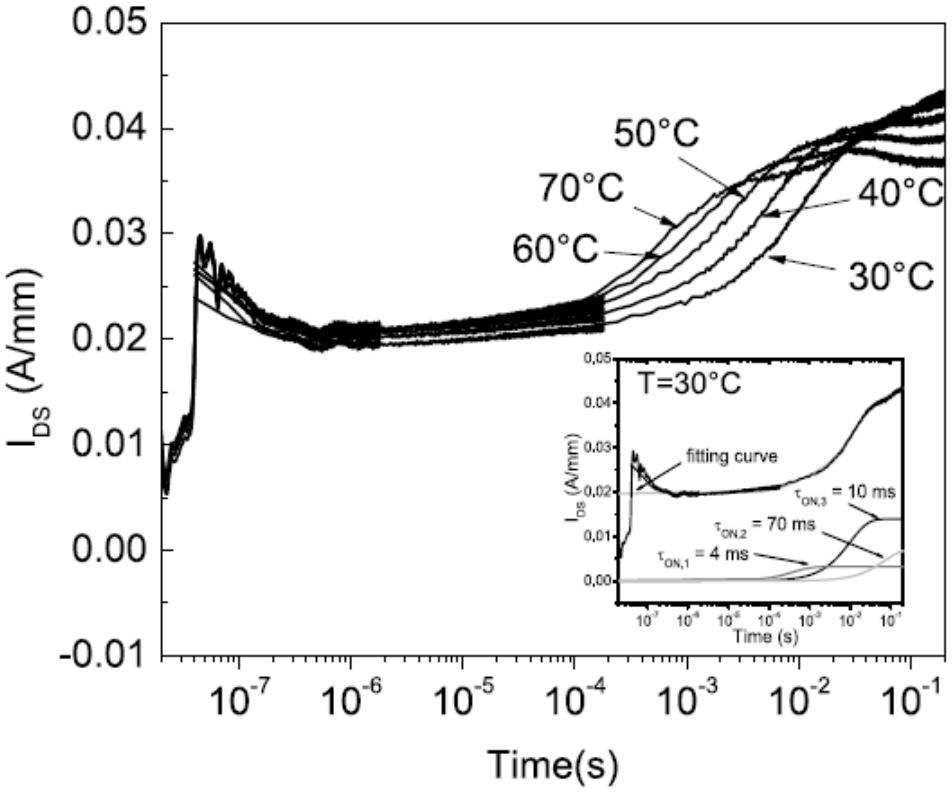

Figure 3.4: Experimental I_D versus time waveform in response to a V_{GS} step (-14 to -4 V) at V_{DS}=1.5V. In the inset the 3 exponentials used to fit the waveform at 30°C are reported with the corresponding time constant τ_{ON}.

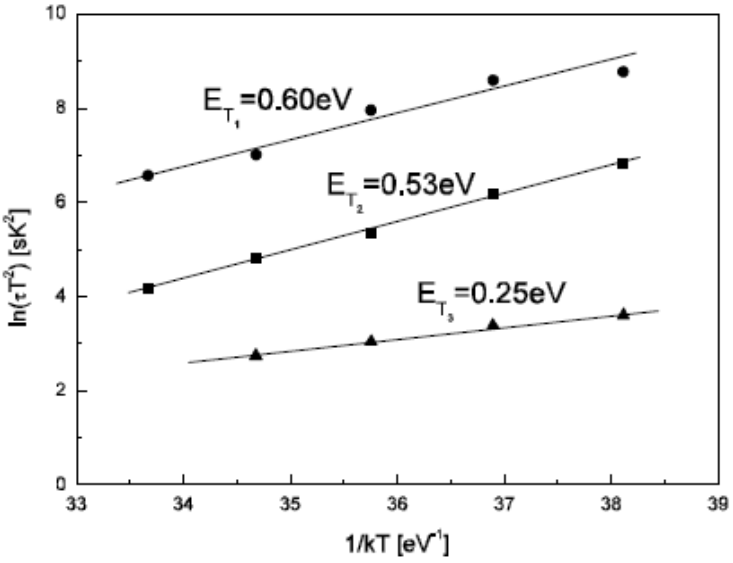

Figure 3.5: Arrhenius plot from temperature-dependent gate-lag measurements

3.3.4 Low-frequency transconductance dispersion

In HEMTs, where both the surface traps and traps under the gate contribute to dispersive effects, both positive and negative g_m dispersion can be observed in the same device. This kind of g_m dispersion has been observed in InAlAs/InGaAs MODFETs [80, 83] where the deep electron traps are located in the InAlAs layer [84].

In [80], it has been shown that in AlInAs/InGaAs/InP HEMTs both positive and negative g_m dispersions can be present depending on the bias point. The extent of negative dispersion was smaller at more positive gate voltages, a trend opposite to that reported in [81]. In [80], gate leakage current is assumed to supply the electrons needed to charge the surface states, and since this current is larger at more negative gate voltages, the g_m compression is larger when V_{GS} is closer to pinch-off. Positive g_m dispersion is attributed to electron traps in the InAlAs donor layer.

Negative g_m dispersion was observed in AlGaN/GaN HEMTs too by various research groups [85-87].

Figure 3.6 shows the normalized transconductance vs frequency measured from our short-gate HEMTs. This measurement was carried out at different temperatures from 30°C to

90°C with a step of 20°C, at V_{GS}=-3.5V and V_{DS}=1.5V. As can be seen this plot points out a negative g_m dispersion.

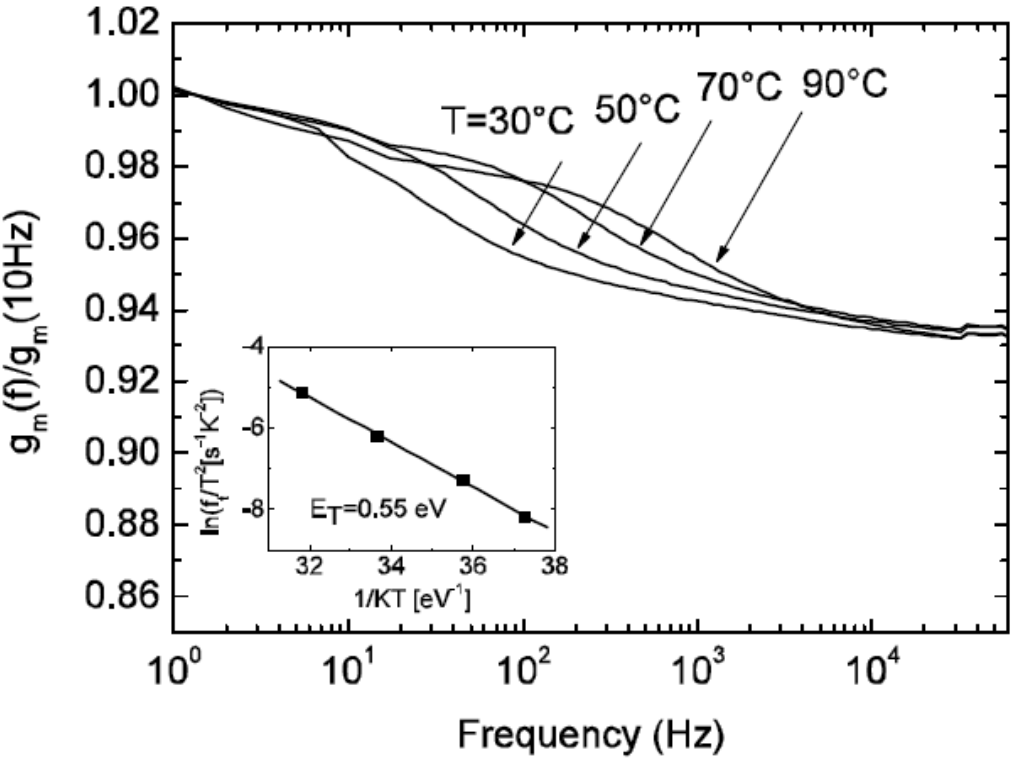

Figure 3.6: normalized transconductance vs frequency measured on short-gate HEMTs, at temperatures from 30°C to 90°C, at V_{GS}=-3.5Vand V_{DS}=1.5V.

It is apparent that the transition becomes more important and moves down in frequency with decreasing temperature. This temperature dependence is expected, since the process is governed by a relationship of the form which describes thermally activated reactions. The obtained Arrhenius plot can be seen in the inset of Figure 3.6, and the resulted activation energy (0.55eV) corresponds to trap B.

3.3.5 Discussion of the results

Table 3.1 summarizes the outcomes of all the experimental techniques adopted to characterize traps in our devices.

When DLTS is applied to diodes (that do not have the GaN cap layer), only traps B and C are detected, while trap A is not. This suggests that trap A is located in the cap layer or at the device surface, while traps B and C are located in the device bulk.

On the other hand, the remaining three techniques, that is current mode DLTS on FAT-HEMTs, low-frequency transconductance dispersion measurements and temperature-dependent gate-lag measurements (the latter two methods being applied to short-gate HEMTs), provide the same indications for the three traps.

Now, for trap A all techniques consistently indicate that it must be located in the cap or at the device surface. For traps B and C, on the contrary, we got inconsistent indications, with the comparison between DLTS on FAT-HEMTs and diodes pointing at bulk localization, while current mode DLTS, transconductance and gate lag methods suggesting surface localization.

TECHNIQUE	**Trap A**	**Trap B**	**Trap C**
DLTS on diodes	NOT detected	Detected	Detected
DLTS (FAT-HEMTs)	Detected	Detected	Detected
I-DLTS (FAT-HEMTs)	"Hole-like" peak	"Hole-like" peak	"Hole-like" peak
$g_m(f)$	N.A.	Negative dispersion	N.A.
Gate lag measurements	Increasing I_D transient	Increasing I_D transient	Increasing I_D transient
Location	Surface, cap	Inconsistent indications	Inconsistent indications

Table 3.1: the results from all trap characterization techniques

In order to investigate these contrasting evidences, the drain-current (I_D) transients were measured at room temperature, where trap B dominates (see Figure 3.2), by using different V_{GS} test pulses.

As a matter of fact, as long as V_{GS} is pulsed from 0 V to a negative value ($V_{GS,off}$) higher than the pinch-off voltage, the I_D transient is of the type that is generally attributed to surface traps (see Figure 3.7). However, when $V_{GS,off}$ approaches the pinch-off voltage (that is about 4.8 V in the devices under test), the shape of the I_D transient changes to that characteristic of a bulk trap (Figure 3.8).

In this regard, some questions arise: can the same trap be at the origin of the two opposite I_D transient behaviors? and why? and where must this trap be located?

To try to answer to these questions, two-dimensional numerical simulations were carried out by using a commercial code.

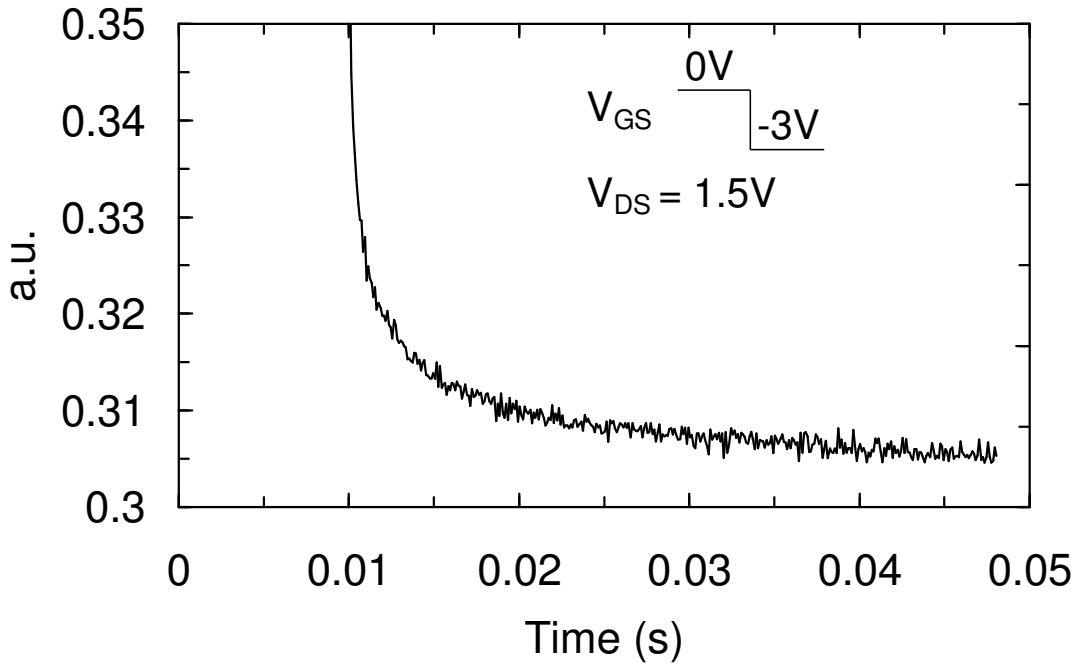

Figure 3.7: Experimental drain-current transients in the FAT-HEMTs for a V_{GS} pulse from 0V to -3V at a V_{DS} of 1.5V. Expanded plot of the slow transient governed by trap B.

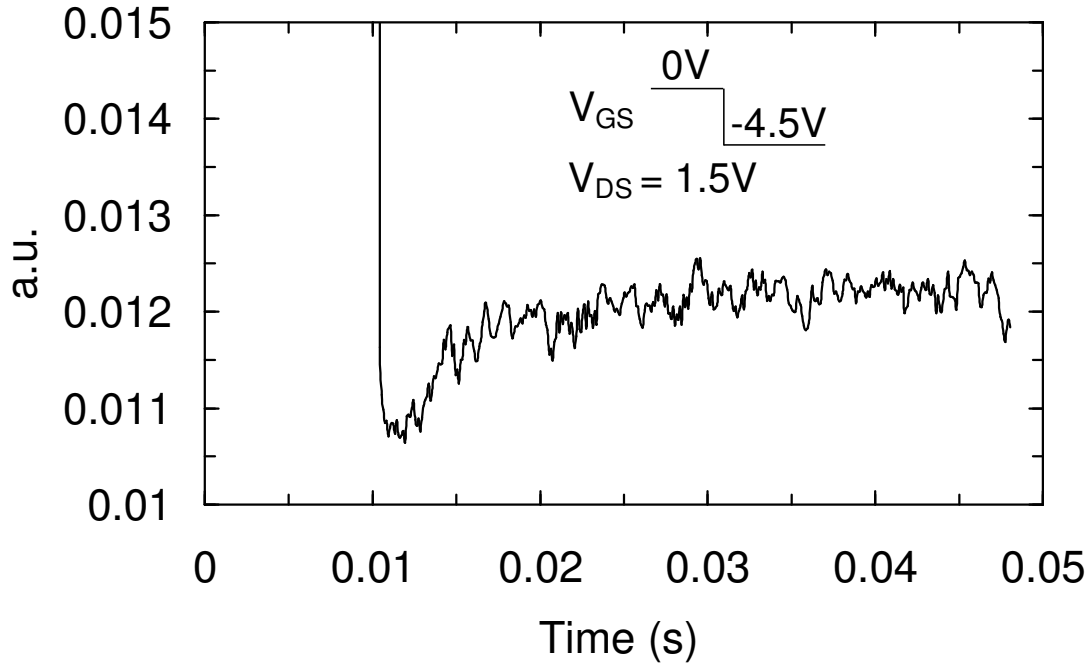

Figure 3.8: Experimental drain-current transients in a FAT-HEMTs for a V_{GS} pulse from 0V to -4.5V at a V_{DS} of 1.5V. Expanded plot of the slow transients governed by trap B.

3.4 Interpretation based on device simulations

3.4.1 Simulation approach

Two-dimensional, drift-diffusion simulations were been carried out with the code DESSIS8.0 (Synopsys Ltd.), including deep-level-trap dynamics. The gate current was modeled as the combination of thermoionic emission plus tunneling (field emission) injection across the gate barrier and drift-diffusion transport within the semiconductor layers. To account for polarization charges at the two AlGaN–GaN heterointerfaces, positive fixed charges with a sheet density $N_{pol}^{+} = 1x10^{13}$ cm^{-2} were placed at the bottom AlGaN–GaN interface (uniformly distributed over a 0.5 nm-thick region), while negative fixed charges having an equal sheet density $N_{pol}^{-} = 1x10^{13}$ cm^{-2} (and similarly distributed over a 0.5 nm region) were accounted for at the top GaN–AlGaN interface (Figure 3.9). The Schottky barrier height was set to 0.9 eV.

In agreement with the surface-donor theory explaining the channel 2DEG formation in GaN HEMTs [70], donor like traps (with a density N_{TD} = $8.5 \cdot 10^{12}$ cm^{-2}) have been assumed to be present at the device surface. Figure 3.9 shows a not to scale schematic cross-section of the simulated HEMT structure in this work .

Consistently with experimental results, trap A parameters (0.18 eV, $4.5 \cdot 10^{-19}$ cm^2) were assumed for energy and capture cross-sections of these surface donors.

Acceptor like traps were instead placed within the GaN buffer layer (with a density N_{BA} = $1 \cdot 10^{17}$ cm^{-3}). Assumed trap parameters were in this case those characterizing trap B (0.5 eV, $5 \cdot 10^{-16}$ cm^2) for energy and capture cross-section.

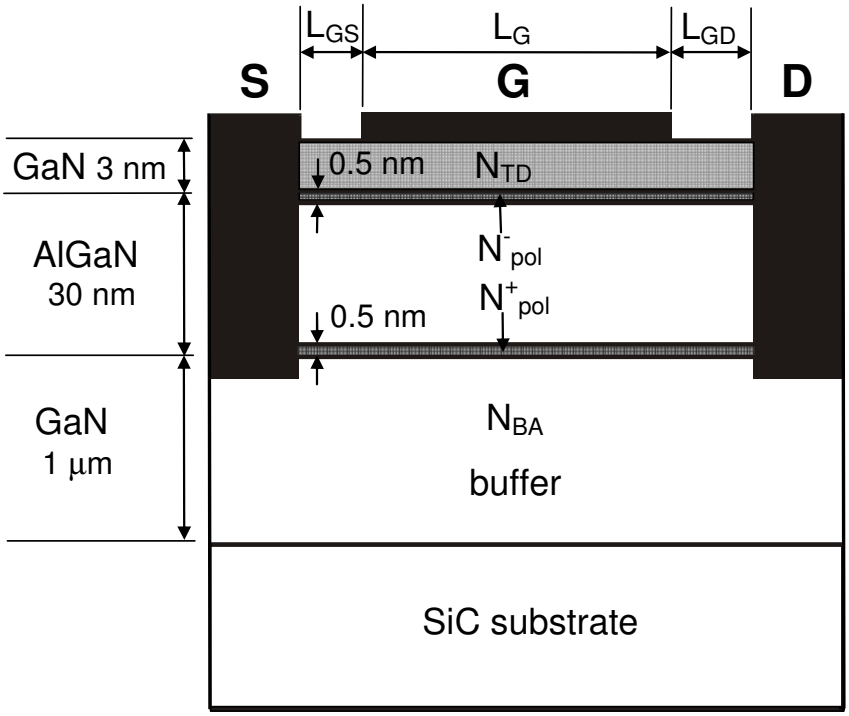

Figure 3.9: Schematic cross-section of HEMT structures adopted for this work (not to scale).

3.4.2 Simlation results

The same changing behavior observed experimentally in FAT-HEMTs and shown in Figures 3.7 and 3.8, can actually be reproduced by simulations provided that trap B and/or C is placed in the buffer. This is demonstrated by Figure 3.10 and 3.11, showing simulated I_D transients (at T = 300 K) in response to V_{GS} pulses similar to those adopted for measurements.

The type of the I_D transient actually changes from "surface- trap"-like (see Figure 3.10) to "buffer-trap"-like (see Figure 3.11), as $V_{GS,off}$ is decreased to a value close to the pinch-off voltage. However, inspection of internal electron and trapped-charge distributions points out that buffer trap modulation is involved in both cases (whereas the contribution of surface-trap modulation is negligible).

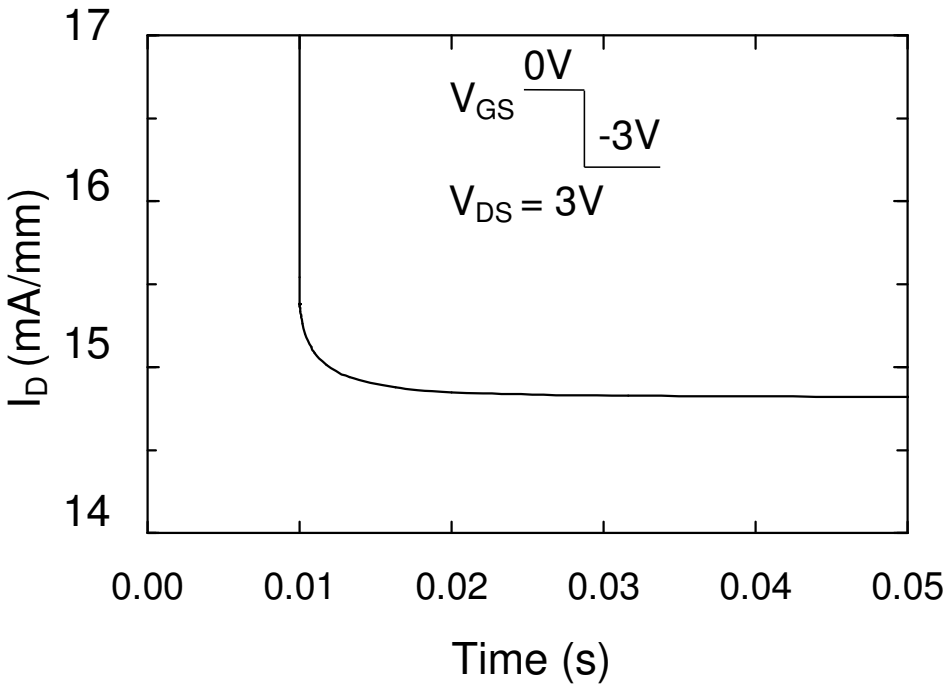

Figure 3.10: Simulated drain-current transients in a FAT-HEMTs for a V_{GS} pulse from 0V to -3V at a V_{DS} of 1.5V. Expanded plot of the slow transient controlled by buffer traps.

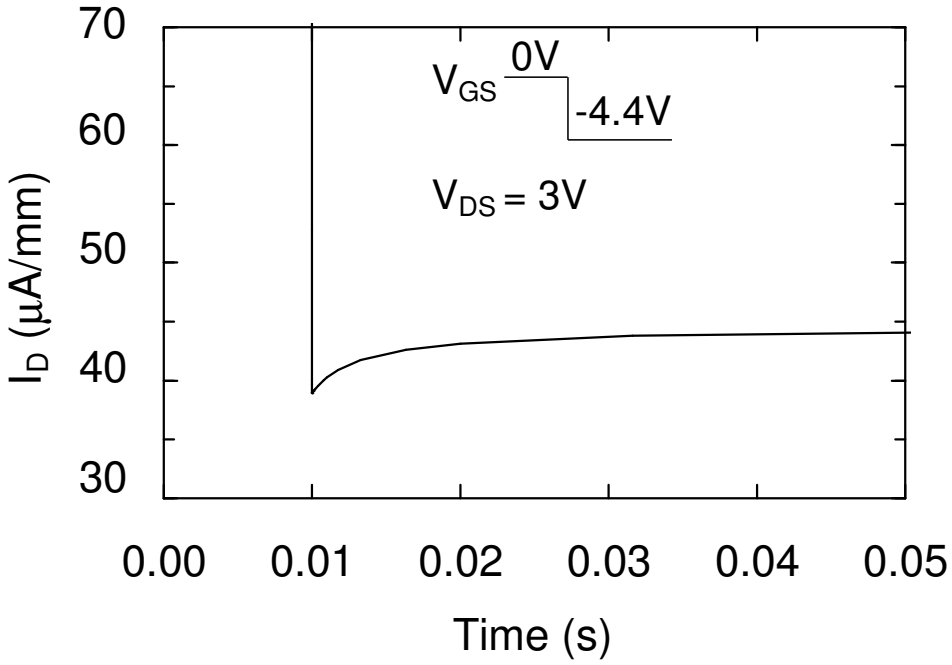

Figure 3.11: Simulated drain-current transients in a FAT-HEMTs for a V_{GS} pulse from 0V to -4.4V at a V_{DS} of 1.5V. Expanded plot of the slow transient controlled by buffer traps.

The underlying physics can be understood with the aid of Figures 3.12–3.15, showing the time evolution of the electron and trapped-charge distributions during the I_D transients shown in Figure 3.10 and 3.11, respectively.

As can be noted from Figure 3.12, for $V_{GS,off}$ values sufficiently higher than the pinch-off voltage, the (free) electron density decreases moderately, immediately after the application of the V_{GS} turn-off step, in the region of the buffer closer to the AlGaN–GaN interface. It instead increases in the deeper buffer region. Afterwards, the electron density decreases slowly with time (see Figure 3.12), as a consequence of trapping by buffer traps (see Figure 3.13). As a matter of fact, when V_{GS} is switched to a voltage value higher than the pinch-off voltage, the channel is not completely depleted, while electrons are temporarily injected deep into the buffer, giving rise to electron capture by buffer traps. This explains why I_D decreases during the slow transient governed by trap B observed both experimentally and in simulations (see Figures 3.8 and 3.10).

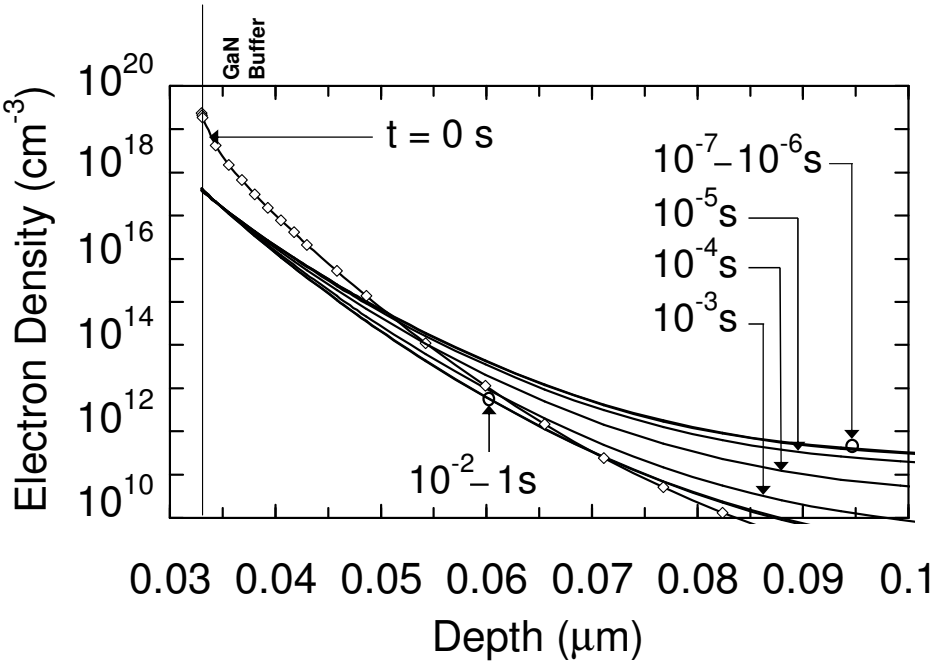

Figure 3.12: Electron-density distribution through the buffer layer at different times during the turn-off transient shown in Figure 3.10.

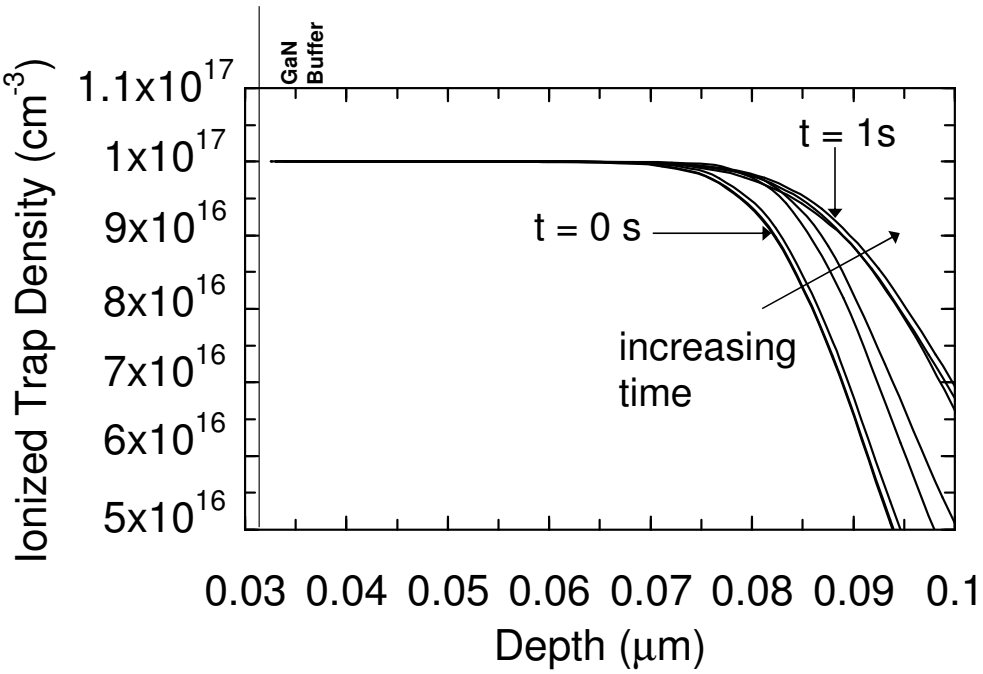

Figure 3.13: Ionized-trap-density distribution through the buffer layer at different times during the turn-off transient shown in Figure 3.10.

On the other hand, for $V_{GS,off}$ values close to the pinch-off voltage, the electron density drops drastically in the region of the buffer closer to the AlGaN-GaN interface when the V_{GS} turn-off step is applied (see Figure 3.14). As a result, the trapped-charge density decreases with time (see Figure 3.15); in other words, electron emission from buffer traps is the dominant effect in this case. This explains the increasing I_D transient resulted from both measurement and simulations and shown in Figures 3.9 and 3.11.

Trap C (which is not included for simplicity in the simulations) behaves similarly to trap B and is therefore inferred to be a buffer trap, too.

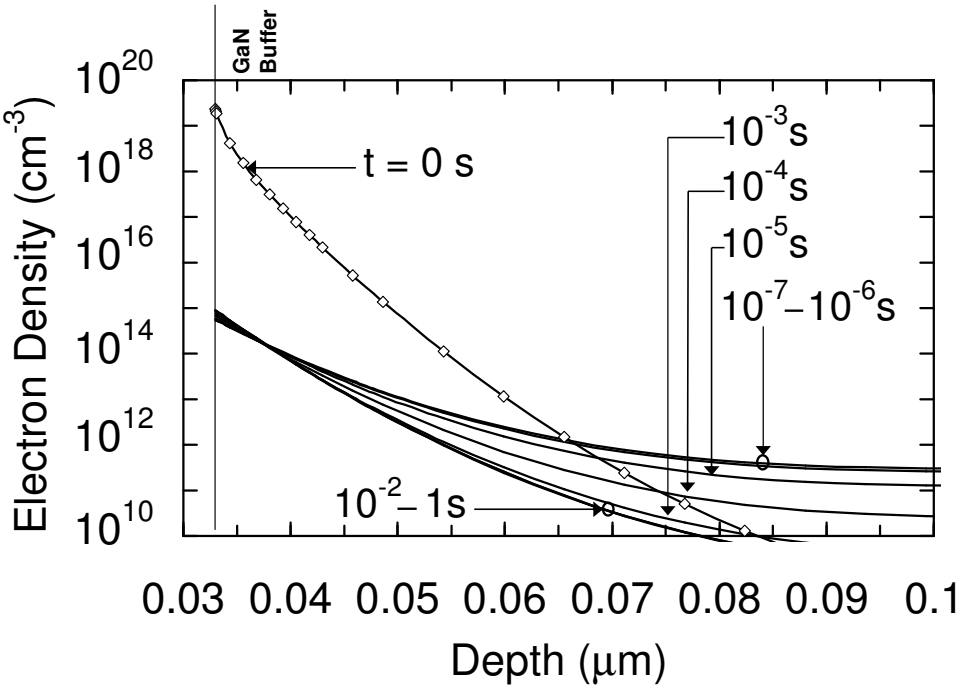

Figure 3.14: Electron-density distribution through the buffer layer at different times during the turn-off transient shown in Figure 3.11.

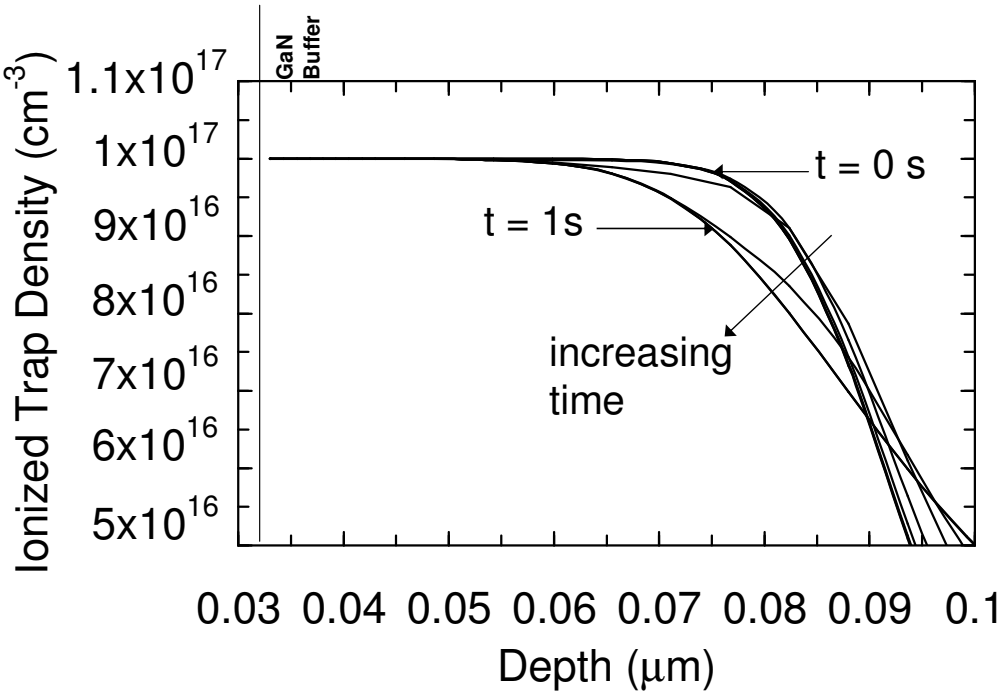

Figure 3.15: Ionized-trap-density distribution through the buffer layer at different times during the turn-off transient shown in Figure 3.11.

3.5 Conclusions

In conclusion, traps have been identified in AlGaN–GaN HEMTs by means of different characterization techniques and the associated physical behavior has been interpreted with the aid of numerical device simulations. Unless V_{GS} is pulsed to a value close to the pinch-off voltage, buffer traps in HEMT structures have been shown to produce ‘‘false’’ surface-trap signals and the underlying physics has been explained. Clarifying this aspect is important for both reliability testing and device optimization, as it can lead to erroneous identification of the degradation mechanism, thus resulting in wrong correction actions on the technological process.

Chapter IV:

Mechanisms of RF Current Collapse in GaN HEMTs

4.1 Introduction

Current-collapse effects represent one of the major pitfalls of the GaN-HEMT, impeding the combination of high two-dimensional electron gas (2DEG) density, high saturation velocity and high critical electric field characterizing the AlGaN-GaN material system to translate into the expected, extraordinary HEMT RF power performance.

Current-collapse effects can arise during either DC or RF operation. DC current collapse, i.e. the drop in the drain current (I_D) following the application of drain-source-voltage (V_{DS}) DC sweeps [72], has generally been attributed to hot-electron trapping into deep levels within the barrier [75] and/or buffer [18,24] epilayers. Accordingly, it has become less and less important as the refinement of growth techniques progressed.

RF current collapse, i.e. the I_D compression during the ON phase of the RF cycle [72], has instead generally been put into relation with the action of surface traps. As a matter of fact, it has been reduced to tolerable levels by means of SiN surface passivation [33]. Other technological counteractions that have proved able to minimize it, either in addition or as an alternative to surface passivation, include: “surface-charge-control” cap layers [60], field plates [89], pre-passivation plasma treatments [51], deeply-recessed gate structures [90]. RF current collapse reduces the transistor RF output power with respect to the nominal value computable from the DC output characteristics. Only its minimization opened the way to the RF power performance records reported recently [91, 92].

Demonstrating a solid reliability is nowadays the final step before AlGaN-GaN HEMTs can massively be adopted in RF power applications. The appearance and/or amplification of RF current collapse is unfortunately one of the effects that more commonly take place during both DC [51] and RF [49, 93] electrical stresses, even in devices that show immunity from this detrimental phenomenon before stress. For this reason, gaining physical insight and trying to make the picture of the different, possible physical mechanisms that can lead to RF current collapse as complete as possible is still a worthwhile effort.

To this aim, the different mechanisms underlying RF current collapse in passivated AlGaN-GaN HEMTs are investigated in this work by means of measurements and two-dimensional numerical device simulations. Energy, capture cross sections and location of deep levels introduced in the simulated device are taken from the results of DLTS

measurements carried out on the devices under study, which have the same structure of the devices reported in chapter 3. In this regard, Table 4.1 summarizes the results obtained from DLTS measurements. Specific aspects addressed by this chapter improving the comprehension of mechanisms underlying RF current collapse include: 1) the relationship between surface potential and surface-trap energy, 2) the role played by both surface and buffer traps in RF current collapse, 3) the impact of surface passivation.

	Activation energy [eV]	**Cross section [cm^2]**	**Location**
Trap A	0.18	4.5×10^{-19}	Cap and/or surface
Trap B	0.5	5×10^{-16}	Buffer
Trap C	0.76	2×10^{-15}	Buffer

Table 4.1: Activation energies, apparent capture cross section, and location of deep-level traps detected by DLTS

4.2 Samples

Devices adopted for this work are AlGaN-GaN HEMTs grown on semi-insulating SiC substrates by MOCVD. The epitaxial multilayer consists (from bottom to top) of a 1-μm-thick undoped GaN buffer/channel layer, followed a 30-nm-thick $Al_{0.22}Ga_{0.78}N$ barrier (20 nm of AlGaN doped with Si at the concentration of 5×10^{17} cm^{-3}, sandwiched between two 5-nm AlGaN undoped spacers) and by a 3-nm-thick undoped GaN cap. Ohmic contacts consist of a Ti/Al/Ni/Au structure annealed for 30 s at 900 °C, while gate metallization is made of Mo/Au deposited by electronic evaporation. The devices are passivated with SiN (500 Å). The gate length (L_G) is 1 μm, whereas the gate-source (L_{GS}) and gate-drain (L_{GD}) spacings are 0.7 μm and 2 μm, respectively. The gate width is 100 μm. A not-to-scale sketch of the device cross section is shown in Figure 4.1. DC characterization yielded a saturation drain current (I_{DSS}) of 0.65±0.05 A/mm (at V_{GS}=0 V and V_{DS}=10 V), a peak extrinsic transconductance of 170±4 mS/mm at V_{DS}=10 V, and a threshold voltage (V_{TH}) of -4.8±0.2 V.

4.3 Device simulation approach

Two-dimensional numerical device simulations were carried out with the aim of correlating the observed experimental characteristics with the effects of deep-level traps put into evidence by DLTS measurements (see Table 4.1). The commercial code Dessis 8.0 (Synopsys Int. Ltd) was used. The drift-diffusion model was adopted as transport model. The Schottky barrier height was set to 0.9 eV. Low-field electron mobility and electron saturation velocity in the GaN channel were set to 1070 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (in agreement with Hall measurements) and 1×10^7 cm/s, respectively. GaN and $Al_{0.22}Ga_{0.78}N$ bandgaps were set to 3.42 eV and 3.84 eV, respectively, while the AlGaN-GaN conduction-band discontinuity was set to 0.29 eV [6].

The gate current (I_G) was modeled as the combination of thermoionic emission plus field-emission injection across the gate barrier. Other tunneling mechanisms, beside field-emission injection, can actually contribute to I_G [66,94]. However, assessing the exact physical mechanism underlying gate current goes beyond the scope of the present work. However, any model incorporating a mechanism of electric-field-dependent injection would produce qualitatively-equivalent results obtained from this work.

Deep-level traps were accounted for by including, for each distinct trap level, one trap-balance equation, describing, within the framework of the Shockley-Read-Hall theory, the dynamics of trap occupation without any quasi-static approximation.

Figure 4.1 represents the simulated cross section, except for the SiC substrate which was not included into the simulation domain.

To account for spontaneous and piezoelectric polarization charges at the two AlGaN-GaN heterointerfaces, positive fixed charges with a sheet density $N^+_{pol}=9.5\times10^{12}$ cm^{-2} were placed at the bottom AlGaN-GaN interface (uniformly distributed over a 0.5-nm thick region), while negative fixed charges having an equal sheet density $N^-_{pol}=9.5\times10^{12}$ cm^{-2} (and similarly distributed over a 0.5-nm region) were accounted for at the top GaN-AlGaN interface (see Figure 4.1) [6].

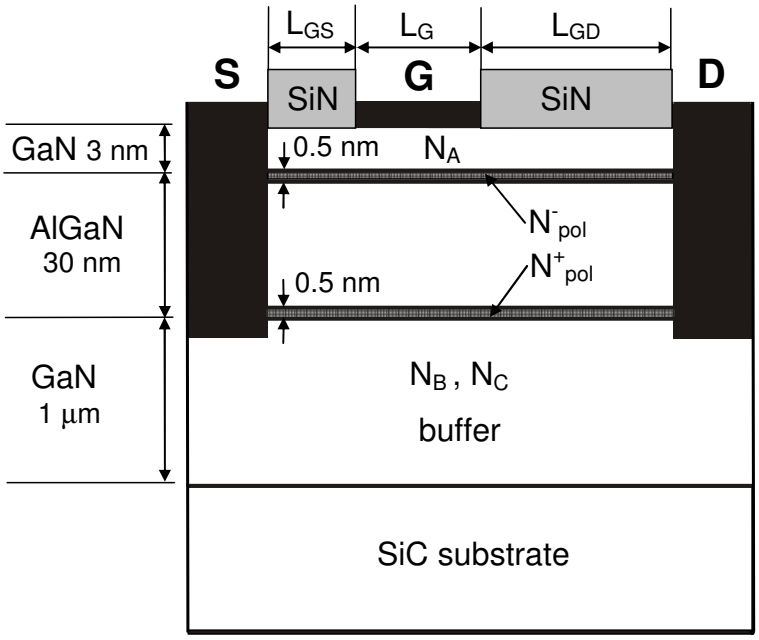

Figure 4.1: Sketch of the device cross section (not to scale). Symbols are defined in the text.

In agreement with the "surface-donor" theory explaining the channel 2DEG formation in GaN HEMTs [70], donor-like traps were assumed to be present at the device surface. Donor traps were uniformly distributed throughout the GaN cap (see Figure 4.1). In actual devices, both surface traps at the exposed GaN surface and volume distributions of near-surface traps [66, 71] may be present. The assumed donor-trap distribution within the GaN cap must therefore be regarded as a simplified way to include the cumulative effect of surface and near-surface defects. Activation energy and apparent cross section achieved by DLTS for trap A (see Table 4.1) were assumed for the energy depth with respect to the conduction band edge (E_C) and the electron and hole capture cross sections of these surface donors.

Acceptor-like traps having energy depths (from E_C) and capture cross sections of traps B and C (see Table 4.1) were instead placed within the GaN buffer. A uniform volume density of 5×10^{16} cm^{-3} was assumed for each of traps B and C (i.e., $N_B=N_C=5\times10^{16}$ cm^{-3}). Buffer traps B and C were assumed to be acceptor-like in order to suppress buffer conductivity effects otherwise predicted by simulations.

The actual picture can, of course, be more complicated and may include acceptor-like traps deeper (in energy) than traps B and C suppressing buffer leakage but not contributing to DLTS signal. If this is the case, either or both traps B and C could actually be donor-like traps. In any case, their dynamic effects are related with the variations of ionized charge rather than with its sign. For this reason, conclusions drawn in the following about dynamic effects related with buffer traps B and C are not strictly dependent on the assumed acceptor-like nature for these traps.

The density per unit area of surface donor traps (N_A) was finally adjusted so that simulations could fit the experimental V_{TH}. Surface donor traps contribute, in fact, along with the intentional shallow-donor doping in the barrier, to the formation of the 2DEG at the barrier-to-buffer heterostructure [70]. The value for N_A yielding a good V_{TH} agreement was $N_A=7.5\times10^{12}$ cm^{-2}.

4.4 Variation of surface-potential barrier with trap density

Figure 4.2 shows the device band diagram along a vertical cut under the ungated surface obtained at equilibrium ($V_{GS}=V_{DS}=0$ V) for different N_A (density per unit area of surface donor traps) values. As can be noted, for $N_A\leq7.5\times10^{12}$ cm^{-2} the Fermi level (E_F) is not pinned at the donor-trap level (E_C-0.18 eV). For $N_A=7.5\times10^{12}$ cm^{-2}, in particular, (E_C-E_F) is ≈0.75 eV (well above the energy depth of surface donors) and ≈1.25 eV at the GaN and the AlGaN surface, respectively.

For the adopted N_A value of 7.5×10^{12} cm^{-2}, surface trap energy and surface potential barrier are thus decoupled parameters, i.e. the device surface can be characterized by relatively-shallow surface traps and a large surface potential barrier at the same time.

This may reconcile works showing RF current collapse or other dispersion effects associated with surface traps relatively shallow in energy (0.1-0.7 eV) [58, 95-98], with works estimating the surface potential barrier to be in the 1-2 eV range [2, 70, 38].

Of course, (E_C-E_F) drops at increasing N_A and finally becomes controlled by surface donors for $N_A \geq 9\times10^{12}$ cm^{-2}, see Figure 4.2. Therefore, large surface potential barriers can coexist with shallow surface traps inducing RF current-collapse effects characterized by short time constants.

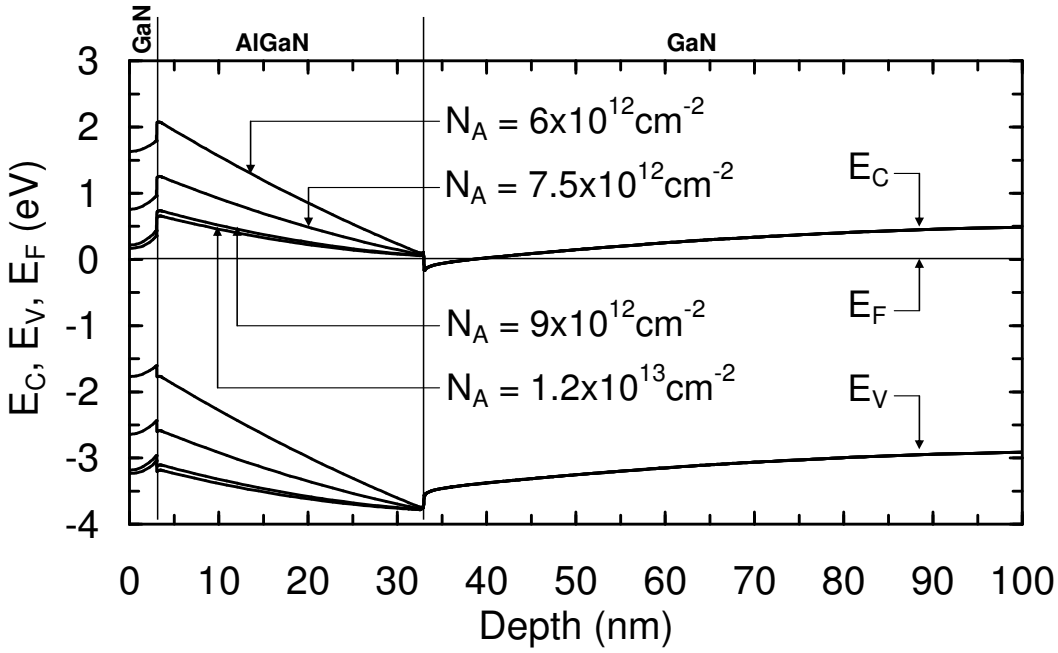

Figure 4.2: Conduction-band minimum (E_C), valence-band maximum (E_V) and Fermi level (E_F) along a vertical cut under the ungated surface obtained at equilibrium (V_{GS}=V_{DS}=0 V) for different densities of the donor-like traps in the cap layer (N_A).

4.5 The effect of passivation on current collapse

4.5.1 Experimental measurement

Figure 4.3 shows the typical I_D versus time (t) waveform measured from the devices under study in response to the application of a gate-source-voltage (V_{GS}) pulse from sub-threshold to open-channel conditions at high V_{DS}. V_{GS} was in particular pulsed from -7 V to 0 V at a drain voltage (V_{DD}) of 10 V (applied through a 50-Ω resistor). The measurement setup consisted of an Agilent HP8110A pulse generator for gate pulsing and a Tektronix TDS680 oscilloscope (1GHz band, 5 GS/s) for drain-voltage recording. Pulsed measurements like that shown in Figure 4.3 are the simplest way to assess whether (and to what extent) the devices at hand suffer from RF current collapse. The magnitude of RF current collapse can actually be quantified as the ratio $\Delta_{CC}=(I_{DC}-I_{Dpulse})/I_{DC}$, where I_{Dpulse} is

the drain current measured at the end of the V_{GS} rise time (i.e., at $t=5\times10^{-8}$ s in Figure 4.3) and I_{DC} is static drain current. The smaller I_{Dpulse} with respect to I_{DC}, the larger the RF current collapse. In the case of Figure 4.3, I_{Dpulse} is larger than I_{DC}. RF current collapse is therefore absent in these passivated devices at the adopted bias.

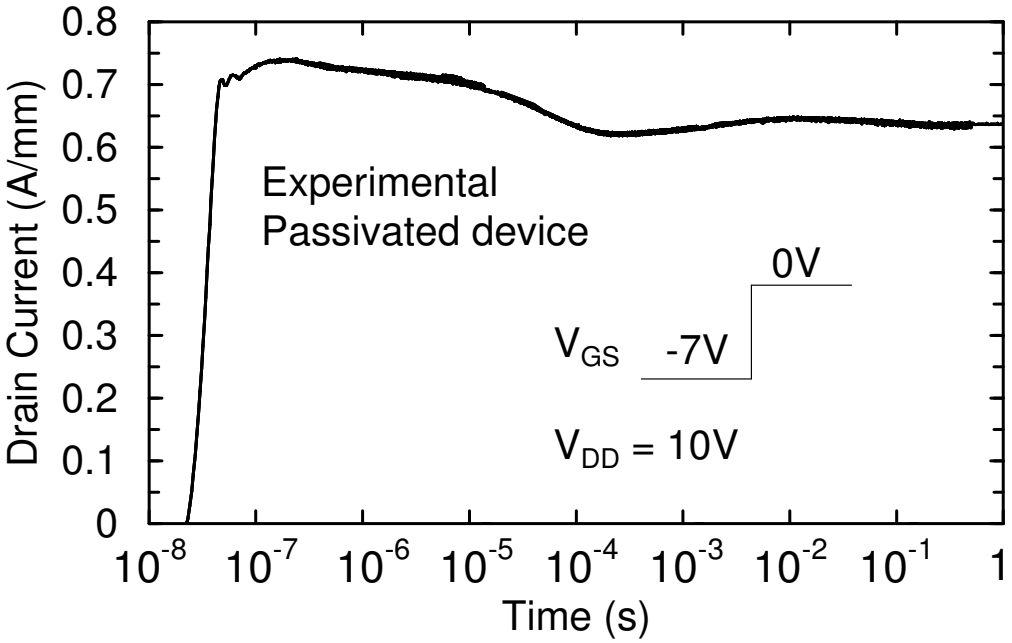

Figure 4.3: Experimental drain current versus time waveform in response to a gate-source-voltage (V_{GS}) step from -7 V to 0 V at a drain voltage (V_{DD}) of 10 V (applied through a 50-Ω resistor).

To try to understand the impact of passivation, two-dimensional device simulations are adopted.

4.5.2 Simulation study

Figure 4.4 shows simulated I_D vs time waveforms in response to a turn-on V_{GS} step from -7 V to 0 V at V_{DS}=10 V with and without surface SiN passivation. As can be noted, the device with SiN passivation shows, in qualitative agreement with experiments reported in Figure 4.3, negligible current-collapse effects. The initial decreasing transient that is present in the measured pulse response (see Figure 4.3) is not present in the simulated

transient, resulting in a final DC I_D value larger than the measured value. This can be ascribed to having neglected self-heating effects within simulations.

If the SiN passivation layer is removed from the simulation domain, the pulse response changes radically, as significant RF current collapse effects ($\Delta_{CC} \approx 64\%$) emerge characterized by a time constant of about 10^{-3} s.

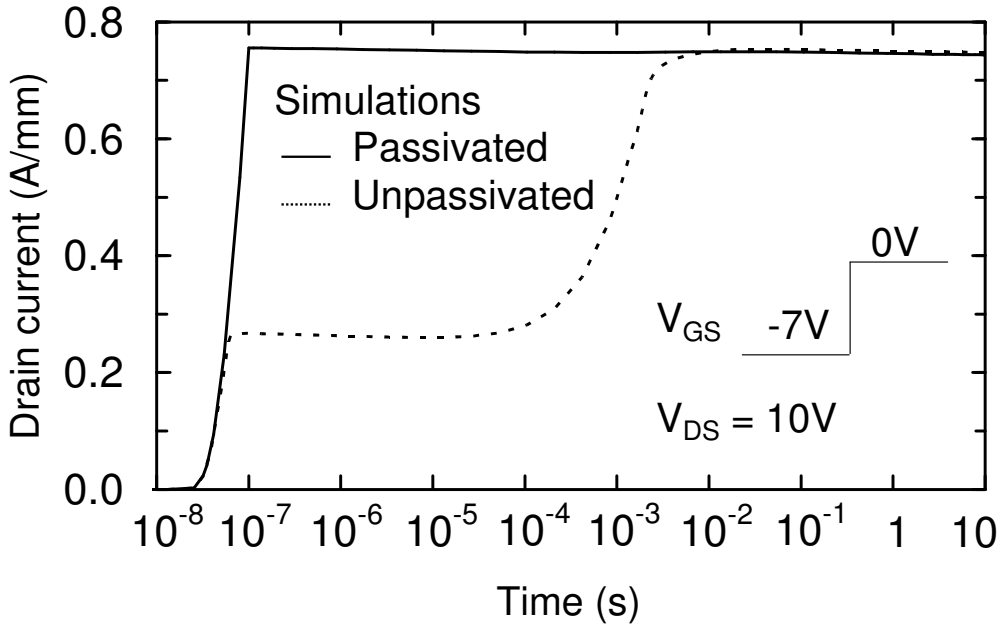

Figure 4.4: Simulated drain-current versus time waveforms in response to a gate-source-voltage (V_{GS}) step from -7 V to 0 V at a drain-source voltage (V_{DS}) of 10 V with and without surface SiN passivation.

The physical mechanism that simulations suggest to be at the origin of the large RF current collapse shown by the unpassivated device in Figure 4.4 agrees well with the concept of ”virtual gate” formed by surface donors [36]. Insight can be gained with the aid of Figure 4.5 a), showing the ionized-trap density (N_A^+) associated with donor traps A along the cap in the unpassivated device at different times during the turn-on transient shown in Figure 4.4. When the device is biased at a negative and large-in-modulus V_{GS} (as for $t \leq 0$ s in Figures 4.4 and 4.5), significant gate electron injection takes place, concentrated, due to the positive V_{DS} applied, at the drain-end of the gate contact. Part of injected electrons flows to the drain contact through the GaN cap. As a consequence, electron trapping into surface donors takes place, reducing N_A^+ [see curve for t=0 in Figure 4.5 a)].

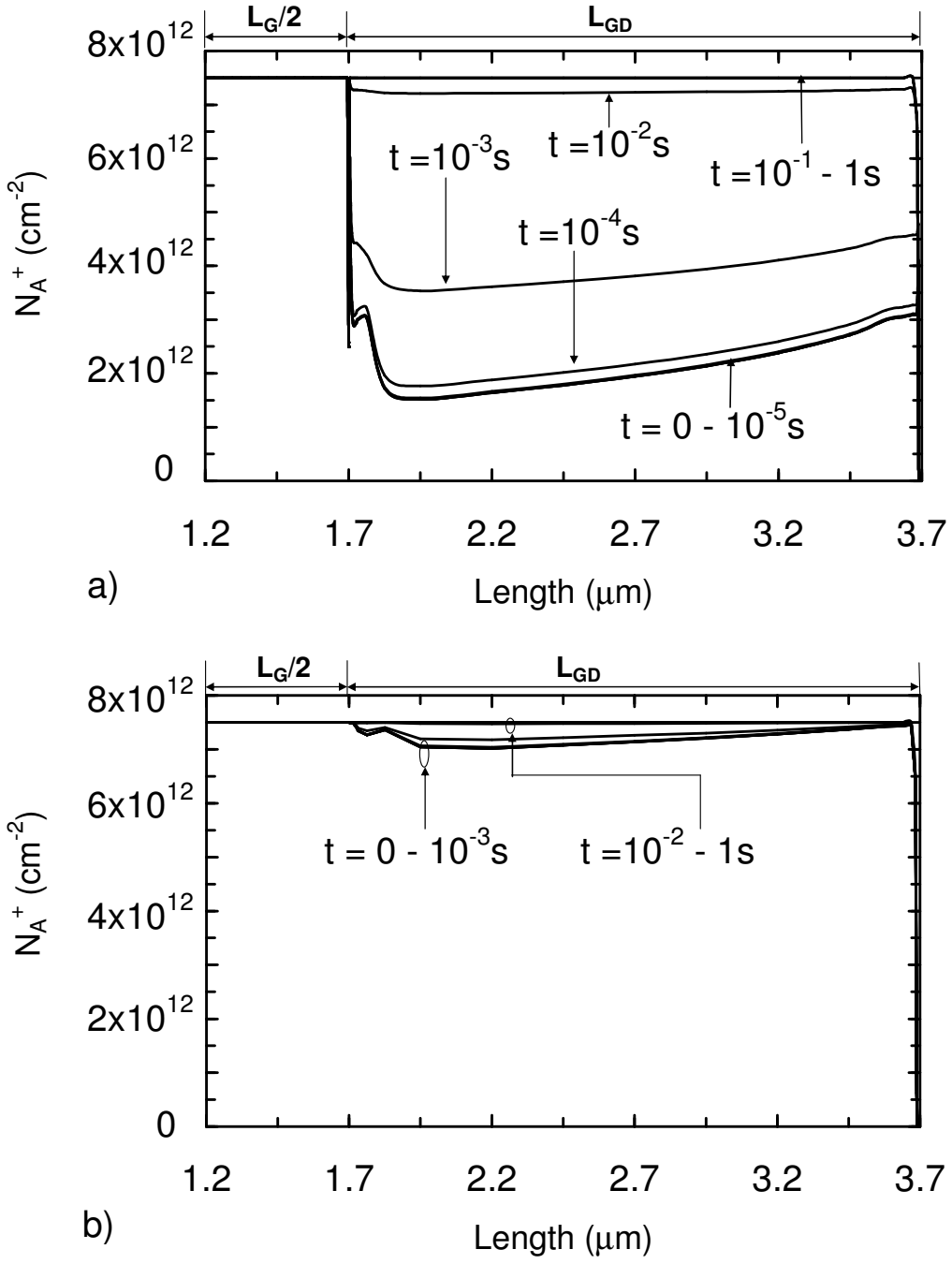

Figure 4.5: Ionized-trap density (N_A^+) associated with donor traps A along the cap for the unpassivated device [Figure 4.5 a)] and for the passivated one [Figure 4.5 b)], at different times (t) during the turn-on transient shown in Figure 4.4. Only the drain side of the device is shown. The drain-end of the gate is at 1.7 μm, while the gate-drain access region spans from 1.7 to 3.7 μm.

When V_{GS} =0 V (under steady-state conditions), electron injection from the gate is instead small, thus suppressing electron capture. Correspondingly, donor traps are completely ionized, i.e. $N_A^+ \approx N_A = 7.5\times10^{12}$ cm^{-2} [see curves for t=10^{-1}-1 s in Figure 4.5 a)].

As V_{GS} is stepped from a negative value to 0 V, N_A^+ initially does not change as traps respond to bias changes with a finite time constant [see curves for t=0-10^{-5} s in Figure 4.5(a)]. For t>10^{-5} s, then, electrons start being emitted by traps and N_A^+ increases. For t>10^{-2} s, all trapped electrons have been emitted, so that $N_A^+ \approx N_A$. Any change in N_A^+ reflects into a corresponding change in the 2DEG density (n_S) at the bottom AlGaN-GaN interface. The growth of N_A^+ results in particular in the increase of n_S, this in turn explaining the increasing I_D transient developing between 10^{-4} s and 10^{-2} s in the unpassivated device (see Figure 4.4).

The above considerations apply qualitatively to the passivated device as well. However, thanks to surface passivation the gate-drain electric field is significantly relaxed. This can be appreciated in Figure 4.6, showing the lateral component of the electric field along the device surface at V_{GS}=-7 V and V_{DS}=10 V.

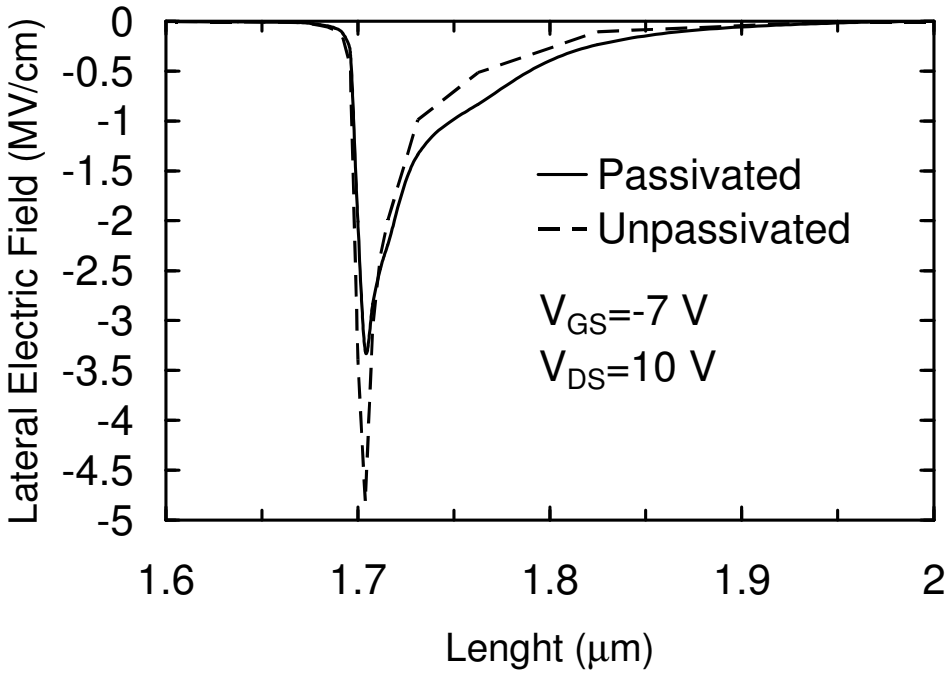

Figure 4.6: Simulated lateral electric-field component along the device surface at V_{GS}=-7 V and V_{DS}=10 V with and without surface SiN passivation. The drain-end of the gate is at 1.7 μm.

As a consequence of the reduced electric field, gate electron injection is much smaller in the passivated device with respect to the unpassivated one for the same bias. Figure 4.5 (b) shows N_A^+ along the cap in the passivated device at different times during the turn-on transient shown in Figure 4.4. Owing to reduced gate electron injection, electron trapping into surface donors is almost completely suppressed even at V_{GS}=-7 V and $N_A^+ \approx N_A$ already at t=0 s, see Figure 4.5 (b). The change in N_A^+ required to recover steady-state conditions after the application of the V_{GS} turn-on step is therefore very small. Correspondingly, the amplitude of the induced I_D transient is negligible for the passivated device, see Figure 4.4.

The two devices considered in Figures 4.4-4.6 are characterized by the same surface and buffer trap distributions. This means that, according to our simulations, the simple electrostatic effect associated with SiN passivation is sufficient to explain the removal of RF current collapse in the considered devices at the adopted bias.

Other phenomena can actually contribute to the beneficial effect of surface passivation, including the reduction of surface-trap density [39, 95], the stabilization of surface charge [44] and/or the creation of a discharge path for surface traps [99]. These effects were not considered in our analysis. Moreover, the contribution of possible, non-bulk properties of the GaN cap and/or of nonideal transport mechanisms at the device surface, like “hopping” transport through traps, were neglected by our simulations.

4.6 The role of surface and buffer traps in current collapse

4.6.1 Experimental measurement

Despite RF current collapse is not present, the pulse response shown in Fig. 4.3 is far from being ideal. It actually contains several slow variations, the more evident of which being the initial I_D decrease finishing at $t \approx 10^{-4}$ s. This transient may be induced by device self heating. Trap effects are instead likely to be at the origin of the subsequent slow I_D oscillations, but, in principle, they can contribute to the initial I_D decrease as well. Trap-related effects can be decoupled from self-heating ones by reducing the power dissipated during the ON state, i.e. by decreasing the ON-state V_{GS} and V_{DS}. Of course, the OFF-state V_{GS} must accordingly be decreased to keep trap-modulation effects appreciable.

Figure 4.7 shows, in particular, the $I_D(t)$ waveform obtained by pulsing V_{GS} from -12 V to -4 V at a V_{DD} of 1.5 V. As can be noted, three slow transients emerge clearly: one decreasing transient [labeled as (1) in Figure 4.7] starting immediately after the end of the V_{GS} rise time and extinguishing at $t \approx 10^{-6}$ s, followed by two increasing transients, the first one [labeled as (2) in Figure 4.7] mainly developing within the 10^{-4}-10^{-1} s interval , the second [labeled as (3)] starting at $t \approx 10^{-1}$ s and being truncated by the end of the V_{GS} pulse. Concerning the ringing present in the $I_D(t)$ waveform for times below 100 ns, see Figure 4.7, these are caused by voltage reflection through the measurement cables and must therefore be regarded as a measurement artifact.

As a matter of fact, DLTS characterization identified several trap levels in these devices. Activation energies and apparent capture cross sections of the three dominant traps are reported in Table 4.1. As shown in chapter III, Trap A was attributed to the cap layer and/or to the ungated surface, whereas traps B and C were inferred to be located in the GaN buffer layer.

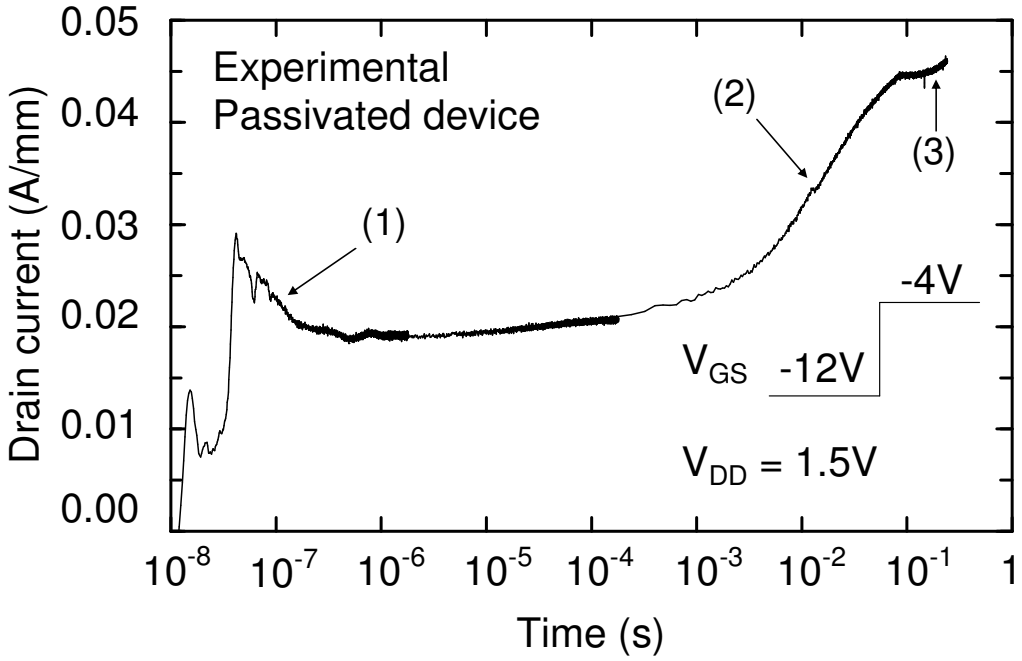

Figure 4.7: Experimental drain current versus time waveform measured in response to a gate-source-voltage (V_{GS}) pulse from -14 V to -4 V at a drain voltage (V_{DD}) of 1.5 V (applied through a 50-Ω resistor).

4.6.2 Simulation study

Figures 4.8-4.11 show simulation results aiming at clarifying the origin of the slow transients observed in Figure 4.7. Figure 4.8 shows, in particular, simulated I_D vs time waveforms in response to a turn-on V_{GS} step from two different off-state V_{GS} values ($V_{GS,OFF}$) to -4 V at a drain voltage V_{DS}=1.5 V.

When $V_{GS,OFF}$=-12 V (dashed curve), the same V_{GS} change adopted in Figure 4.7 is actually considered. As can be noted, slow transients of amplitudes comparable with those observed experimentally are reproduced by simulations. However, for $V_{GS,OFF}$= -12 V, I_{Dpulse} is significantly higher than in experiments. To obtain a better overall agreement with measurements, $V_{GS,OFF}$ had to be reduced to a smaller value, namely $V_{GS,OFF}$=-28 V (solid curve).

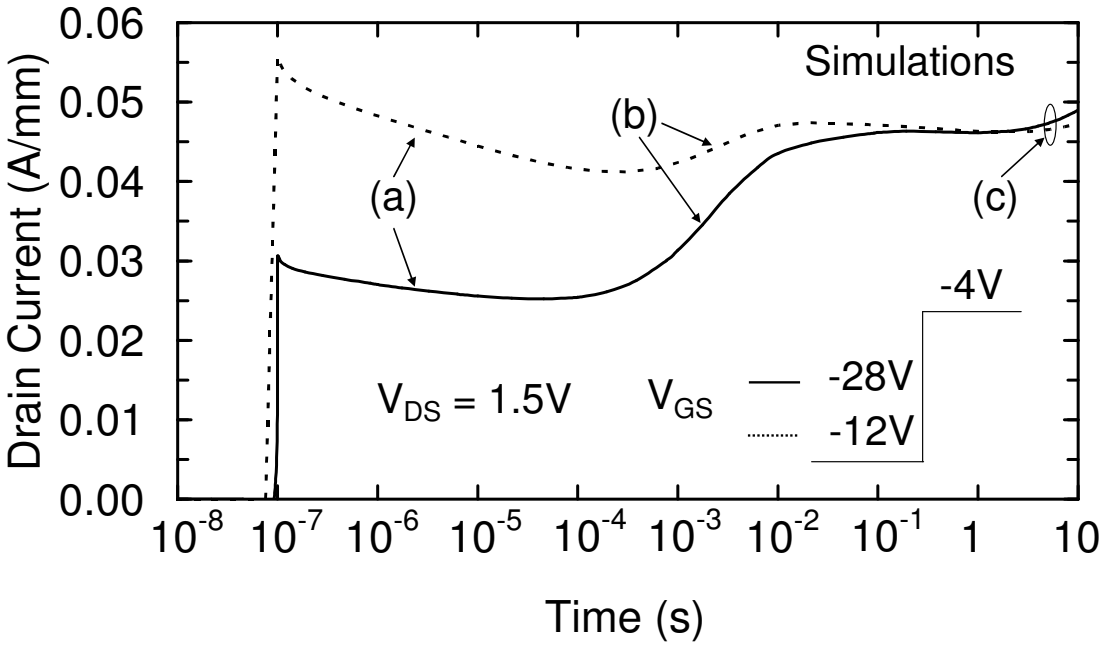

Figure 4.8: Simulated drain-current versus time waveforms in response to a turn-on voltage-source voltage (V_{GS}) step from two different off-state V_{GS} values ($V_{GS,OFF}$) to -4 V at a drain-source voltage (V_{DS}) of 1.5 V. The simulated device is passivated.

As a matter of fact, reducing $V_{GS,OFF}$ increases the gate electron injection, thus resulting in increased negative trapped charge (both into surface and buffer traps) at t=0 s, and consequently in reduced I_{Dpulse}. Our simulations underestimate the actual gate current measured from these devices. Reducing $V_{GS,OFF}$ compensates the error on I_G allowing simulations to match the experimental I_{Dpulse}. In any case, both simulated curves in Figure 4.8 exhibit three distinct transients, labeled as (a), (b), and (c), and having characteristic times comparable with those of experimental transients (1), (2), and (3), respectively (compare Figures 4.8 and 4.7).

Figures 4.9-4.11 provide insight about traps involved in the three transients (a), (b), and (c), by showing the ionized-trap-density distributions associated with surface and buffer traps at different times during the switching transient shown in Figure 4.8 for $V_{GS,OFF}$=-28 V. Figure 4.9, in particular, shows the total ionized-trap density (N_{BC}^-= N_B^- +N_C^-) associated with buffer traps B and C along a vertical cut at the centre of the gate.

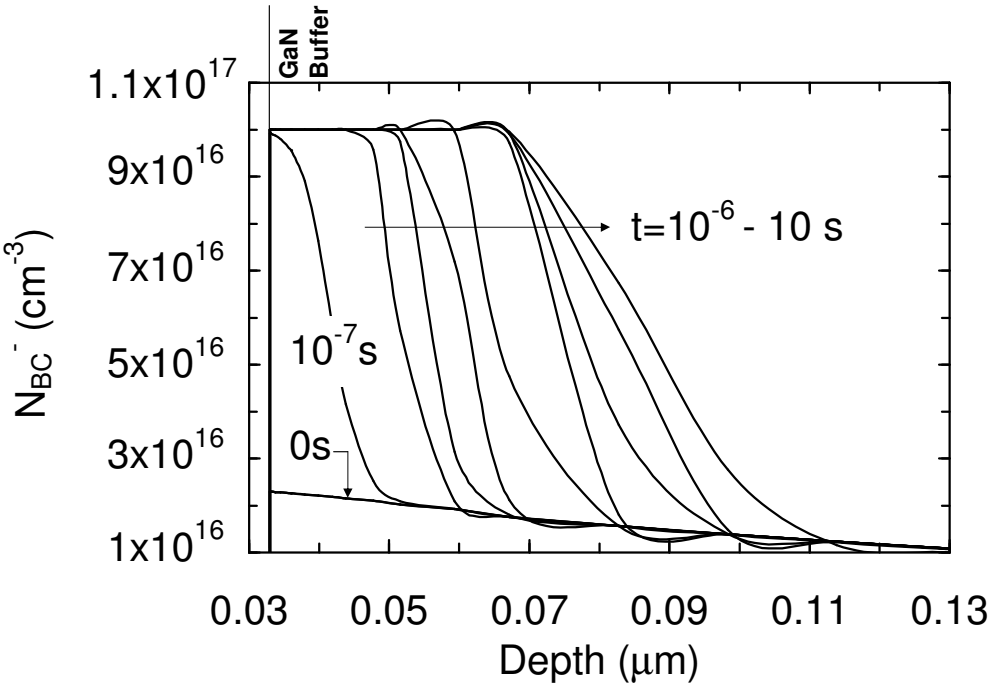

Figure 4.9: Total negative ionized-trap density (N_{BC}^-= N_B^- +N_C^-) associated with buffer acceptor traps B and C, along a vertical cut at the centre of the gate at different times (t) during the transient shown in Figure 4.8 for $V_{GS,OFF}$=-28 V.

As can be noted, N_{BC}^- increases promptly at the AlGaN-GaN interface from a small value (in the order of 2×10^{16} cm^{-3}) to its maximum value of 1×10^{17} cm^{-2} ($=N_B+N_C$) already during the V_{GS} rise time (10^{-7} s).

Afterwards, N_{BC}^- expands into the buffer. The increase in N_{BC}^- with time is due to electron trapping into buffer traps located under the gate. This, in turn, is induced by the large increase in the (free) electron concentration resulting from the applied positive V_{GS} change. These phenomena are at the origin of transient (a) in Figure 4.8. N_{BC}^- actually continues to grow with time even after transient (a) is finished. As a matter of fact, the impact of the N_{BC}^- increase on I_D decreases as traps located more and more deeply in the buffer are involved.

Figure 4.10 shows the positive ionized-trap density (N_A^+) associated with traps A along a horizontal cut in the middle of the cap region. N_A^+ increases with time owing to electron emission. The underlying mechanism is the same described earlier for Figures 4.4 and 4.5. N_D^+ changes during the 10^{-5}-10^{-1} s interval, see Figure 4.10.

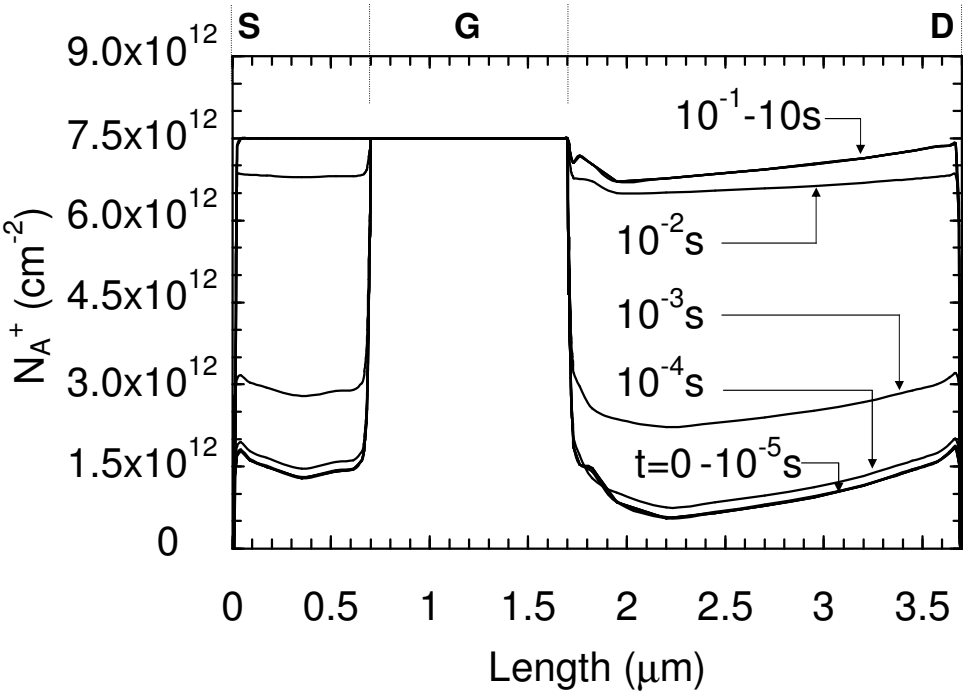

Figure 4.10: Positive ionized-trap density (N_A^+) associated with traps A along a horizontal cut in the middle of the cap region at different times (t) during the transient shown in Figure 4.8 for $V_{GS,OFF}$=-28 V.

Figure 4.11, finally, shows N_{BC}^- along a vertical cut in correspondence of the drain-end of the gate. In this region of the device, gate electron injection is maximum and buffer traps capture electrons tunneling from the gate when V_{GS} is negative and sufficiently large in modulus and emit them as V_{GS} is stepped to a less negative value. This makes N_{BC}^- to decrease at elapsing time, see Figure 4.11. This mechanism is similar to that underlying surface-trap modulation, the only differences being that (i) electrons tunneling from the gate into the buffer are involved (instead of electrons injected into the cap) and (ii) a decrease in the negative N_{BC}^- charge is induced (in place of an increase in the positive N_A^+ charge). As can be noted from Figure 4.11, N_{BC}^- drops principally during the 10^{-3}-1 s interval and then, for a lesser extent, for t> 1 s. This happens because of electron emission from buffer traps B and C, respectively. The first phase of the N_{BC}^- change is partially superimposed with the time interval when modulation of trap A takes place as well (see Figure 4.10), thus giving rise to an unbroken increasing I_D transient for time spanning from 10^{-4} s to 1 s [transient (b)]. The second phase of the N_{BC}^- change corresponds, instead, to transient (c).

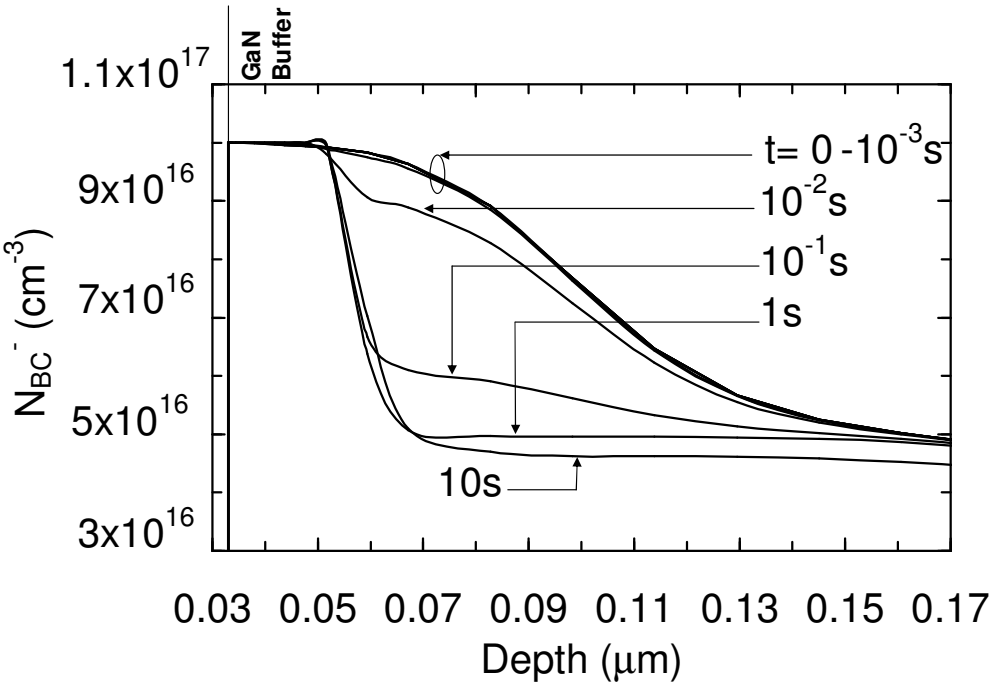

Figure 4.11: N_{BC}^- along a vertical cut in correspondence of the drain-end of the gate at different times (t) during the transient shown in Figure 4.8 for $V_{GS,OFF}$=-28 V.

Due to comparable time allocation and similar I_D behavior, it is reasonable to assume that transients (a), (b), and (c) in Figure 4.8 correspond to transients (1), (2), and (3) shown in Figure 4.7, thus suggesting that all of the three traps A, B, and C detected by DLTS contribute to the slow transients affecting the device pulse response. It is interesting to note that the role of buffer traps in RF current collapse effects has generally been associated, in previous literature, with drain-lag effects, i.e. to the delayed response observed after step changes in V_{DS} [72]. When V_{GS} is pulsed from off- to on-state conditions, a negative V_{DS} change actually takes place owing to the voltage drop induced across the drain load resistance, resulting in electron emission from buffer traps [72]. According to our simulations, buffer traps can contribute to RF current collapse also through "pure" gate-lag effects, as those shown in Figure 4.8.

4.7 Conclusions

RF current collapse effects were investigated in AlGaN-GaN HEMTs by means of measurements and device simulations. The main conclusions of our study can be summarized as follows.

1) Both surface and buffer traps can contribute to gate lag and associated RF current collapse through a similar physical mechanism involving capture of electrons tunneling from the gate when the device is biased under sub-pinch-off conditions and re-emission of trapped electrons as the device is turned on.

2) Despite other mechanisms can come into play, the primary effect of surface passivation might simply be that of reducing the gate-drain electric field, thus inhibiting electron injection from gate into traps. According to our simulations, this simple, electrostatic effect of passivation is able to account for the complete suppression of RF current collapse in the devices under study at the adopted bias.

3) For moderate surface donor trap densities per unit area ($<9\times10^{12}$ cm^{-2}), the Fermi level is not pinned by traps at the device surface. As a result, surface potential barriers in the 1-2 eV range can coexist with surface traps having much a smaller energy depth from E_C (0.18 eV in our case) and inducing RF current collapse effects characterized by relatively short time constants ($< 10^{-2}$ s).

Chapter V:

Kink effect in GaN HEMTs

5.1 Introduction

Kink effects in GaAs- or InP-based high electron mobility transistors (HEMTs) have been widely reported [100-104] and considered as sudden rise in the drain current at a certain drain-to-source voltage that results in high drain conductance and g_m compression, leading to reduced voltage gain and poor linearity. In these devices it was suggested that traps could cause the kink: trap charging in the buffer or in the insulator, leads to a shift in threshold voltage [105, 106]. On the other hand, simulations [107], as well as light emission, channel-engineering, and body contact experiments [108, 110] suggested a link between impact ionization and the kink, and that the onset of the kink strongly coincides with the onset of impact ionization in the considered devices [100].

However, the kink effects on AlGaN/GaN HEMTs have been discussed with only a few literatures, since impact ionization is difficult to be observed in AlGaN or GaN material due to their wide bandgaps and low ionization rate characteristics. The correlations between the kink effect and impact ionization have been demonstrated by Brar et al. and Dyakonova et al., where the specific electric field of 2.1×10^6 V/cm was obtained [111, 112]. The kink effect observed in the output current–voltage (I–V) characteristics is commonly attributed to impact ionization in the conducting channel, or to traps either at the surface or at the buffer. No matter what the reason is causing this effect, the mechanism is expected to have a strong dependence on temperature. In this regard, authors in [113] have discussed the kink effect in the GaN HEMTs at 100K to 300K by analyzing the device transient responses. Based on this approach, they observed that the kink was associated with a trapping mechanism time constant and was more significant at cryogenic temperatures. Furthermore, by extracting the gate hole currents they suggested that in addition to the trapping effect contributing to this kink, impact ionization to some extent also plays a role at cryogenic temperatures.

In this chapter, a possible explanation of the kink effect in GaN-based HEMTs is proposed by means of two-dimensional device simulations. Pulsed measurements, photoionisation experiments as well as spectral measurements have been performed and the obtained results are discussed.

5.2 Experimental results

5.2.1 Pulsed and DC measurements

The study was carried out on 0.5µm GaN/AlGaN/GaN HEMTs grown on SiC substrates. The gate is composed of eight fingers (W=8x125µm). The Ni/Au gate is passivated by SiN and located closer to the source than to the drain (L_{GD}=2.5µm; L_{GS}=1µm). The ohmic contacts are composed of a Ti/Al/Au/Ni stack with a Ti/Pt/Au thickening.

The I_D-V_{DS} pulsed characteristics have been measured for different quiescent points with a pulse width of 500 ns and a pulse separation of 10 µs (see Figure 5.1).

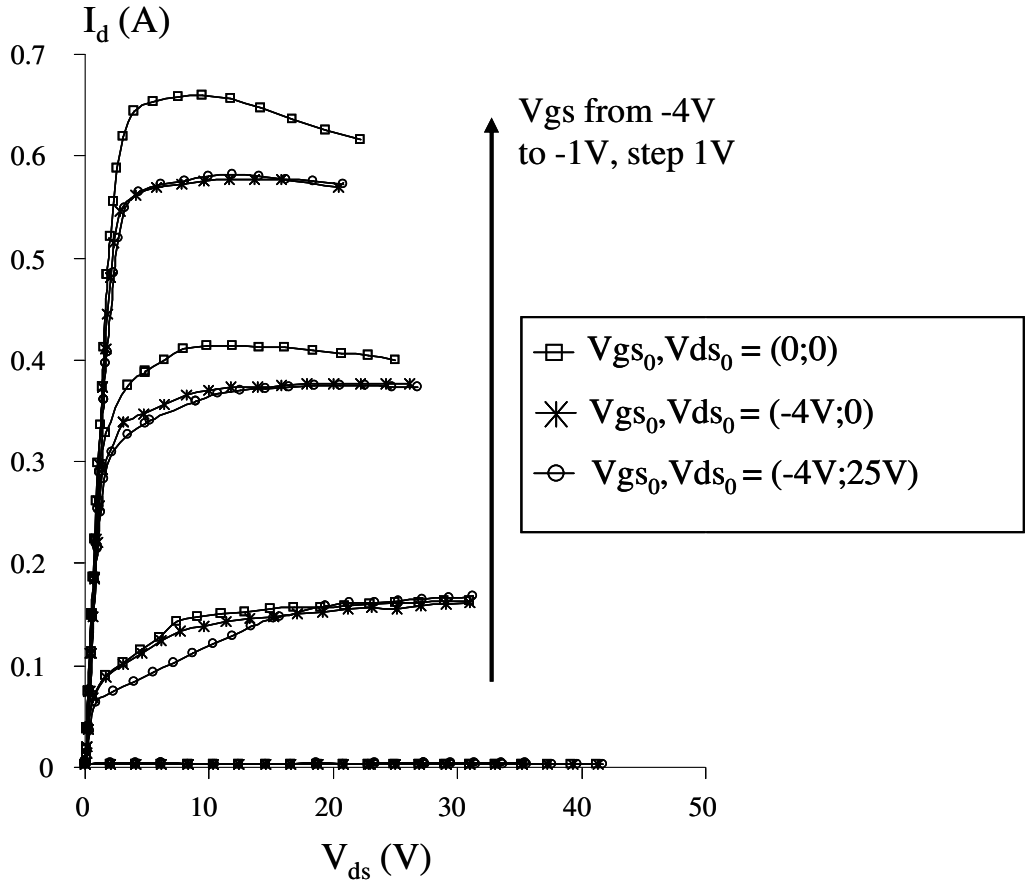

Figure 5.1: Pulsed I_D-V_{DS} characteristics measured for V_{GS} = –4V to 0V, step 1V for three quiescent bias points (V_{GS0}, V_{DS0})=(0V,0V) ;(-4V,0V) ;(-4V,25V).

As can be seen in Figure 5.1, the drain current is higher for the quiescent point (V_{GS0}, V_{DS0}) of (0V,0V) compared with the other ones. This result is linked with the activation of

surface and/or barrier traps with time constant higher than 500ns. These traps are generally assumed to induce the RF current collapse. In GaN HEMTs, detrapping time constants on the order of minutes have been reported [58, 72]. In fact, the gate-lag mechanism suggested by 2D physical simulations is basically the concept of "virtual gate" formed by surface donor traps, which capture electrons injected by the gate under large and negative V_{GS} bias and emit them as V_{GS} is switched to higher values as shown in the previous chapters.

As far as drain lag is concerned, buffer traps are predicted to play the major role [72]; in this case they should have a time constant smaller than the adopted pulse width since the drain lag effect is negligible.

On the other hand, the DC I_D-V_{DS} characteristics show a drain current collapse at small V_{DS}, related to the kink effect when increasing V_{DS} from 0V to 20V while this effect disappears partially if the measurement is performed with V_{DS} decreasing from 20V to 0V (see Figure 5.2).

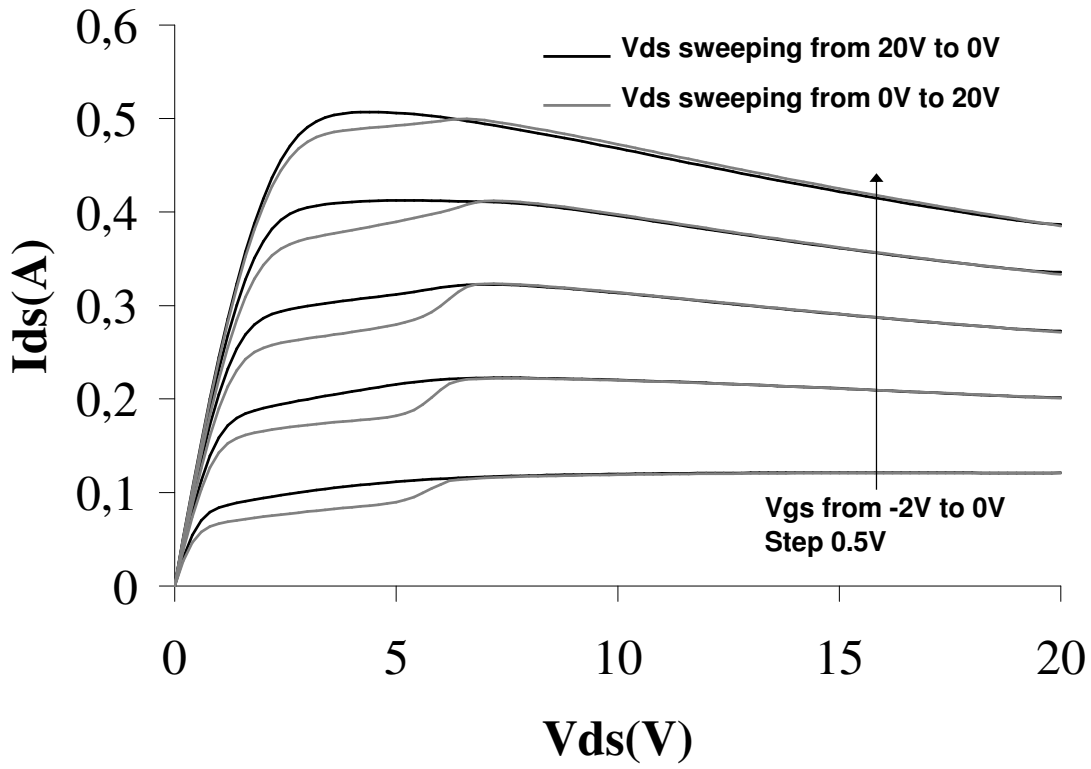

Figure 5.2: DC I_D- V_{DS} characteristics measured for V_{GS} =-2V to 0V, step 0.5V, with V_{DS} swept from 0V to 20V and subsequently from 20V to 0V.

5.2.2 Spectral measurements

The spectral study was performed with the Renishaw microscope, which is used as a spectrometer in the following spectral range: 500 nm to 1000 nm. The light emission spectrum is measured during 60 seconds.

In Figure 5.3, the light emission spectra are compared for the device in unbiased conditions and at open channel bias conditions and low V_{DS} (V_{DS} = 4V and V_{GS} = -0.5V). For these latter bias conditions, the light spectrum presents a weak intensity with discrete peaks at different energies.

These peaks correspond to the following energies: 2.3eV (545.00nm), 2.03eV (610.62nm), 1.75eV (700.00nm), 1.53eV (810.70nm), 1.47eV (841.00nm), and 1.36eV (911.60nm). The light emission spectrum features strongly depend on the device bias. The increase of V_{DS} drastically induces the increase of the amplitude of the light spectrum.

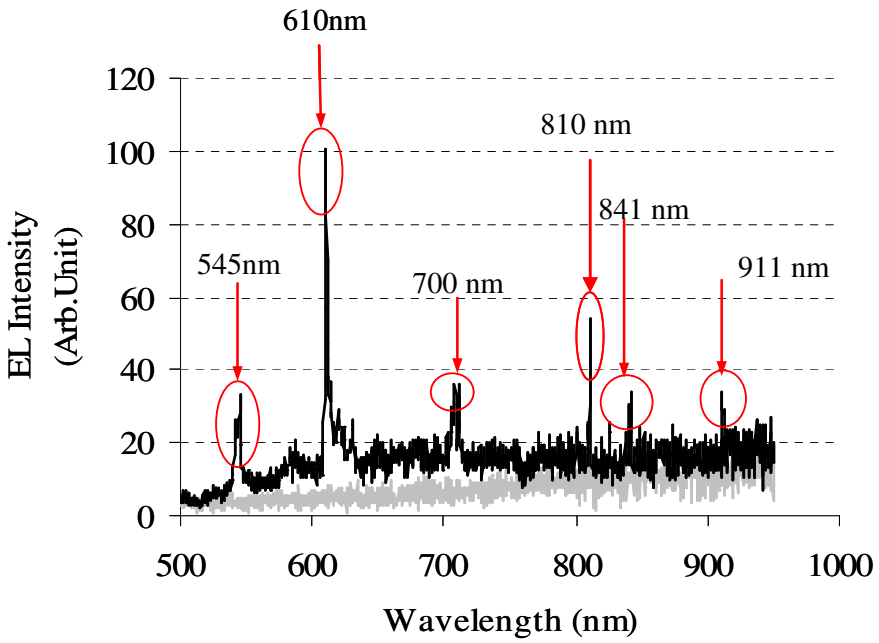

Figure 5.3: Electroluminescence spectrum in the gate drain region of the GaN HEMT under study, measured without bias (grey line) and at V_{GS} = -0.5V, V_{DS} = 4V (black line).

5.2.3 Photoionisation experiments

The devices have been illuminated with light of different wavelengths corresponding to the identified peaks in the spectral measurments in order to monitor the impact of the illumination on the DC I_D- V_{DS} and I_G- V_{DS} characteristics. This experiment aims at determining the light wavelengths/energies that separately change the drain current and the gate leakage current and therefore showing the presence of different traps in surface, barrier and buffer.

A Xenon lamp and a monochromator are used as a source, with selective filters of 1 nm resolution. The transmitted flux was measured by a photomultiplier to tune the same lighting intensity for the different wavelengths. The device is illuminated and measured simultaneously with a Keithley 4200. Then, the lighting is stopped and the device I-V static characteristics are measured again in dark condition.

A complete recovery of the current collapse effect was observed under illumination with energy around 1.75 eV as can be seen in Figure 5.4, while a significant decrease in the leakage gate current was observed under lighting with an energy of 1.45 eV as shown in Figure 5.5.

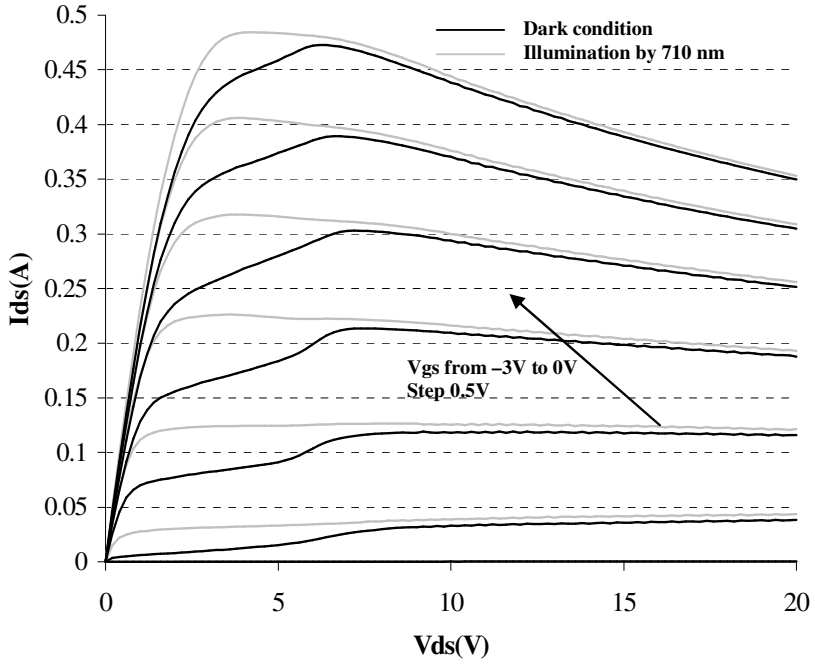

Figure 5.4: DC I_D-V_{DS} characteristics, in dark condition, and current collapse recovery while illuminating the device with light of 710 nm (1.75 eV) wavelength.

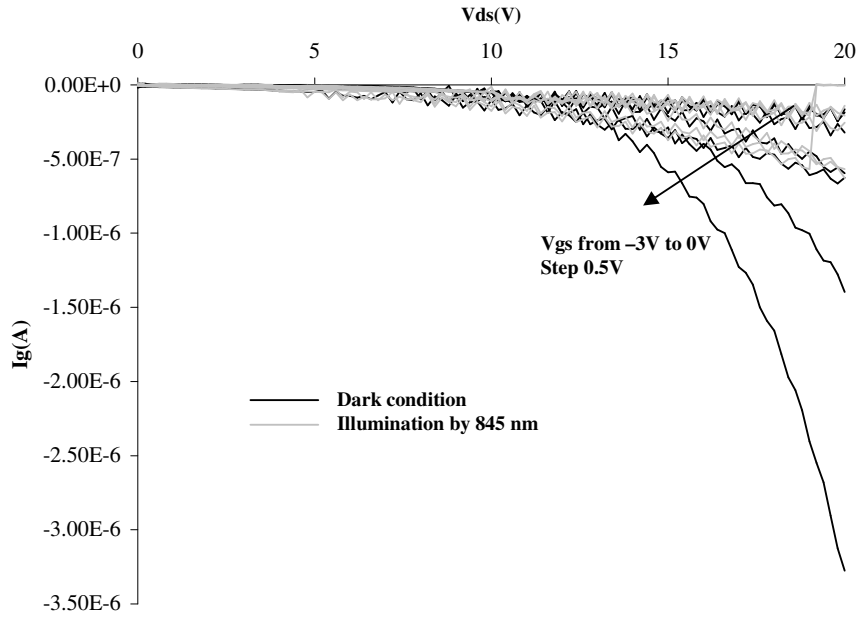

Figure 5.5: DC I_G-V_{DS} characteristics in dark condition and leakage gate current decrease observed during illumination with a wavelength of 845 nm (1.47 eV).

The effect of illumination at the other energies is negligible [114].

It has been shown that light emitted by GaN HEMTs can be attributed to intraband transitions of highly energetic electrons that acquire kinetic energy in the high field region of the channel [115, 116]. Accordingly, various trap levels are present in surface, barrier, and buffer. These traps can contribute to the different current collapse effects observed in the present work.

5.3 Simulation based interpretation

Two-dimensional numerical device simulations were carried out with the aim of giving a possible explanation to the kink effect observed in Figure 5.2. The commercial code Dessis 8.0 (Synopsys Int. Ltd) was used. The drift-diffusion model was adopted as transport model. The Schottky barrier height was set to 0.9 eV. Low-field electron mobility and electron saturation velocity in the GaN channel were set to 1100 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 1×10^7 cm/s, respectively. The gate current (I_G) was modeled as the combination of thermoionic

emission plus field-emission injection across the gate barrier. Deep-level traps were accounted for by including, for each distinct trap level, one trap-balance equation, describing, within the framework of the Shockley-Read-Hall theory, the dynamics of trap occupation without any quasi-static approximation. To account for spontaneous and piezoelectric polarization charges at the two AlGaN-GaN heterointerfaces, positive and negative fixed charges with a sheet density $N^{-}_{pol}=N^{+}_{pol}=9\times10^{12}$ cm^{-2} were placed at the bottom and top AlGaN-GaN interface respectively [6]. In agreement with the "surface-donor" theory explaining the channel 2DEG formation in GaN HEMTs [70], donor-like traps were assumed to be present at the device surface. Acceptor-like traps were instead placed within the GaN buffer in order to suppress buffer conductivity effects and fit the experimental V_{TH}.

Figure 5.6 shows the simulated I_D vs time waveform in response to a V_{DS} step from 3 V to 6 V at V_{GS}=0 V. The first decreasing transient (a) is the commonly obtained transient in the drain-lag measurements, which is ascribed to electron trapping to buffer traps as confirmed by inspection of internal simulations results (see Figure 5.7) showing that the density of ionized buffer traps is increasing in the time interval of transient (a). The second increasing transient (b) is obtained only if donor-like traps are included in the AlGaN barrier. Insight can be gained with the aid of Figure 5.8, showing the ionized-trap density (N_B^+) associated with barrier traps along a vertical cut at the centre of the gate at different times during the turn-on transient shown in Figure 4. Owing to electron emission, N_B^+ increases in the corresponding time interval of the increasing transient (b), thus explaining the I_D increase.

The above physical mechanism suggested by simulations could be at the origin of the current collapse (kink effect) observed in Figure 5.2. As a matter of fact, the points of the output characteristics are obtained by applying different V_{DS} steps. Therefore, if the current is measured before the emission transient is completed (see Figure 5.6), the obtained value will be lower than the one of steady-state condition giving rise to the current collapse observed in Figure 5.2. It is worth mentioning that the activation energy of barrier traps used in simulation was assumed to be 0.7 eV, and of course, the deeper the donor-trap energy, the longer the emission time constant.

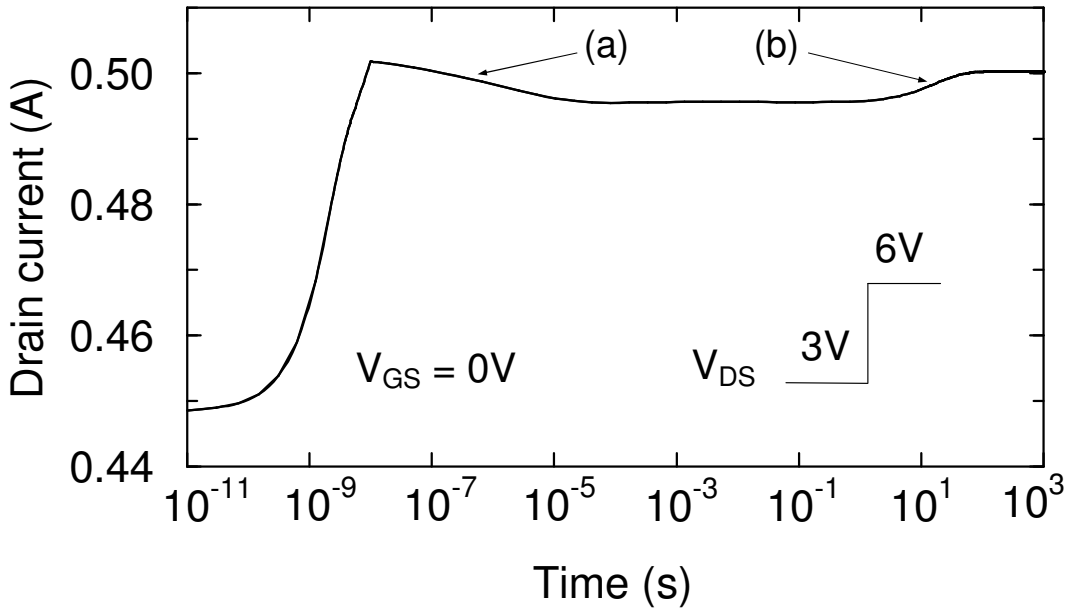

Figure 5.6: Simulated I_D vs time waveform in response to a V_{DS} step from 3 V to 6 V at V_{GS} =0 V.

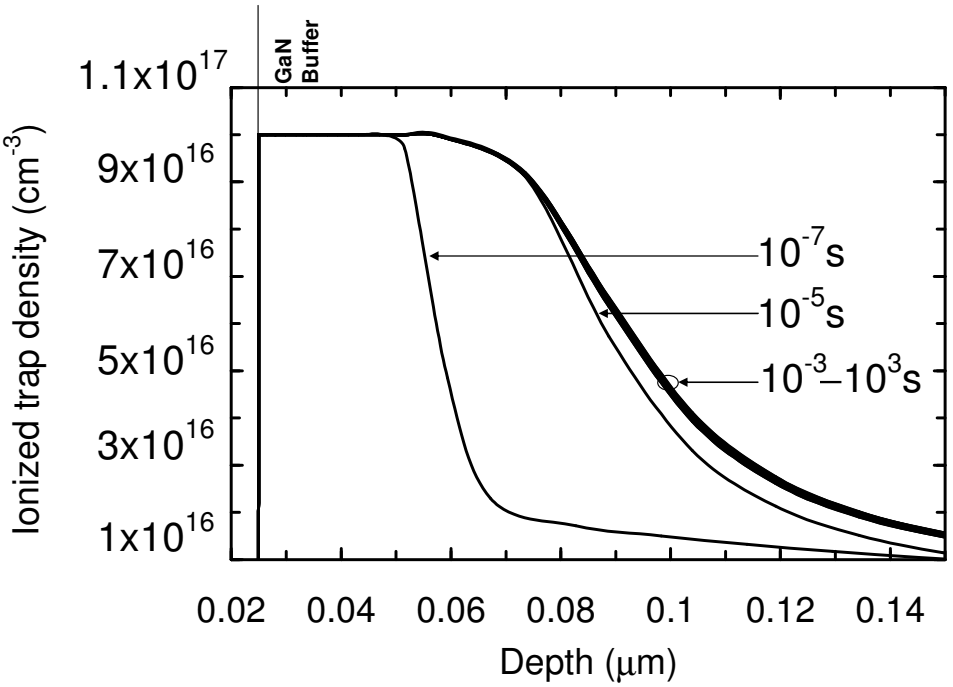

Figure 5.7: Ionized-trap density associated with buffer traps along a vertical cut at the centre of the gate at different times during the turn-on transient shown in Figure 5.6.

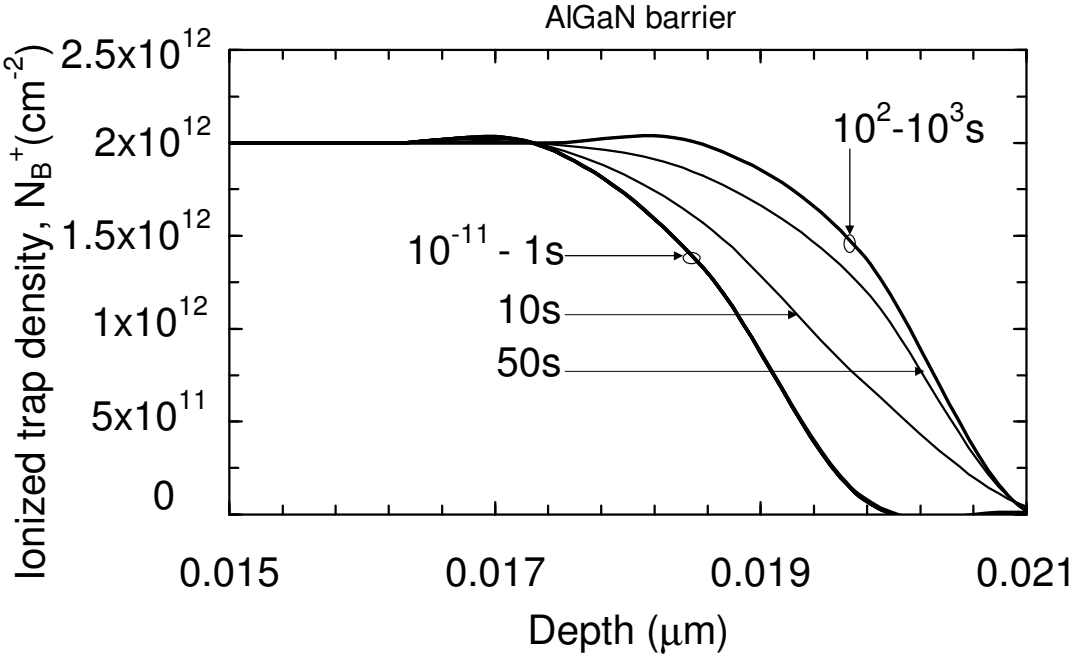

Figure 5.8: Ionized-trap density (N_B^+) associated with barrier traps along a vertical cut at the centre of the gate at different times during the turn-on transient shown in Figure 5.6.

At equilibrium (V_{DS}=0 V), part of electrons get trapped in barrier traps before reaching the channel. Afterward, V_{DS} is stepped to higher values, and once a certain value of electric-field is reached, electrons start being emitted by traps giving rise to a transient characterized by a time constant.

On the other hand, if the measurement is performed with V_{DS} decreasing from 20V to 0V (see Figure 5.2), electron trapping to barrier traps is expected to take place in order to obtain the kink effect. Nevertheless, in this situation, barrier is almost completely depleted and the density of free electrons is very small, thus suppressing electron capture. Correspondingly, almost all barrier traps are ionized and the trapping effect is negligible, in other words the capture time constant is very high.

These simulation suggestions are confirmed by experimental results showing that kink effect is not present in output characteristics measured at a temperature of 155°C (see Figure 5.9). Obviously, the higher the temperature, the lower the emission time constant and therefore the shorter the time required to reach the steady-state condition.

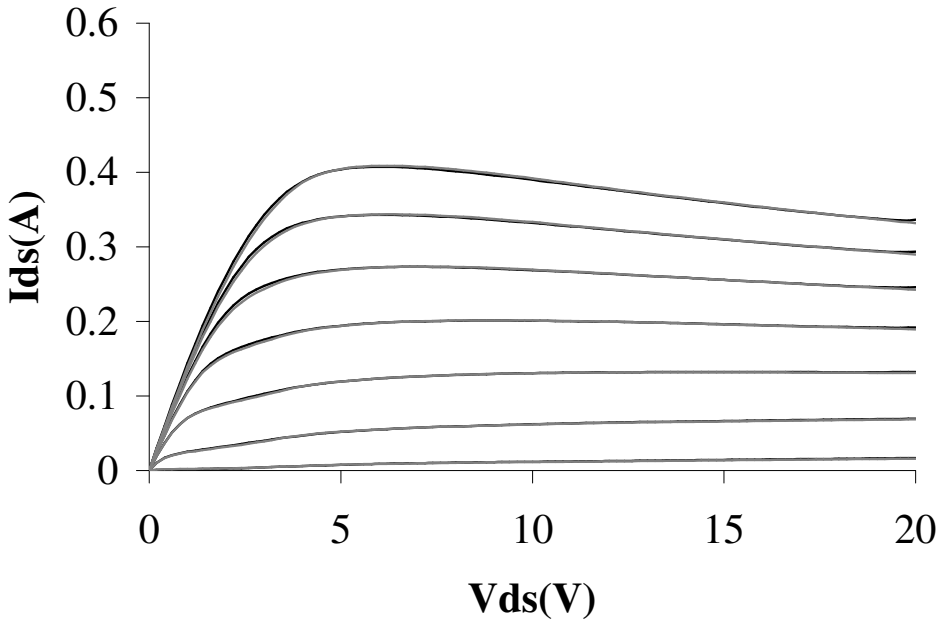

Figure 5.9: DC I_D-V_{DS} characteristics, for V_{GS} =-3V to 0V, step 0.5V, with V_{DS} sweeping, first from 0V to 20V (grey line) and from 20V to 0V (black line) at T=155°C.

5.4 Conclusion

In conclusion, current collapse effects have been analyzed in our study by means of measurements and 2D physical simulations. The presence of different trap levels causing current collapse effects has been demonstrated by pulsed measurements and photoionisation. Finally, simulations suggest that kink effect can be explained by electron trapping into barrier traps and a subsequent electron emission once a certain value of electric-field is reached.

Conclusions and future work

Conclusions and future work

In this thesis we have presented the results of an extensive analysis of the physical mechanisms that limit the performance and reliability of GaN-based HEMTs.

High-electric-field degradation phenomena have been investigated in GaN-capped AlGaN/GaN HEMTs by comparing experimental data with numerical device simulations. Under power- and OFF-state conditions, 150-h DC stresses were carried out. Degradation effects characterizing both stress experiments were as follows: a drop in the dc drain current, the amplification of gate-lag effects, and a decrease in the reverse gate leakage current. Numerical simulations indicate that the simultaneous generation of surface (and/or barrier) and buffer traps can account for all of the aforementioned degradation modes. Experiments also showed that the power-state stress induced a drop in the transconductance at high gate–source voltages only, whereas the OFF-state stress led to a uniform transconductance drop over the entire gate-source-voltage range. This behavior can be reproduced by simulations provided that, under the power-state stress, traps are assumed to accumulate over a wide region extending laterally from the gate edge toward the drain contact, whereas, under the OFF-state stress, trap generation is supposed to take place in a narrower portion of the drain-access region close to the gate edge and to be accompanied by a significant degradation of the channel transport parameters. Channel hot electrons and electric-field-induced strain-enhancement are finally suggested to play major roles in power-state and off-state degradation, respectively.

Traps have been characterized in AlGaN-GaN HEMTs by means of DLTS techniques and the associated charge/discharge behavior is interpreted with the aid of numerical device simulations. Under specific bias conditions, buffer traps can produce ‘‘false’’ surface-trap signals, i.e. the same type of current-mode DLTS (I DLTS) signals that are generally attributed to surface traps. Clarifying this aspect is important for both reliability testing and device optimization, as it can lead to erroneous identification of the degradation mechanism, thus resulting in wrong correction actions on the technological process.

The physical mechanisms underlying RF current collapse effects in AlGaN-GaN high-electron-mobility transistors have been studied by means of measurements and numerical device simulations. The following conclusions have been proposed: i) both surface and

buffer traps can contribute to RF current collapse through a similar physical mechanism involving capture and emission of electrons tunneling from the gate; ii) surface passivation strongly mitigates RF current collapse by reducing the surface electric field and inhibiting electron injection into traps; iii) for surface-trap densities lower than 9×10^{12} cm^{-2}, surface-potential barriers in the 1–2 eV range can coexist with surface traps having much a shallower energy and, therefore, inducing RF current-collapse effects characterized by relatively short time constants.

Current collapse effects have been investigated in AlGaN/GaN HEMTs by means of measurements and numerical device simulations. According to pulsed measurements, the adopted devices exhibited a significant gate-lag and a negligible drain-lag ascribed to the presence of surface and buffer traps, respectively. Furthermore, it has been shown that illumination of the devices with two specific wavelengths can result in either a recovering of current collapse or a decrease in the gate current. On the other hand, numerical device simulations have suggested that the kink effect can be explained by electron trapping into barrier traps and the subsequent electron emission after a critical electric-field is reached. In this regard, more experimental measurements will be carried out in order to extract all the parameters of the traps involved in the various current collapse effects that have been mentioned and find out the correlation between the photoionisation and current collapse. In addition, the same analysis will be applied to other kind of devices in order to confirm the obtained results.

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