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Development of CMOS sensors with digital pixels for the ILD vertex detector

Composition du jury:

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Résumé en Français

R.1 Introduction

Afin d'étendre notre compréhension des mystères de l'univers, des expériences de physique subatomique ont été menées. Ces expériences nécessitent des détecteurs fiables pour mesurer le produit de la collision. L'énergie des particules est mesurée avec des calorimètres, et les impulsions sont fournies par le trajectomètre. Parce les quarks lourds ont une durée de vie courte de l'ordre de picoseconde, ils ne peuvent être reconnus que par les trajectoires provenant des vertex de la désintégration secondaire. Cette tâche est accomplie avec le détecteur de vertex (VTX) avec une grande précision pour être placé très près du point d'interaction. Cette thèse vise à contribuer au développement d'un type prometteur de capteur de pixels de silicium — CMOS Pixel Sensor (CPS) — utilisé pour équiper le détecteur de vertex pour le Collisionneur Linéaire International (International Linear Collider, ILC).

L'ILC est la prochaine grande installation expérimentale en physique des hautes énergies, en complément pour le LHC (Large Hadron Collider au CERN). Les caractéristiques proéminentes de l'ILC y compris l'énergie du faisceau bien défini, des faisceaux polarisés, un background de fonctionnement propre, permettre une mesure précise pour vérifier et étendre les découvertes réalisée au LHC. Par exemple, deux deux expériences — ATLAS et CMS — appartenant au LHC ont confirmé l'existence du boson de Higgs à $\sim$125 GeV/c^2. L'ILC peut mesurer ses propriétés avec précision, y compris la masse, le spin, les canaux de désintégration pour vérifier l'identité davantage. Le fonctionnement de l'ILC commencera à partir d'une énergie de centre-de-masse de 500 GeV et une luminosité de $1,8\times10^{34}$ cm^{-2}s^{-1}, par la suite monter finalement à $\sim$1 TeV [1]. La longueur totale de l'installation de l'ILC est l'ILC 31 km. Le seul point d'interaction est entouré par un parmi deux détecteurs — International Grand Detector (ILD) et Silicon Detector (SiD) fonctionnant dans un schéma push-pull à partager une même luminosité. Tous les deux détecteurs suivent l'algorithme de flux de particules (Particle Flow Algorithm, FPA) pour séparer et mesurer les particules neutres dans le calorimètre et les particules chargées dans le trajectomètre. Leur différence principale entre est que le trajectomètre dans l'ILD est hybridée par TPC et de silicium, tandis que le SiD est réalisé par tout-silicium. La figure R.1(a) montre une vue artistique complète de l'expérience ILD. Le détecteur est composé de plusieurs sous-détecteurs, qui sont illustrés sur la figure R.1(b).
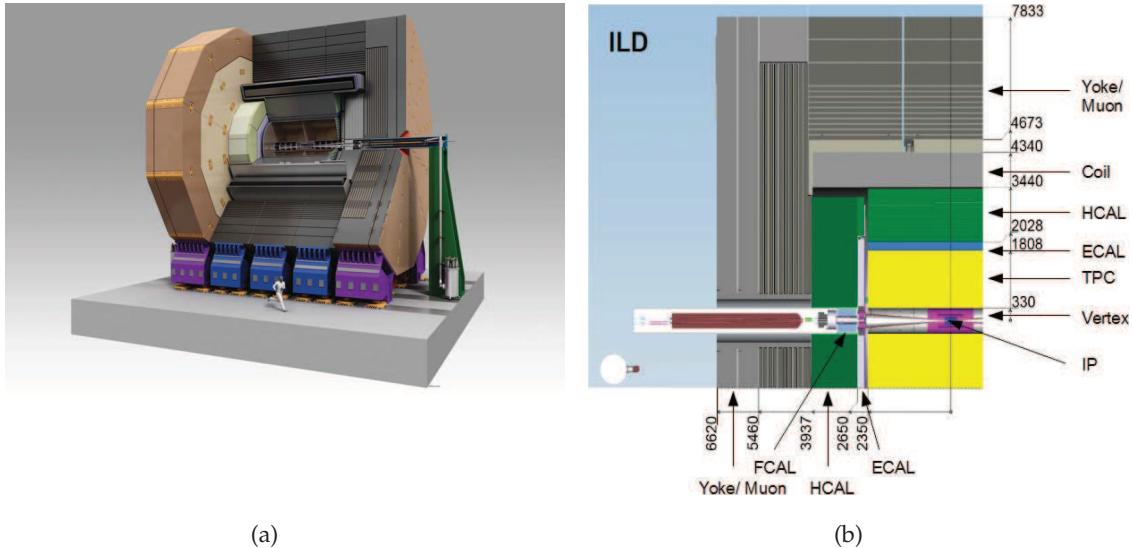
Figure R.1: *Architecture de l'expérience ILD. (a) Vue en perspective de l'expérience ILD, (b) vue du détecteur en coupe.*

La capacité de reconstruire les vertex de la désintégration de la particule de courte durée de vie s'appuie sur le fait que le VTX dispose une mesure de haute précision des trajectoires des particules chargées dans le voisinage du point d'interaction. Afin d'atteindre une résolution spatiale de point extraordinaire, le VTX est composé d'une structure cylindrique concentrique multi-couche et chaque couche présente une forte résolution spatiale. En plus, un budget de matière comprimé est imposé pour chaque couche. La condition opérationnelle de rigueur impose aussi des exigences sur la vitesse de lecture et la tolérance au rayonnement. Malheureusement, les exigences mentionnées sont généralement en contradiction, ce qui résulte en un défi pour la R&D du VTX.

Deux géométries candidates existent pour l'ILD-VTX, comme l'illustre la figure R.2: une avec 5 couches simple-face ce qui signifie qu'un seul côté de chaque couche est équipé des capteurs, et l'autre avec 3 couches double-face où tous les deux côtés de chaque couche sont montés avec des capteurs indépendants [2]. Plusieurs techniques de capteurs sont activement développées pour satisfaire les exigences du détecteur de vertex de l'ILD. Parmi eux, les capteurs à pixels CMOS (CPS) est un candidat prometteur. Une série de prototypes CPS développée à l'IPHC (Institut Pluridisciplinaire Hubert Curien, Strasbourg, France), appelé MIMOSA, a été vérifiée en performances par les tests de faisceau. Le volume sensible constitué par la couche épitaxiale de haute résistance peut être implémenté en même temps que les circuits de traitement du signal sur le même substrat de silicium par le procédé CMOS du commerce. Une structure de grande densité en pixel assure la résolution spatiale suffisante. Le CPS permet que l'amincissement soit adéquat pour l'application de faible masse. Le sujet de cette thèse est le développement des prototypes CPS dédiés aux couches externes du détecteur de
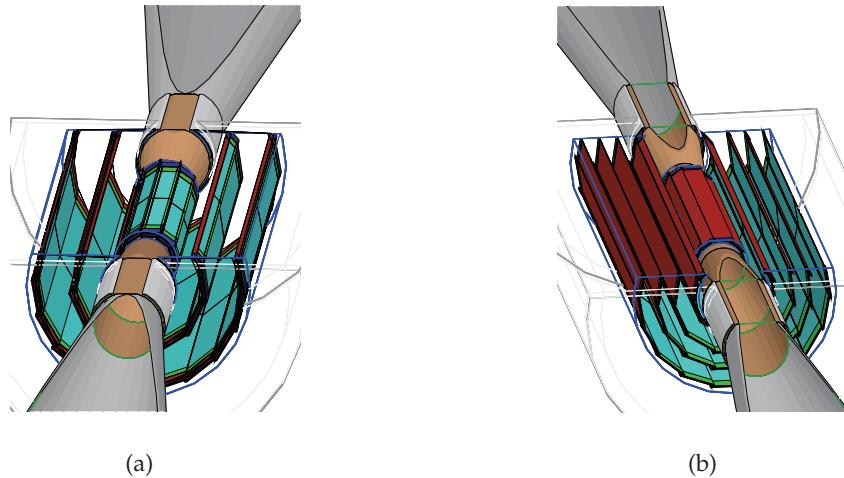
Figure R.2: *Géométrie d'un détecteur de vertex: (a) 3 couches doubles (VTX-DL); (b) 5 couches simples (VTX-SL).*

vertex de l'ILD.

La R&D des capteurs pour le VTX dans l'ILD est motivée par les contraintes de fonctionnement. Il exist une différence significative dans les contraintes de fonctionnement entre la couche la plus interne et les couches extérieures, en raison de la variation du gradient de la densité des impacts en rapport avec le rayon de la couche. Dans la couche la plus intérieure, l'accent dans la conception est mis sur la vitesse de lecture et la granularité. Le CPS peut bénéficier de la géométrie des couches à double face puisque une face est montée par le capteur de segmentation élevée pour la haute résolution spatiale, et l'autre côté est muni des capteurs composés de pixels allongés pour la vitesse de lecture élevée [3]. La priorité des capteurs montés sur les couches externes est une faible consommation d'énergie en raison du rapport élevé de couverture de la surface sensible (∼90 %) dans le VTX. Entre temps, la faible densité des impacts s'accommode de pixels des plus grandes dimensions, ainsi que dans la vitesse de lecture. Un pixel relativement grand de 35×35 µm^2 est adopté de manière à réduire le nombre de colonnes, et en outre la consommation d'énergie. La perte en résolution spatiale est compensée par l'encodage du signal sur 3-4 bits de CAN (Convertisseurs Analogiques Numériques) pour parvenir à une résolution spatiale estimée à ∼3-4 µm. Les prototypes précédents ont permis de vérifier que le bruit du pixel est d'environ 1 mV. Afin diminuer la résolution sur la position de reconstruction de la particule, le bit le moins significatif (least significant bit, LSB) est fixé au niveau du bruit du pixel. Le premier capteur prototype qui cible les couches externes de l'ILD-VTX, appelé MIMOSA-31, avait été conçu avant cette thèse. Il est composé de 48×64 pixels avec un pas de 35 µm, et du CAN 4-bits de colonnes parallèles qui numérise les sorties de chaque colonne.

CAN dans le CPS fournissent une relation de correspondance un-à-un entre la quantité de la charge recueillie et les codes numériques nécessaires pour positionner les particules in-

cidentes. Dans les capteurs à pixel, les CAN peuvent être implémentés à des niveaux divers, entre autre au niveau de la puce, de la colonne et du pixel. En comparaison des CAN au niveau de la puce, ceux au niveau de la colonne présentent l'avantage d'un temps de relaxation élevé à la fréquence de conversion, présentant ainsi une réduction de la consommation d'énergie. Cependant, le rapport signal sur bruit (Signal-to-Noise Ratio, SNR) est considérablement dégradé parce que les signaux analogiques faibles qui sortent des pixels doivent traverser le long bus de colonne, et cela devient encore pire pour un capteur de grande échelle. En outre, les tampons analogiques, avec la capacité de conduite forte pour entraîner les grandes capacités parasites réparties sur les fils de colonnes, résultent une consommation d'énergie significative.

La cause des problèmes mentionnés ci-dessus réside en ce que les sorties analogiques des capteurs ne sont pas seulement sensibles au bruit, mais aussi difficiles d'être traitées davantage. Le concept du capteur numérique de pixel (Digital Pixel Sensor, DPS) est proposé qui comporte la sortie tout-numérique directement à partir du pixel. La sortie numérisée a le mérite de l'immunité au bruit et est facile d'être dirigée, ce qui fournit une performance supérieure sur le SNR et la consommation d'énergie. Dans le DPS, les circuits complexes de traitement du signal sont intégrés dans les pixels afin d'obtenir des fonctions plus intelligentes. La numérisation de pixel permet également l'opération parallèle de pixel pour atteindre une vitesse de lecture élevée. En plus, des circuits en plus petit nombre de colonnes conduisent à moins de zones mortes existant dans le capteur. Le CAN au niveau du pixel est la clé essentielle dans la construction du DPS. Le principal défi dans la conception est comment intégrer un CAN complète au sein d'un pixel de zone limitée. Le circuit de pixel complexe aussi demande un agencement sophistiqué pour réduire la diaphonie entre les blocs voisins. Ceux défis seront étudiés dans ce travail.

R.2 Travail Doctoral

Les capteurs équipant les couches externes du VTX ont la priorité sur le SNR et la consommation d'énergie, ce qui offre une opportunité de remplacer les CAN de colonnes parallèles par ceux au niveau du pixel. Entre temps, la grande taille du pixel est également en faveur de la disposition complexe. Dans cette thèse, un prototype de capteur, appelé MIMADC, est mis implémenté par un processus de 0,18 µm CIS, visant à l'application de la couche extérieure VTX dans l'ILD. L'objectif de ce capteur est de vérifier la faisabilité du CPS intégré avec les CAN au niveau des pixels à fonctionner dans un contexte de fréquence élevée. Trois matrices sont incluses dans ce prototype, mais avec deux types de CAN au niveau de pixel différents: une matrice, appelé MIMADC-SAR, avec des CAN à registre à approximations successives (SAR); les deux autres, appelé MIMADC-SS1 et -SS2, avec des CAN à une seule pente (Single-Slope, SS) CAN. Toutes les trois sont dotées de pixels de la même taille de $35{\times}35$ µm^2 et une résolution de 3-bit, réduisant ainsi la consommation d'énergie tout en gardant la résolution spatiale nécessaire.

R.2.1 Conception de CAN SAR de niveau de pixels
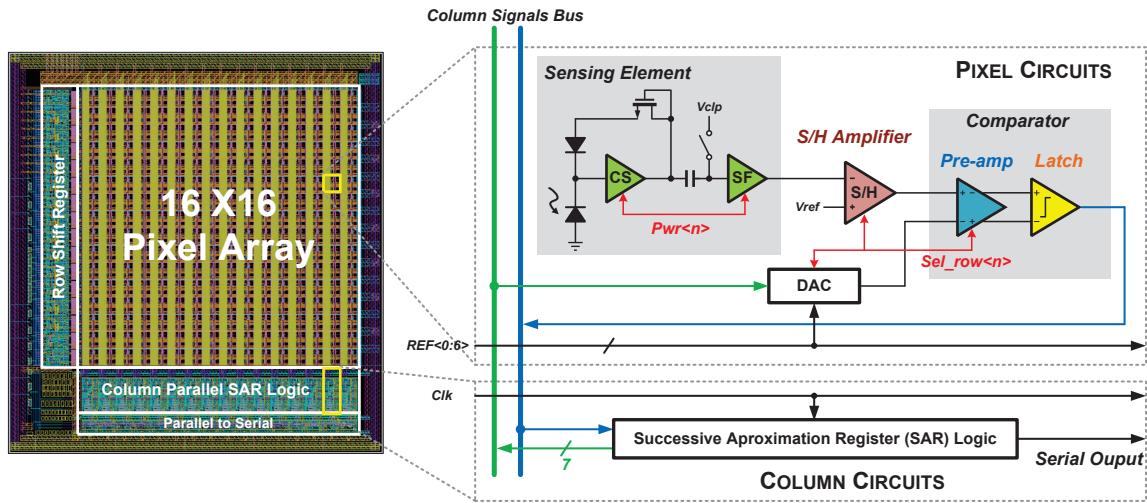
Figure R.3: *Architecture du MIMADC-SAR.*

La figure R.3 présente le schéma fonctionnel d'un convertisseur SAR qui contient une matrice de 16×16 pixels. La matrice de pixels est lue en mode volet roulant qui pilote via un sélecteur de ligne et un séquenceur de pixels situés sur le côté gauche. En mode volet roulant où la matrice est lue, une seule ligne est sous tension et contribue ainsi à la consommation d'énergie de la matrice. Chaque pixel inclut un élément de détection et un CAN SAR. L'élément de détection combine amplification au sein des pixels et opération d'échantillonnage double liée. Afin de maximiser le rapport signal sur bruit, un amplificateur de source commune avec un gain et une rétroaction améliorés a été utilisé.

Le CAN SAR se compose d'un amplificateur d'échantillonnage-mise en attente (sampling-and-hold, S/H), d'un convertisseur numérique-analogique (CNA), d'un comparateur et d'un circuit logique SAR. Pour améliorer la précision de conversion et réduire le bruit à motif fixe (fixed pattern noise, FPN), un amplificateur à boucle fermée est utilisé. Le gain de cet amplificateur est défini par le rapport de deux condensateurs, menant ainsi à une dispersion minimisée du processus. Le comparateur comprend un préamplificateur et une bascule dynamique. Les influences du décalage du verrou, du bruit de «kickback» et de la traversée d'entrée sont nettement atténuées dans la conception. Dans un CAN SAR typique, le CNA mis en place par un ensemble de condensateurs à poids binaire occupe un vaste espace et nécessite une grande quantité de courant pour piloter. Dans cette configuration, une structure multiplexe de commutateurs est utilisée pour respecter les exigences relatives à l'intégration au sein des pixels et à une faible consommation d'énergie. Pour le processus CMOS de 0,18 μm

employé, la zone de pixels limitée ne peut pas intégrer le circuit logique SAR. Le mode volet roulant où la matrice est lue nous permet de localiser le circuit logique SAR à l'extrémité de la colonne. Chaque circuit logique SAR au niveau de la colonne est partagé par les pixels dans la colonne correspondante. Malgré la présence de circuits au niveau de la colonne, la numérisation au sein des pixels permet de garantir de bonnes performances en termes de bruit, de vitesse et de consommation d'énergie. En outre, la contribution du circuit logique à la zone insensible est négligeable.

R.2.2 Conception de CAN SS de niveau de pixels

Nous proposons deux matrices de pixels avec des CAN de niveau de pixels basés sur des architectures SS. Chacune d'entre elles contient 16×18 pixels. La principale différence entre elles est la disposition des mémoires numériques : dans la matrice MIMADC-SS1, les mémoires sont placées à l'extrémité des colonnes, de la même façon que le circuit logique SAR du modèle MIMADC-SAR; dans la matrice MIMADC-SS2, les mémoires sont intégrées dans chaque pixel. De plus, la différence réside également dans la conception de l'amplificateur S/H.
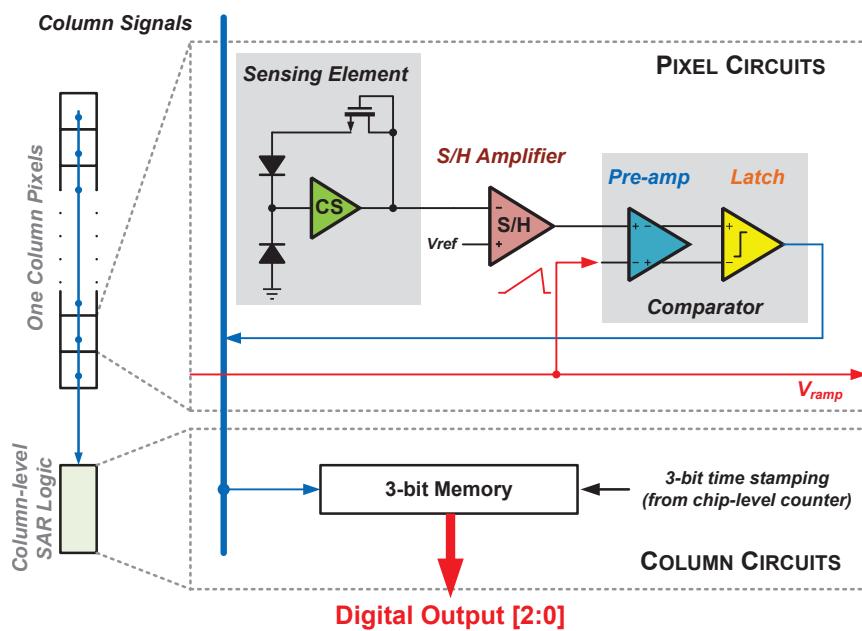
Figure R.4: *Synoptique d'un pixel du MIMADC-SS1.*

Le schéma fonctionnel de la matrice MIMADC-SS1 est illustré dans la figure R.4. Les circuits de pixels sont les mêmes que ceux de la matrice MIMADC-SAR. Les mémoires du CAN

se trouvent à l'extrémité des colonnes et sont partagées par les pixels dans la colonne correspondante. Cette architecture assouplit la limitation de la zone de pixels et permet de mettre en place les mémoires par les bascules «flip-flop» fournies par la bibliothèque de cellules standard.
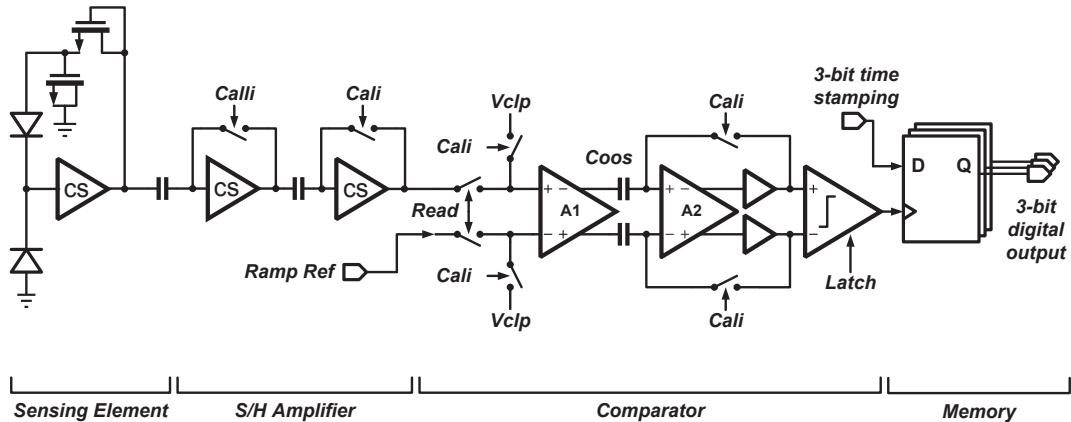
Figure R.5: *Schéma de un pixel du MIMADC-SS2.*

Dans les deux matrices précédentes (MIMADC-SAR et MIMADC-SS1), le circuit au niveau de la colonne limite l'extension d'une lecture de volet roulant à ligne unique vers une approche à plusieurs lignes. Afin d'atteindre une vitesse de lecture supérieure adaptée à l'énergie de collision de l'ILC allant jusqu'à 1 TeV, une architecture différente (MIMADC-SS2) a été conçue. Comme illustré sur la figure R.5, dans la matrice MIMADC-SS2 le pixel est intégré à une chaîne de signal complète qui couvre la détection de particules, l'amplification, la conversion analogique-numérique et le stockage de données. Cette architecture permet d'utiliser une méthode de lecture flexible pour un taux de trame élevé et/ou une consommation d'énergie basse. Pour économiser la zone de pixels pour les mémoires, un amplificateur S/H à deux étages et à boucle ouverte est employé.

Afin de générer une référence de rampe pour les CAN SS, un générateur de rampe sur puce a été conçu. Pour être différente du générateur de rampe traditionnel basé sur le chargement d'un condensateur avec un courant constant, notre conception utilise une architecture adaptative. Les principaux paramètres du signal de rampe (par ex. le temps de montée) peuvent être régulés sur la carte. La rétroaction assure une haute linéarité et une bonne tolérance aux variations de processus.

R.2.3 Caractérisation de la puce MIMADC

La microphotographie de la matrice MIMADC est montrée sur la figure R.6. La taille de
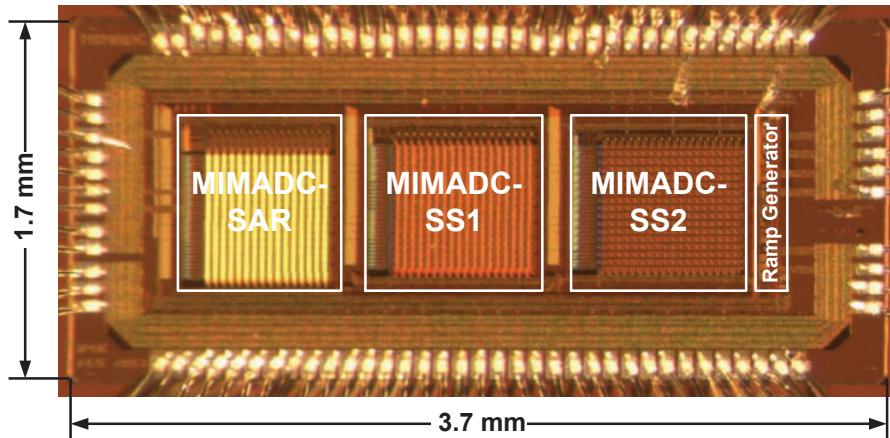
Figure R.6: *Photographie du prototype MIMADC bondé sur la carte de test.*

la puce est de 1,7×3,7 mm². Les résultats du CAN en série sont transmis par quatre paires de dispositifs de signalisation différentielle à basse tension (Low-Voltage Differential Signaling, LVDS), qui sont multiplexés par trois matrices. Les trois différents types de CAN peuvent être caractérisés indépendamment. Deux cartes de test ont été conçues et fabriquées. Comme illustré sur la figure R.7, la puce est microcâblée à la carte de proximité, laquelle peut être branchée dans la carte auxiliaire. Un stimulus analogique d'amplitude variable est injecté dans les entrées du CAN. Les résultats de la mesure vérifient les performances de base, notamment le bruit temporel, le bruit à motif fixe, la non-linéarité et la consommation d'énergie. Le prototype a été mesuré en utilisant une horloge externe de 100 MHz pour générer la séquence du temps de fonctionnement. Le temps de conversion correspondant des CAN SAR et des CAN SS est respectivement de 160 ns et de 180 ns. En outre, la puce a également été mesurée avec une fréquence d'horloge inférieure pour explorer l'influence de la diaphonie, qui est généralement fonction de la fréquence. Les caractéristiques mesurées des trois matrices sont résumées dans le tableau R.1.

R.3 Conclusion

Dans ce thèse, nous présentons des études faites sur les capteurs de pixels CMOS pour aux couches externes de l'ILD-VTX. Le premier prototype de capteur CMOS intégré à des CAN de niveau de pixels à 3 bits a été conçu en ayant pour objectif de réduire la consommation d'énergie sans perdre de résolution spatiale. Diverses architectures de CAN et topologies de puce ont été explorées pour vérifier la faisabilité de la mise en place de CAN dans une
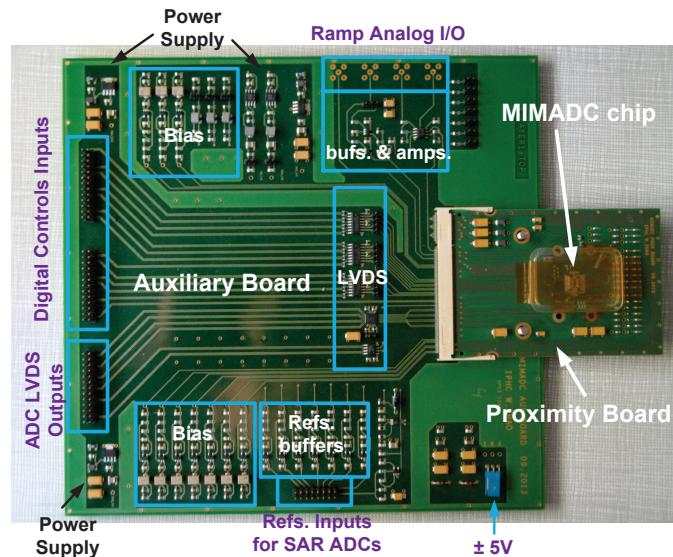
Figure R.7: *Photo de la carte de test du MIMADC*

Charactéristiques	SAR	SS-1	SS-2
Technologie	Towerjazz 0,18 µm CIS		
Résolution	3 bits		
Fréquence d'échantillonnage	6,25 MS/s	5,55 MS/s	
DNL	0,38 LSB	0,32 LSB	0,27 LSB
INL	0,38 LSB	0,32 LSB	0,46 LSB
TN (rms)	0,48 mV	0,37 mV	0,32 mV
FPN (rms)	1,10 mV	0,90 mV	0,70 mV
Taille des pixels	$35{\times}35~\mu m^2$		
Tension d'alimentation	1,8 V		
Dissipation de puissance	200 µW	188 µW	200 µW

Table R.1: *Résumé des performances du microcircuit MIMADC*

zone de pixels limitée avec une consommation d'énergie très basse. Les résultats des tests ont démontré une bonne puissance ainsi que l'efficacité de la zone. Par conséquent, le CPS intégré avec les CAN au niveau des pixels est un choix potentiel pour les conceptions aux couches externes du détecteur de vertex de l'ILD.

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Introduction

In order to extend our understanding of the mysteries of universe, dedicated subatomic physics experiments are built. These experiments require reliable detectors to measure the products of the collision. The energy of the particles is measured by the calorimeters, and the momenta is provided by the tracking detector. Because the heavy quarks have a short lifetime of the order of picosecond, they can only be recognized by the tracks originating from the secondary decay vertices. This task is taken by the vertex detector (VTX) with high precision to be placed very close to the interaction point. This thesis aims to contribute to the development of a promising type of silicon pixel sensor—CMOS Pixel Sensor (CPS) —used to equip the vertex detector for the International Linear Collider (ILC).

The ILC is the next large experimental facility in high-energy physics, as a complement to the LHC (Large Hadron Collider at CERN). The prominent features of the ILC including the well-defined beam energy, polarised beams, clean operational background, enable a precise measurement to verify and extend the discoveries from the LHC. For instance, two experiments—ATLAS and CMS—belonging to the LHC have confirmed the existence of the Higgs boson at ~ 125 GeV/c^2. ILC can measure its properties precisely including the mass, spin, decay channels to further verify the identity. The functioning of the ILC will start from a centre-of-mass energy of 500 GeV together with a luminosity of 1.8×10^{34} cm^{-2}s^{-1}, and then finally upgrade to ~ 1 TeV. The total length of the ILC facility is ~ 31 km. The only interaction point is surrounded by one out of two detectors—International Large Detector (ILD) and Silicon Detector (SiD)—operated in a push-pull scheme to share the same luminosity. Both two detectors follow the Particle Flow Algorithm (FPA) to separate and measure the neutral particles in the calorimeter and the charged particles in the tracker. The main difference between them are that the tracker in the ILD is hybridized by a TPC and a silicon structure, but the SiD is realized by an all-silicon approach.

The ability of reconstructing the decay vertices of the short living particle relies on that the VTX has a highly precise measurement of the tracks of the charged particles in the vicinity of the interaction point. In order to reach an extraordinary spatial point resolution, the VTX is composed of a cylindrical concentric multi-layer structure and each layer exhibits a high spatial resolution. In addition, a low material budget is mandatory for each layer. The stringent operational condition also imposes requirements on the readout speed and radiation toler-

ance. Unfortunately, the requirements mentioned are generally in contradiction, which results in a challenge for the R&D of the VTX.

Two candidate geometries exist for the ILD-VTX: one with 5 single-sided layers meaning that only one side of each layer is equipped with the sensors, and the other one with 3 double-sided layers where both sides of each layer are mounted with independent sensors. Several sensor techniques are actively developed to adapt the requirements of ILD vertex detector. Among them, the CMOS pixel sensor (CPS) is a promising candidate. A series of CPS prototypes developed at the IPHC (Institut Pluridisciplinaire Hubert Curien, Strasbourg, France), called MIMOSA, has been verified in performances by the beam tests. The sensitive volume can be implemented together with the signal processing circuits on the same silicon substrate by the commercial CMOS process. A high density pixel structure ensures the sufficient spatial resolution. The CPS allows thinning to be suit for the low-mass application. The subject of this thesis is the development of CPS prototype dedicated to the outer layers of the ILD vertex detector.

The R&D of the sensors for the ILD-VTX is driven by the running constraints. There is a significant difference in the running constraints between the innermost layer and the outer layers, because of the gradient variation of the hit density related to the layer radius. In the innermost layer, the emphasis of design is given on the fast readout speed and high granularity. The CPS can benefit from the geometry of double-sided layers since one side is mounted by the high-segmented sensors for the high spatial resolution, and the other side is equipped with the sensors composed of the elongated pixels for the high readout speed. The priority of the sensors mounted on the outer layers is low power consumption due to the large coverage ratio of the sensitive area ($\sim$90%) in the VTX. Meanwhile, the low hit density allows for the use of larger dimension pixels and the slower readout speed. A relatively large pixel of 35×35 μm^2 is adopted to reduce the number of the columns, and further the power consumption. The loss of the spatial resolution is compensated by the signal being quantized by the 3-4 bits ADCs (Analog to Digital Converters) to reach an estimated spatial resolution of $\sim$3-4 μm. The first prototype sensor that targets the outer layers of ILD-VTX, called MIMOSA-31, had been designed before this thesis. It is composed of 48×64 pixels with a pitch of 35 μm, and the 4-bit column-parallel ADCs digitalizing the outputs from each column.

ADCs in the CPS provide an one-to-one corresponding relation between the collected charge quantity and the digital codes needed for positioning the incident particles. In the pixel sensors, the ADCs can be implemented at various levels including the chip-, column- and pixel-level. In comparison to the chip-level ADCs, the column-level ones present the advantage of a great relaxation in the conversion speed. However, the signal-to-noise ratio (SNR) is dramatically degraded because the weak analog outputs from the pixels have to drive the long column-bus, and this becomes even worse for a large scale sensor. Moreover, the analog buffers with the strong driving ability for driving the large parasitic capacitances distributed on the column wires result in a significant power consumption.

The reason of the aforementioned problems lies in that the analog outputs of sensors are not only sensitive to noise, but also difficult to be further processed. The concept of digital pixel sensor (DPS) that features all-digital output directly from pixels was proposed. The digitalized outputs are immune to noise and easy to be driven, which provide superior performances on SNR and power consumption. In DPS, complex signal processing circuits are integrated within pixels to realize more smart functions. The in-pixel digitalization also allows the parallel pixel operation to reach a high readout speed. In addition, less column circuits lead to less insensitive area existing in the sensor. The pixel-level ADC is the key block in building the DPS. The main challenge in design is to integrate a complete ADC within an area-limited pixel. The complex pixel circuit also asks for a sophisticated layout to reduce the crosstalk among the neighboring blocks. Those challenges will be studied in this work.

The sensors for the outer layers of VTX have the priorities on SNR and power consumption, which will benefit from the approach of integrating CPS with pixel-level ADC. Meanwhile, the large pixel size is also in favour of the complex layout. In this thesis, a prototype sensor, called MIMADC, has been implemented by a 0.18 μm CIS process, aiming to the application of the outer layer VTX in the ILD. The target of this sensor is to verify the feasibility of the CPS integrated with pixel-level ADCs. Three matrices are included in this prototype but with two different types of pixel-level ADCs: one with successive approximation register (SAR) ADCs, and the other two with single-slope (SS) ADCs. All of them feature a same pixel size of 35×35 μm^2, a resolution of 3-bit, and a power consumption of $\sim$200 μW/pixel. The matrix with the SAR ADCs has the scale of 16×16, and is read out in the rolling shutter method with the conversion time of 160 ns. The matrices integrated with SS ADCs include 16×18 pixels, but with a little longer conversion time of 180 ns.

In this thesis, we study the feasibility of employing pixel-level ADCs within CPS to meet the requirements of the outer layer VTX in the ILD. A prototype sensor has been implemented to verify the concept of using SAR ADCs and SS ADCs for the in-pixel integration.

This thesis is organized as follows:

- In chapter 1, the physics motivation of the ILC is introduced. Then the ILC project and required detectors are briefly presented. As an important subdetector, ILD, its structure and specification are reviewed in order to better understand the requirements of the ILD vertex detector.
- In chapter 2, the detector techniques dedicated to the ILD-VTX are discussed. In the beginning, the basic physics of charge generation and collection are explained. The issue about the silicon damage due to the particle irradiation is discussed. In the second part, several detector techniques are presented as the candidates to the VTX. The discussion focuses on the knowledge of the CPS including the principle, basic architecture and development status. Then, a detailed discussion on a typical CPS—MIMOSA-26 is presented. Lastly, we address the conceptual considerations for the ILD-VTX based on the CPS.

- In chapter 3, we study the ADCs used in the CPS at the system-level. The basic performances and the typical structures of ADCs are briefly introduced. The pros and cons of chip-, column- and pixel-level ADCs are analyzed. The results show that pixel-level ADCs features some merits that are attractive for the sensors used in the outer layers of VTX. The selection of the process and the ADC type are also studied. Finally, a report on the state-of-the-art of the pixel-level ADCs in pixel sensors is provided.

- In chapter 4 and 5, the design of the prototype sensor − MIMADC is discussed in detail. Chapter 4 focuses on the studies about the implementation of the pixel-level SAR ADCs within a small size pixel. The discussion starts from the sensor architecture, circuit design, to the layout implementation, and focuses especially on the compactness of the circuit and the noise analysis. Chapter 5 addresses the design with the SS ADCs. Besides the pixel design, some peripheral circuits including the adaptive ramp generator and bandgap are also covered.

- In chapter 6, the detailed experiments for the MIMADC prototype are presented. A comparison of the pixel-level ADCs characteristics with the previous column-level ADCs is provided.

- In the conclusion, the results obtained in this thesis will be summarized and the main conclusions will be presented. At the end, the perspectives for the CPS integrated with pixel-level ADCs are addressed.

1

The ILC and ILD

The goal of high-energy physics is to understand the fundamental constituents of matter and the forces between them. The laws governing the particles and their interactions were summed up in a quantum gauge field theory, called the Standard Model. This model describes matter made of six types of quarks and six types of leptons, interacting with each other through strong, weak and electromagnetic interactions. Quarks are grouped in pairs, up (u) and down (d), charm (c) and strange (s), and top (t) and bottom (b). Leptons are also grouped in pairs, electron and electron neutrino, muon and muon neutrino, and tau and tau neutrino. The forces carriers, including photon, Z boson, W boson and gluon, make up the third section of the Standard Model. They transmit three of the four fundamental forces through which matter interacts. The Standard Model has been verified by numerous high-precision experiments over a wide range of energies. Nevertheless, it is not yet a complete theory, for example it does not describe "dark matter" that makes up 80% of the mass in the universe, and it does not include gravitation. In the Standard Model, the quarks, leptons, and bosons acquire their mass from the spontaneous symmetry breaking of the electroweak symmetry through a hypothetical field, called the Higgs field. The problem of the Higgs field is likely to be connected to the questions about the matter content of the universe. A way to prove the existence of the Higgs field and to study its interactions is to find and study the quantum of this field, called the Higgs boson. In 2012, the LHC (Large Hadron Collider) at CERN announced the discovery of the "Higgs-like particle" near 125 GeV. After the discovery of the Higgs boson, it becomes natural to study its properties with great precision. The International Linear Collider (ILC) was designed to study in detail the Higgs boson and search for new discoveries beyond the Standard Model.

The ILC is a proposed electron-positron linear collider, which will produce collisions at a centre-of-mass energy ranging up to 1 TeV and cover a wide range of physics programs. To facilitate its physics goal, it is essential to develop efficient collider detectors. And one of the most important ingredients of such complex is to construct a fine pitch, low-mass, high precision pixel vertex detector as close to the interaction point as possible. Such a vertex detector is motivated by the identification of the flavour of the particles containing heavy (b and c) quarks which originate from the electron-positron collisions, and decay very close to

the interaction point. The development of the vertex detector for the ILC is the main topic of this thesis.

This chapter is intended to provide an introductory overview of the ILC, including its major physical programs and the baseline accelerator parameters. The main features of the ILD (International Linear Detector), one of the proposed detectors for the ILC, are reviewed.

1.1 The International Linear Collider

After the Higgs discovery, many more years of follow-up research will be needed to measure the properties of the Higgs particle with unprecedented precision. While the LHC and its high luminosity upgrade will certainly improve its precision on Higgs property measurements, it has been appreciated that an electron-positron collider operating at the centre-of-mass energy range of 250 GeV to 1 TeV would be an ideal instrument for the precise study of the Higgs particle. The ILC, a high luminosity linear electron-positron collider, will be an ideal candidate. As a lepton collider, the ILC will provide much cleaner events than a hadron collider. At the ILC, each bunch crossing produces a few hadrons in the final state and a large number of secondary electron-positron pairs, but these are mainly confined to small volume within 1 cm of the beam. Because of the much more benign environment at the ILC than at the LHC, the tracking detectors of the ILC can be made as thin as technically feasible. At the ILC, both the vertex detector and the calorimeter can be placed much closer to the interaction point, leading to excellent b, charm and τ tagging capabilities. In addition, the reduced pileup from multiple collisions in each beam crossing much facilitates the event reconstruction at the ILC. The electron-positron environment thus provides a setting in which the basic high-energy collision can be measured with high precision.

1.1.1 Physics program

One of the advantages of a linear collider is its ability to operate, with only minor modification, at any energy within its range that might give the greatest physics potential. This flexibility allows the designers of the ILC to envision experimental programs at a series of energies well adapted to individual physics goal.

Table 1.1 lists the major physics processed to be studied at the ILC in the various stages of its program, and the full detail can be found in the Physics Volume of the ILC Technical Design Report [1]. The table indicates the various Standard Model reactions that will be accessed at increasing collider energies, from 90 GeV to 1000 GeV, and their physic motivations. For any new particle in the ILC energy range, the ILC offers a rich program to address its properties. The ILC experiments have the capability to measure the masses with high precision, determine the electroweak quantum numbers and measure any associated mixing angles and the decay branching ratios in a model-independent way.

Energy	Reaction	Physics Goal
91 GeV	$e^+e^- \rightarrow Z$	ultra-precision electroweak
160 GeV	$e^+e^- \rightarrow WW$	ultra-precision W mass
250 GeV	$e^+e^- \rightarrow Zh$	precision Higgs coupling
350-400 GeV	$e^+e^- \rightarrow t\bar{t}$	top quark mass and couplings
	$e^+e^- \rightarrow WW$	precision W couplings
	$e^+e^- \rightarrow \nu\bar{\nu}h$	precision Higgs couplings
500 GeV	$e^+e^- \rightarrow f\bar{f}$	precision search for Z'
	$e^+e^- \rightarrow t\bar{t}h$	Higgs couplings to top
	$e^+e^- \rightarrow Zhh$	Higgs self-coupling
	$e^+e^- \rightarrow \tilde{\chi}\tilde{\chi}$	search for supersymmetry
	$e^+e^- \rightarrow AH,\ H^+H^-$	search for extended Higgs states
700-1000 GeV	$e^+e^- \rightarrow \nu\bar{\nu}hh$	Higgs self-couplings
	$e^+e^- \rightarrow \nu\bar{\nu}VV$	composite Higgs sector
	$e^+e^- \rightarrow \nu\bar{\nu}t\bar{t}$	composite Higgs and top
	$e^+e^- \rightarrow \tilde{t}\tilde{t}^*$	search for supersymmetry

Table 1.1: *Major physics processes to be studied by the ILC, together with the lowest centre-of-mass energy at which they can be studied, from [1].*

1.1.2 Machine overview

The ILC, based on the 1.3 GHz superconducting radio-frequency (SCRF) accelerating technology, is designed to reach 200-500 GeV (extendable to 1 TeV) centre-of-mass energy with high luminosity. The collider design is the result of nearly twenty years of research and development. Figure 1.1 shows a schematic view of the overall layout of the ILC, indicating the location of the major sub-systems [1]:

- **electron source** — the polarised electron source is produced by a laser illuminating a strained GaAs photocathode in a DC gun;
- **positron source** — positrons are obtained from a beam of electron-positron pairs, which is generated by the high-energy photons transporting the high-energy electron beam through a helical undulator;
- **damping rings (DR)** — one electron ring and one positron ring, operating at a beam energy of 5 GeV in the baseline design, are housed in a common tunnel at the center of the ILC complex, with a circumference of 3.2 km;
- **main linacs** — two 11 km long main linacs are for electrons and positrons, utilising 1.3 GHz SCRF cavities; they are operating at an average gradient of 31.5 MV/m, with a pulse length of 1.65 ms;
- **ring to main linac (RTML)** — the layout of the RTML systems are identical for both electrons and positrons, consisting of a 5 GeV transport line, betatron- and energy-
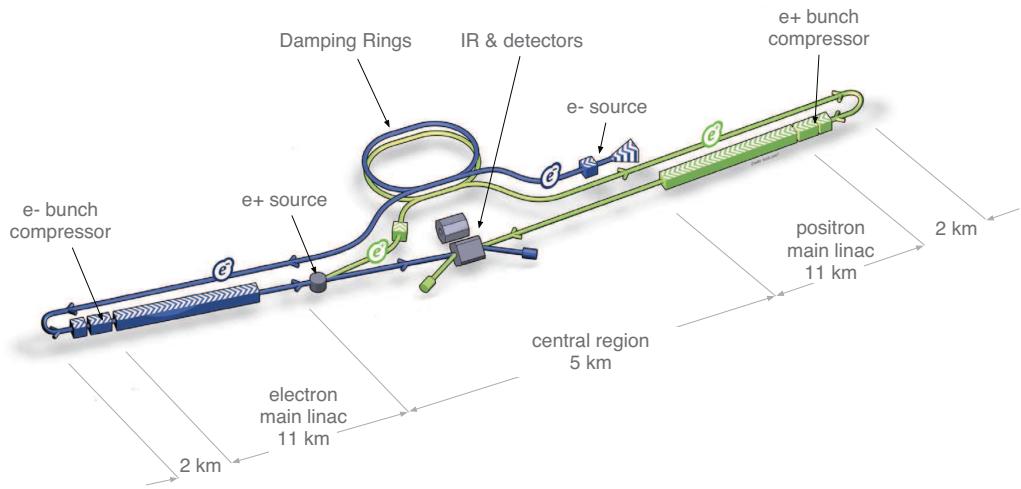
Figure 1.1: *Schematic layout of the ILC, indicating all the major subsystems [2].*

collimation systems, spin rotators, and a two stage bunch compressor system prior to injection into the main linac;

- **beam delivery system (BDS)** — it is responsible for bringing the two beams into collision with a 14 mrad crossing angle, at a single interaction point which can be shared by two detectors (in a so-called "push-pull" configuration).

The top-level parameters for the baseline design have been optimized to provide the maximum achievable physics performances with a relatively low risk and minimum cost [3]. Some of the ILC baseline parameters are summarized in Table 1.2.

Centre-of-mass energy	GeV	250	350	500
Luminosity	$\times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$	0.75	1.0	1.8
Luminosity pulse repetition rate	Hz	5	5	5
Bunch population	$\times 10^{10}$	2	2	2
Number of bunches		1312	1312	1312
Linac bunch interval	ns	554	554	554
RMS bunch length	μm	300	300	300
RMS horizontal beam size at IP	nm	729	684	474
RMS vertical beam size at IP	nm	7.7	5.9	5.9

Table 1.2: *ILC 250-500 GeV baseline parameters, form [3].*

Beam-induced backgrounds   The rate for the events from the high-energy electron-positron interactions are low, therefore the unwanted interactions are crucial in the ILC. The most important sources are machine-induced backgrounds, in which a major contribution is electron-positron pairs created by scattering of beamstrahlung photons.

As two opposite bunches approach each other, they exert a significant electromagnetic force. The individual particles are accelerated towards the center of the oncoming bunches. This mutual attraction known as the pinch effect has both pros and cons [4]. On one hand, the pinch effect reduces the bunch sizes and thereby increases the luminosity by a factor of two. On the other hand, the deflection of particles by the change of the opposite bunch causes the so-called beamstrahlung photons to degrade the center-of-mass energy for interactions. The electron-positron pairs created by the beamstrahlung photons in the vicinity of the interaction point are the dominant source of beam-induced backgrounds in the detector.
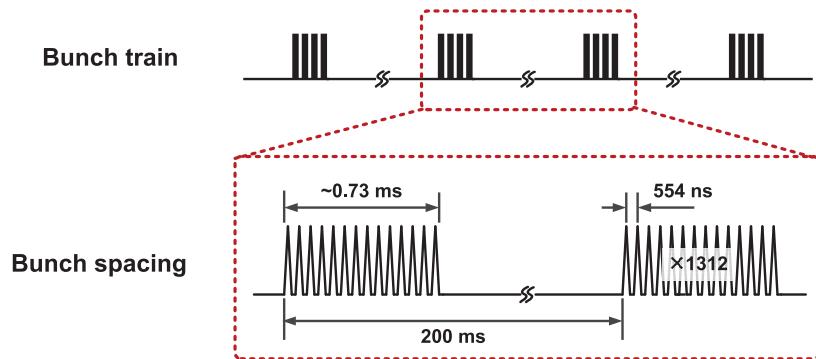
Figure 1.2: Bunch structure of the ILC.

Bunch structure   The bunch structure of the ILC is illustrated in Fig. 1.2. Each bunch train consists of 1312 bunches at a repetition rate of 5 Hz [3]. Various bunches are separated by 554 ns time intervals, translating into a ∼0.73 ms duration for each bunch train. The ILC time structure with a long duty cycle permits power pulsing which is a desirable feature for the detector subsystems to significantly reduce the heat dissipation. The benign operational conditions at ILC, i.e., less event rate and modest backgrounds, result in relatively low hit occupancies, allowing the construction of high precision detectors.

1.2 ILD

The ILC has been designed to enable two experimental detectors to sharing one interaction region using a push-pull approach [2]. The independent operation of the two experiments is expected to provide complementary strengths, cross-checking and confirmation of results, reliability, insurance against mishaps, competition between collaborations, as well as increased number of involved scientific personnel. In August 2009, the International Detector Advisory Group (IDAG) approved that the ILD (International Linear Detector) and the SiD (Silicon Detector) as the two detector options in the ILC. SiD is a compact, cost-constrained detector made possible by silicon tracking in a 5 Tesla magnetic field. ILD is a large detector with robust and stable performance over a wide range of energies.

1.2.1 ILD concept overview

The ILD concept has been designed as a multi-purpose detector, shown in Fig. 1.3. As the most adjacent detector, the vertex detector (VTX) consists of barrel geometry multi-layers surrounding the interaction point. The highly pixelated silicon based VTX features a superiority in granularity. A tracking system based on silicon micro-strip sensors surrounding the VTX is designed to improve the tracking performance. Outside the VTX is a large volume time projection chamber (TPC) optimized for high three-dimension point resolution and minimum material in the field cage and in the end-plate. This gas-filled detector is the most distinction from the SiD which is a all-silicon detector. Followed the tracking system is the calorimeter system including the highly segmented electromagnetic calorimeter (ECAL) and the hadronic calorimeter (HCAL). At very forward angles, a system of additional calorimeter detectors including LumiCAL, BeamCAL and LHCAL are foreseen to contribute the coverage to the ECAL and the HCAL. The whole calorimeter system is filled in a 3.5 Tesla magnetic field created by a large volume superconducting coil. An iron yoke, following the coil instrumented with scintillator strips or resistive plate chambers, returns the magnetic field and also serves as a muon detector. The detailed descriptions of the sub-detectors of the ILD are presented in the following sections.

(a)   (b)
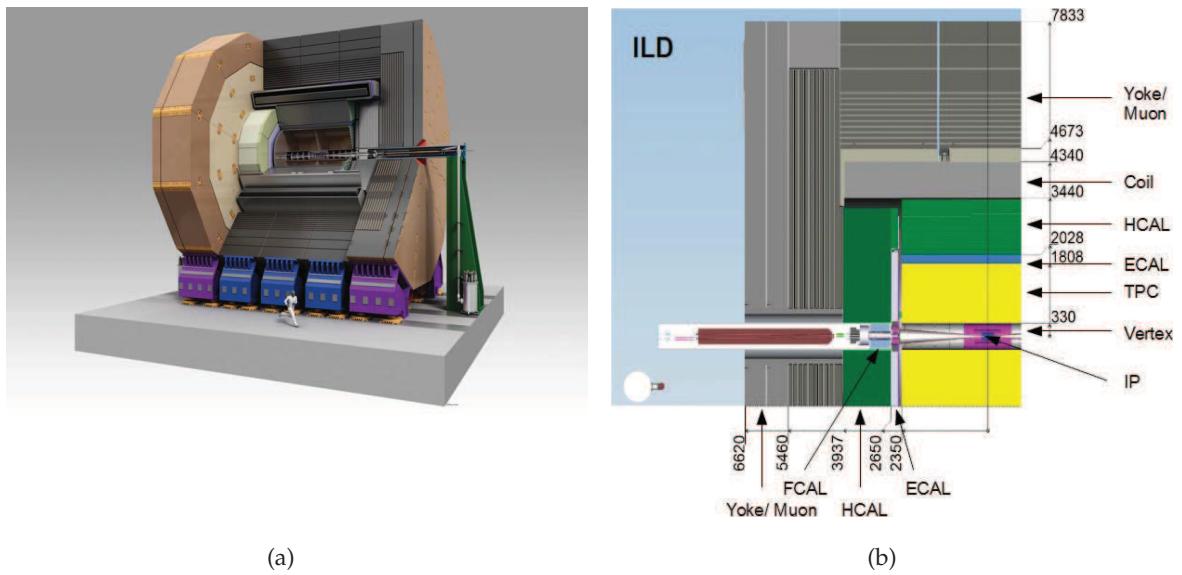
Figure 1.3: *(a) Cut-away view and (b) quadrant view of the ILD, where the interaction point is in the lower right. Dimensions are in millimeter.*

1.2.2 ILD vertex detector

The ILD vertex detector system surrounding the interaction point plays a critical role in the ILD. It is required to match some challenging physics processes of importance at the ILC,

namely multi-jet processes in which the flavors and sign of the quark charge of some of the low energy b and c-jets needs to be determined.

Requirements   The impact parameter resolution, σ_{ip}, is a figure of merit to characterize the detector. It is described by the usual gaussian expression:

$$\sigma_{ip}^2 = a \oplus b/p \cdot \sin^{2/3}\theta \, , \tag{1.1}$$

where p is the particle momentum and θ is the polar angle. The parameter a is related to the single point resolution. The parameter b depends on the distance of the innermost layer to the interaction point and on the material budget. According to the optimized results, a and b are requested to below 5 µm and 10 µm·GeV/c respectively. To achieve such a high resolution ($\sigma_{ip}^2 < 5 \oplus 10/p \cdot \sin^{2/3}\theta$), the ILD vertex detector should comply with the following specifications: a spatial resolution near the interaction point less than 3 µm; the innermost layer located at a radius of ~16 mm; a material budget below ~$0.15X_0$ per layer; a pixel occupancy not exceeding a few percent.

In order to minimize the material budget of the cooling system inside the detector sensitive volume, the power consumption of the ILD vertex detector should be low enough. Power saving was greatly simplified by the ILC time structure. The frequency of bunch train is 5 Hz, translating into a period of 200 ms. Each bunch train lasts for 0.7 ms, consisting of 1312 bunches with an interval of 554 ns. This very sparse filling allows power for many of the vertex detector to be switched off between bunch trains (~199 ms). This strategy greatly reduces the heat load and the need for cooling. In addition, the bunch train interval provides the possible time slot for the data readout.

The required radiation tolerance is driven by the beam related background, which is expected to affect primarily the innermost layer. The requirements for the total ionising dose and the fluence are about 1 kGy and 10^{11} n_{eq}/cm^2 per annum, respectively. These values are obtained by assuming that neutrons backscattered from the beam dump are shielded well enough to add a minor contribution to the overall radiation load [5].

Baseline design   The baseline design of the ILD vertex detector (called VTX-DL) comprises three concentric layers of double-side ladders as depicted in Fig. 1.4(a). The pixel sensors are installed on both sides of each ladder with ~2 mm apart. A traversing particle crossing the detector will generate six impact points for the track reconstruction. To minimize the occupancy from background hits, the first superlayer is only half as long as the outer two. The material budget of each ladder amounts to ~0.3% X_0, equivalent to 0.15% X_0/layer.

The parameters of the baseline design are illustrated in Table 1.3, having been optimized for point resolution and minimum material thickness. The radii covered by the six layers range from 16 mm to 60 mm. The spatial resolution and readout times shown in the Table 1.3 are for the simulated CMOS option.

	R (mm)	$|z|$ (mm)	$|\cos\theta|$ (mm)	σ_{sp} (µm)	Readout time (µs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6.0	10
Layer 3	37	125	0.96	4.0	100
Layer 4	39	125	0.95	4.0	100
Layer 5	58	125	0.91	4.0	100
Layer 6	60	125	0.90	4.0	100

Table 1.3: *Vertex detector baseline design parameters, from [5]. R is the radii of the multi-layer sensor. $|z|$ is the length in z-axis. $|\cos\theta|$ is the angular coverage, and σ_{sp} is the required spatial resolution.*

An alternative geometry (called VTX-SL) as depicted in Fig. 1.4(b) is based on five equally spaced single-sided layers, with radii ranging from 15 mm to 60 mm.

(a)   (b)
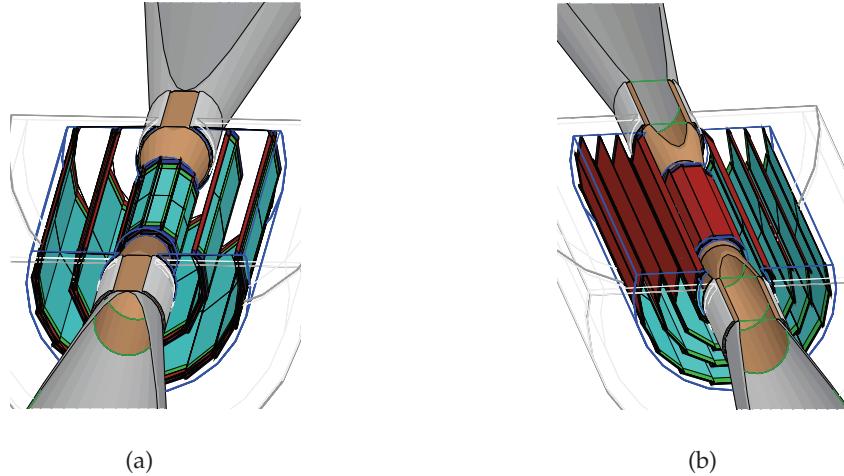
Figure 1.4: *Two options for the ILD vertex detector geometries: (a) three-double-layer option (VTX-DL); (b) five-single-layer option (VTX-SL).*

1.2.3 Time Projection Chamber

The Time Projection Chamber (TPC) as a main tracking detector, provides a high accurate momentum resolution. The configuration of the TPC is a central barrel frame with the inner radius of 329 mm and the outer radius of 1808 mm. The angle coverage is required to be up to $\cos\theta \sim 0.98$. The TPC consists of a large gas-filled sensitive volume. A central cathode divides the volume into two halves, and each side has an anode connected to the readout circuitry by the pads. A high potential is applied between the cathode and anode to generate a high electric field. A charged particle traversing the gaseous volume will ionize the atoms of the gas mixture along its trajectory. The released electrons drift in the electric field towards

the anode and then are read out by the circuitry. By interpolating the signal collected on the segmented pads, the track of the charged particle can be reconstructed. The TPC provides particle identification capability based on the specific energy loss dE/dx. In addition, a high magnetic field is sent paralleled to the electric field. So the injected charged particle will be bent on a spiral track due to the Lorentz force. Referencing the different spiral tracks, the momentum of the particles can be measured.

There are many differences between the gas-based TPC and the silicon-based detector, just like the VTX. Comparing to the fine granularity of the vertex detector, TPC can only provide a moderate spatial resolution with the $r\phi \leqslant 100$ μm and rz ~ 500 μm. This can be compensated by that up to 224 points per track generated in the three-dimensional space for continuous tracking. The TPC features a low material budget that ~ 0.05 X_0 in the barrel volume and less than 0.25 X_0 in the endcaps. A strong magnetic field of 3.5 Tesla is needed to guarantee good momentum resolution and to suppress backgrounds.

1.2.4 Silicon tracking system

The silicon tracking system, as an auxiliary silicon system to complement the track reconstruction capability of the TPC and the VTX, includes four sub-detectors: two barrel components, the Silicon Inner Tracker (SIT) and the Silicon External Track (SET), the End-cap Tracking Detector (ETD) and the Forward Tracking Detector (FTD).

- **SIT** : It is equipped with layers made each of two single-sided silicon strip layers placed by a small angle with respect to each other. Such layers are also called false double-sided layers. The baseline microstrip sensor for the false double-sided layers has an area of 10×10 cm^2, with 50 μm pitch. The SIT is composed of two such cylindrical false double-sided layers, at radii of 153 mm and 300 mm. The spatial resolution of the SIT is of 7 μm in R-ϕ and 50 μm in z. The SIT is placed in the radial gap between the vertex detector and the TPC to improve the linking efficiency between them. It improves also the momentum resolution and the reconstruction of low p_T charge particles as well as long lived stable particles.

- **SET** : The SET is located in the barrel part between the TPC and the external calorimeter (ECAL), including one false double-sided layer. The SET acts as the outermost layer in the central barrel and also improves the overall momentum resolution. The position resolution is of 7 μm in R-ϕ. A very precise time stamping is possible by combining the hits from the SIT and SET.

- **ETD** : The ETD equipped with the single-sided microstrip sensors, is positioned between the TPC end plate and the end-cap calorimeter system. It improves the momentum resolution for charged tracks with a reduced path in the TPC and the matching efficiency between the TPC tracks as the clusters shown in the EM calorimeter.

- **FTD** : The FTD consists of seven tracking disks installed between the beam pipe and the TPC. The first two disks are composed of silicon pixel detectors and the remains are

strip detectors. Their precise space points with a large lever arm are advantageous to good momentum resolution in the forward region. Both ETD and FTD ensure the full tracking hermeticity.

1.2.5 Calorimeter system

The task of the calorimeter system is to measure the energy of electrons, photons and jets, and then discriminate them. Particles interact with the calorimeter and deposit their energy in the calorimeter either via electromagnetic interactions (*electromagnetic calorimeter*) or via hadronic interactions (*hadronic calorimeter*). The deposited energy can be either measured in its entirety, requiring total containment of the particle shower or sampled. Typical calorimeters are segmented transversely to provide information of the direction and the deposited energy of the particle. Longitudinal segmentation can provide information of the identity of the particle based on the particle shower.

The calorimeter system in the ILD is comprised of a nearly cylindrical barrel system with two large end caps. Three sub-detectors, the Electromagnetic Calorimeter (ECAL), the Hadronic Calorimeter (HCAL) and the Forward Calorimeter (FCAL) are designed for the different goals. Both ECAL and HCAL are sampling calorimeters that consist of alternating layers of an absorber, a dense material used to degrade the energy of incident particle, and an active medium generating the detectable signal.

- **ECAL** : The ECAL is designed to identify photons in the presence of close-by particles and measure their energy. The electromagnetic calorimeter can be realized with tungsten as absorber material because of its small Moliere radius and large ratio of interaction length to radiation length. The active layers must be thin with a highly segmented read-out for granularity requirement. At present, two options are proposed to meet these requirements. The silicon-based option uses pin diodes with a pad size of 5×5 mm^2. This method features large areas, reliable and simple operation. An alternative option based on the scintillator strips of 45×5 mm^2 has merits in dynamic range, insensitivity to magnetic field and cost efficiency. In order to achieve an adequate energy resolution, the ECAL is longitudinally segmented into 30 layers. To optimize the pattern recognition performance, the active layers (either silicon diodes or scintillator) are segmented into cells with a lateral size of 5 mm.
- **HCAL** : The role of the HCAL is to sense the neutral hadron and measure their energy. Two options have been developed for the HCAL: one based on scintillator tiles with silicon photo-sensors and analog read-out electronics, and one based on gaseous devices with two-bit readout but finer transverse segmentation.
- **FCAL** : Two individual calorimeters, named LumiCal and BeamCal, are designed to coverage the forward region. The LumiCal will carry out the measurement of the luminosity with a high precision of better than 10^{-3} at 500 GeV energy. BeamCal will perform a bunch-by-bunch estimation of the luminosity and assist beam tuning when included

in a fast feedback system. LumiCal covers polar angles between 31 and 77 mrad and BeamCal between 5 and 40 mrad. An additional low angle hadron calorimeter LHCAL completes the coverage in the low polar angle range to supplement the LumiCal. Both LumiCal and BeamCal ask for a fast readout and the latter requires radiation hard sensors as well.

1.2.6 ILD outer detector

The basic layout of the ILD has followed the strategy of tracking in a magnetic field. A nominal magnetic field of 3.5 Tesla is therefore required for the TPC with a high homogeneity, and the solenoidal central field can reach up to 4 Tesla. A magnet system consists of a superconducting solenoid coil, an anti-DID (anti-Detector Integrated Dipol), and an iron yoke.

The ILD coil with the length of 7.35 m is composed of three parts, that each one with 2.45 m. The superconducting cables with the electrical stabilized and mechanically reinforced, are operated in the temperature of 1.93 K. The anti-DID field is generated in the outside of the solenoidal coil for the reduction of the beam background in the VTX and TPC.

A barrel iron yoke together with two end caps is installed outside the coil system, to provide a magnetic flux return path and limit the outside stray fields to an acceptable value. It is also equipped with the muon detectors and tail catching of hadronic showers for the supplement detection. The yoke is also used as the mechanical structure for the ILD system.

1.3 Summary

This chapter begins with an explanation why the next high energy physics collider should be a linear lepton one. It then briefly introduces the ILC experiment and its physical goals. To arrive at the expected physics programs, the ILC requires significant advances in detector performances. The ILD is one of the two proposed ILC detectors. The tracking system of the ILD concept, especially the vertex detector, are mainly discussed, as it is the main topic of this thesis. Fine pitch, low-mass pixel vertex detectors are demanded to provide superior impact parameter resolution and excellent track reconstruction capability. Consequently, a material budget below $0.15\% X_0$ per layer, a spatial resolution near the interaction point better than 3 μm, a first layer located at a radius of $\sim$1.6 cm, and a pixel occupancy not exceeding a few percent, are desired for the ILD vertex detector. Several pixel sensor technologies have been shown to have the potential of meeting the detector requirements or to come close to them, as described in the next chapter. Among those vertex technologies, the CMOS Pixel Sensors (CPS), featuring high density sensing node lattice, flexibility and cost effective, are particularly attractive. Chapter 2 will present a detailed discussion on the CPS, concerning their principle of operation, the basic architectures and the conceptual considerations for the ILD vertex detector.

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2

CMOS Pixel Sensors for ILD Vertex Detector

Silicon is a semiconductor material that is widely used for the tracking of ionizing particles, including vertex detector applications. To fulfill the requirements of the future linear collider, several sensor technologies are under development. CMOS pixel sensors (CPS) discussed in this work are an example of monolithic detectors originally developed for tracking detectors in high energy physics. This section starts with an introduction on the principle of operation of silicon detectors. The potential sensor technologies adapted to the ILD vertex detector are reviewed, followed by a discussion on a possible configuration based on CPS.

2.1 The detection principle of silicon detectors

At the beginning of 1960s, silicon was used in radiation detection applications to replace gaseous detectors, marked as a revolution in experimental techniques of particle physics [1]. The moderate band gap energy of silicon, ~1.2 eV, is neither excessively high to allow the abundant production of charge carriers by ionizing particles, nor too low to avoid a large leakage current from electron-hole pair generation. Another reason of using silicon in particle detectors is the fact that it can be cheaply available in large quantities and manufactured by the well-developed integrated circuit technologies based on silicon. Silicon detectors offer good energy and excellent position resolutions, and therefore are particularly attractive for tracking.

2.1.1 Energy deposition by charge particles

The basis of particle detection is that as soon as particles interact with the sensor materials, a part of energy is lost and transferred to an electron-hole pair which is detectable for electronics. The stopping power defined by the energy loss per unit path length in silicon, is widely used for constructing sensor, given by the Bethe-Bloch formula:

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_ec^2\beta^2\gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right]. \tag{2.1}$$

The following list gives an explanation of all variables:

z – charge of the incident particle in units of elementary charge;

Z, A – atomic number and mass of the absorber;

m_e – electron mass, $m_e c^2 = 0.510$ MeV;

r_e – classical electron radius, $r_e = 2.817 \times 10^{-15}$ m;

N_A – Avogadro's number, $N_A = 6.022 \times 10^{23}$ mol^{-1};

I – mean excitation energy in units of eV;

β – velocity of the particle in units of speed of light, $\beta = v/c$;

γ – Lorentz factor, $\gamma = 1/\sqrt{1-\beta^2}$;

$\delta(\beta\gamma)$ – density effect correction to ionization energy loss;

T_{max} – maximum kinetic energy imparted to a free electron in a single collision;

$K/A = 4\pi N_A r_e^2 m_e c^2 / A = 0.307$ MeV g^{-1}cm^2 for $A = 1$ g mol^{-1}.

The Bethe-Bloch formula is only valid in the region of $0.1 \lesssim \beta\gamma \lesssim 1000$. At the low energy, Eq. (2.1) is dominated by the $1/\beta^2$ term. Thus the stopping power is reduced with increasing energy, and will reach a minimum value as a particle velocity β is ~0.96 ($\beta\gamma = 3$). With a further higher energy, the stopping power rises slowly and saturates eventually. Therefore, a particle featuring a minimum value in the Bethe-Bloch formula, meaning a least energy loss in the material, is termed as a Minimum Ionizing Particle (MIP). Every detector must keep its noise well below this energy to be able to detect these MIPs. For a MIP, the most probable number of electron-hole pairs generated in 1 µm of silicon amounts to ~76.

2.1.2 Silicon detector physics

2.1.2.1 P-N junction

Intrinsic silicon is pure with the negligible impurities, and features the same quantities in both electrons and holes. The properties of silicon can be adjusted by doping other additional elements within the intrinsic material. Introduction of donors (e.g. As, P, or Sb) in intrinsic silicon adds electrons to form n-type silicon. Similarly, acceptors (e.g. Al, Ga, or Sn) lead to holes to form p-type silicon. Both of n- and p-type materials are called extrinsic semiconductors. The external doping can introduce the additional energy levels in material. Hence, by regulating doping types and concentrations, the electrical properties of silicon can be changed on purpose.

As the most essential structure in semiconductor devices, p-n junctions are obtained by joining together two extrinsic semiconductors with the opposite doping types. Diodes are the most simply realized by p-n junctions. As a two-terminal devices, the diode has the feature that the current can be conducted only in one direction under the condition of the external voltage bias. To characterize diodes, the analysis start from a diode under the thermal equilibrium condition. Assuming initially two semiconductors, one is n-type and the other one is p-type, are in the thermal equilibrium condition with the homogeneously distributions of
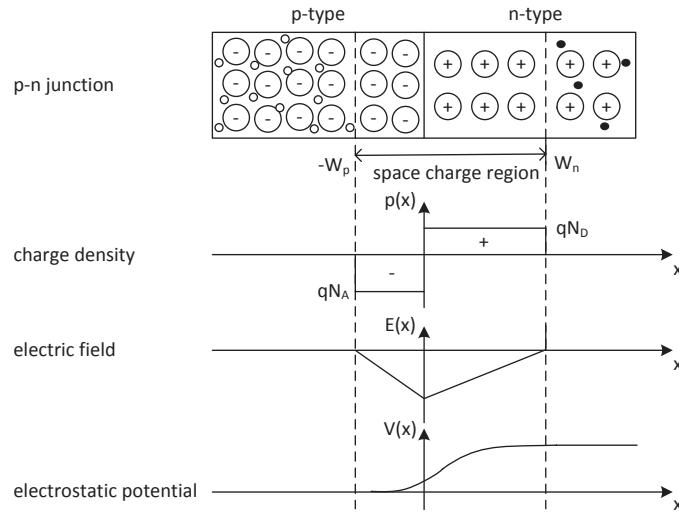
Figure 2.1: *Approximation of an abrupt p-n junction: depletion region, space charge density, electric field distribution, and electrostatic potential distribution.*

electrons and holes. As soon as two semiconductors are connected, the difference of concentrations leads to electrons diffusing from n-type to p-type silicon, while the holes diffuse in the reverse direction. The remained ionized donors in n-type silicon and the ionized acceptors in p-type silicon will create an electric field that counteracts the diffusion between electrons and holes. When the diffusion is counteracted by the electric field, the diode is in dynamic thermal equilibrium. A neutral region free of the mobile carriers is formed to be called depletion region. An abrupt p-n junction is illustrated in Fig. 2.1, where the doping concentration of donors and acceptors are N_D and N_A respectively, and the electrostatic potential difference across the depletion region at thermal equilibrium is referred to as the built-in potential:

$$V_b = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \, , \tag{2.2}$$

where k is the Boltzmann constant, T is the absolute temperature, $q = 1.6 \times 10^{-19}$ C is the elementary charge, and n_i is the intrinsic carrier density.

The width of the depletion region is expressed as

$$
\begin{aligned}
W &= x_n + x_p \\
&= \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_b} \, ,
\end{aligned}
\tag{2.3}
$$

where ε_{si} and ε_0 stand for the dielectric constants of silicon and the permittivity of vacuum, respectively. The width of the depleted region is inversely proportional to the square root of the doping concentration. In the case of the asymmetric doping, assuming $N_A \gg N_D$, Eq. (2.3)

can be simplified to

$$W = x_n$$

$$= \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{qN_D}V_b}\ . \tag{2.4}$$

As indicated in Eq. (2.4), the depletion region in the p-type silicon is extended mostly to the n-type silicon.

The above results are based on the assumption of thermal equilibrium with no external voltage. If an external forward voltage V is applied to the terminals of the diode, the build-in voltages shown in Eqs. (2.3) and (2.4) are reduced from V_b to $(V_b - V)$, resulting in a shrink of the depletion region.

The depletion region plays a very important role in the detection of charged particles. In this region, the electron-hole pairs generated by the incident charge particles are swept away by the build-in electric field toward the terminals of the diode. Applying a large reverse bias is an effective method to widen the depletion region. Typically, a 60 V to 100 V reverse bias voltage can deplete a lightly doped bulk silicon ($\sim$10 kΩ resistivity) with a thickness of 300 μm. However, the junction breakdown voltage limits the maximum allowable reverse bias voltage.

The depletion region sandwiched by the n- and p-type silicon layers, acts as a parallel plate capacitor with the value of

$$C_j = \frac{\varepsilon_{Si}\varepsilon_0 A}{W_j} = A\sqrt{\frac{q\varepsilon_{Si}\varepsilon_0 N_b}{2(V_B - V_b)}}\ , \tag{2.5}$$

where A is the surface area of the junction. A large depleted region leads to a large sensitive volume and a small capacitor at the sensing node, both of which translate into a high signal-to-noise ratio.

2.1.2.2 Charge collection

In silicon detectors, the electron-hole pairs generated by the incident charged particles are collected by electrodes. The motion of these charged carriers is controlled by the built-in electric field (drift) and the inhomogeneous charge carriers' distribution (diffusion). Both of the mechanisms influence the charge collection.

In thermal equilibrium state, free charge carriers have a random movement with the energy of $3/2\ \kappa T$, where κ is the Boltzmann constant, and T is the Kelvin temperature. As soon as an electric field is applied, the charge carriers are accelerated in parallel with this field. Within a low electric field (E), the drift velocities of electrons (v_n) and holes (v_p) are proportional to the

strength of the electric field as

$$v_n = -\mu_n E \, ,$$
$$v_p = -\mu_p E \, . \tag{2.6}$$

The μ_n (μ_p) is the charge carrier mobility, which is approximately 1500 cm^2/(Vs) for electrons and 500 cm^2/(Vs) for holes at room temperature. When the electric field is higher than $\sim$1 V/μm, the mobility starts to decrease, and finally the drift velocity is saturated at the field of 10 V/μm.

The inhomogeneous distribution of charge carriers or doping concentration leads to a gradient of the carrier concentration. With no electric field, the charge carriers will diffuse from the high density region to the low one, resulting in diffusion currents, which can be described by the diffusion equations as

$$F_n = -D_n \nabla n \, ,$$
$$F_p = -D_p \nabla p \, . \tag{2.7}$$

These equations describe the flux of charge carrier F_n (F_p) in the density gradient ∇n (∇p) and diffusion constant D_n (D_p).

The current densities due to both drift and diffusion are

$$J_n = q\mu_n nE + qD_n \nabla n \, ,$$
$$J_p = q\mu_p pE + qD_p \nabla p \, . \tag{2.8}$$

The principle of silicon detectors relies on collecting the charges from incident particles. The fast signal response and the high charge collection efficiency are important. In depletion region, drift is the main mechanism in the motion of charge carriers. Compared with diffusion, drift is more rapid and has less probability of charge trapping. Consequently, full-depleted silicon detectors are favored by particle detection. However, the use of fully depleted structures are generally restricted by operational circumstance. As described in Eq. (2.3), the width of depletion region is proportional to the square root of the reverse biased voltage. To deplete fully a silicon, an external high voltage is required. However, this high voltage is generally unavailable in the standard CMOS process due to the limitation in breakdown voltage. Moreover, the additional high voltage distributed to each sensor complicates the design of detectors. Therefore, partial depletion is common in silicon detectors, such as in CPS. In partially depleted silicon, drift is only available in the vicinity of the anode of diode. Since the impurities presented in the silicon bulk could trap charge carriers, the quantity of the collected charge depends on the carrier life time. The longer charge collection time gives rise to more loss of charge carriers. The different mechanisms in charge carriers collection influence charge collection time. In fully depleted detectors, charge collection time depends on the strength of electric field, while in partially depleted ones, diffusion constant and doping concentration

contributes mainly to charge collection time. Typically, a partially depleted, n-type silicon with a thickness of 300 μm and 10 kΩ·cm resistance value features the charge collection time of ∼30–90 ns, three times longer than that for the fully depleted structure [2].

2.1.2.3 Signal current

Charges generated by the incident particles move toward the collecting electrodes under the mechanism of drift or diffusion, thereby leading to the variation of induced charges on the electrodes. These induced charges are converted to voltage signals, and then processed by circuitry. In fact, the induced current on electrodes is not due to the amount of charges collected by electrodes, but the instantaneous change of electrostatic flux on the surface of the electrodes.

The Shockley-Ramo theorem proposed a simplified method to estimate the induced charge [3]. The current i due to the moving charge q can be expressed as

$$i = -qv \cdot E_0(\chi) \, , \tag{2.9}$$

where v is the instantaneous velocity of the charge. The $E_0(\chi)$ represents the weighting potential and field at the instantaneous position x with the moving charge q, respectively. Since only the weighting field, which is independent with the charge q and the space charge, needs to be calculated, the current i is easily arrived at. The Shockley-Ramo theorem therefore can serve to predict the signal sensed by charge detectors.

2.1.3 Radiation damage

Silicon detectors and readout electronics are widely used in high energy physics experiments. It is the essential requirement that to ensure all the detectors and electronics well working under the high radiation flux during the life cycles. The detector, especially the vertex detector generally suffers the high radiation doses. In the ILD, the vertex detector needs to withstand the radiation fluence of $\sim 10^{11}$ n_{eq}/cm^2 (ionization dose ~ 100 kRad) at room temperature.

Radiation damages can be classified into bulk damages and surface damages. Bulk damages due to the displacement of atoms from their lattice sites, are generated by massive particles, such as neutrons, protons, and pions. Surface damages existing in oxide and its interface to silicon, are introduced by ionizing radiations. Thus, bulk damages have consequences on the performances of silicon detectors, while surface damages on those of readout electronics.

2.1.3.1 Bulk damage

Incident particles not only interact with electron clouds to generate electron-hole pairs, but also collide with the nuclei of the lattice atoms. Bulk damages are produced by the displace-

ment of primary knock-on atoms (PKAs) out of crystal lattices, thereby resulting in silicon interstitials and remained vacancices, termed as frankel pairs. Bulk damages manifest the following features:

Leakage current Radiation-induced defects introduce the deep energy levels in band gap, acting as generation–recombination centers, cause a leakage current to discharge the capacitors at the node of sensing diodes even though no particle traverses the sensor. The leakage current produces shot noise, which is a statistical fluctuation in the current. Moreover, high leakage current can lead to thermal runaway and unstable operational conditions. The density of leakage current is proportion to the particle fluence, and reduced exponentially with the decrease of temperature [4]. Thus the leakage current can be significantly reduced by operating the detector at low temperature.

Effective doping concentration Another important result due to the displacement damage is the change of the effective doping concentration N_{eff} under the irradiation. In a non-irradiated condition, the N_{eff} of a silicon detector is determined by the dopant concentration in the material. The high energy radiation introduces additional deep energy levels in the band gap resulting in the acceptor levels. The induced acceptors accumulated in the depletion region compensate the original donor states, and thus decrease the N_{eff} in an n-type silicon continuously. The further radiation will lead the silicon into intrinsic, and then to p-type. Therefore, a high fluence can reverse the effective doping type in silicon detectors. Besides radiation fluence, the N_{eff} is also affected by annealing and anti-annealing procedures [5]. As indicated by Eq. (2.4), the change of the N_{eff} influences the volume of the depletion region, and thus the charge collection efficiency (CCE).

Trapping of charge The Electron-hole pairs created by incident particles can get trapped by radiation-induced defects. In addition, these trapped charges can be released successively due to the thermal excitation. If the releasing time is comparable to the signal collection time of detectors, an incomplete charge collection will exist.

2.1.3.2 Surface damage

Compared with bulk damages, surface damages are caused by the different mechanisms. In the bulk volumes of detectors, the materials are uniform with complete lattice structures and same band gaps. But at the surface of a detector, part of the surface is terminated by insulators, such as oxide, which are essential structures in Metal-Oxide-Semiconductor (MOS) transistors. Because of the difference of material crystal structures and band gaps between silicon and oxide, there exist high-density defects at the interface of them. The electron-hole pairs induced by the incident particles will be captured by these defects.

In oxide, electron mobility ($\mu_e \approx 20$ cm^2/(Vs)) is several orders higher than hole one ($\mu_h \approx 2\times10^{-5}$ cm^2/(Vs)) [5]. Radiation-induced electrons in oxide will be collected by any positively biased electrode close by. The remained holes which move slowly to the interface of the oxide and silicon may be captured by these defects, leading to the permanent holes accumulated in the oxide as well as the shift of the flat-band voltage of oxide. With respect to MOS transistors, radiation gives rise to the shifts of threshold voltages, and hence affects the operation of readout electronics.

In addition, the radiation also generates the interface states leading to a surface generation current when the space charge region reaches the surfaces. This contribution to the dark current is proportional to the not implanted surface area of the sensor.

2.1.3.3　Radiation-tolerant design

In high energy physics experiments, the detectors which are close to the interaction point demand to endure a high particle flux. This puts the high radiation tolerance requirements for these detectors and the associated readout electronics. As discussed in the previous sections, radiation-induced damages in both detectors and electronics have the different mechanisms that correspond to the various radiation-tolerant approaches. Some of them will be introduced briefly in this section.

The approaches to reduce the bulk damage focus on the optimizations of detector operation circumstances, detector structures, and materials.

- The low operation temperature is a direct method to improve radiation hardness. First, less leakage current not only reduces the loss of SNR for the detector, but also results in less power consumption during the thermal runaway. In addition, the low temperatures are capable to restrict both annealing and anti-annealing procedures.
- Radiation increases depletion voltage, equivalent to the reduction of depletion region and CCE. To compensate the loss of CCE, more reverse-biased voltage is applied. The multi-guard ring structure can prevent the breakdown at a high bias voltage.
- The enrichment of silicon bulk with the surplus oxygen shows a superior radiation hardness. Additionally, some alternative materials, such as SiC, GaN, and diamond, have been studied as the substrate material of detectors to endure an extremely high radiation circumstance (e.g. >10^{16} n$_{eq}$/cm^2) [4].

The surface damage due to the ionizing radiation shifts the threshold voltages of CMOS transistors, and then changes operational points, degrades the transconductance of amplifiers, or even causes a failure in circuits. Since the trapped holes can be tunnel out from the thin oxide layer, the shift of threshold voltage can restore significantly. In addition, fewer holes will be trapped in the oxide since the reduction of the oxide volume. Taking the advantage of the thin, high-quality oxide, the shift of threshold voltage almost cannot be observed for the irradiation fluence large than 300 kGy [6]. However, if the trapped charge density close to the
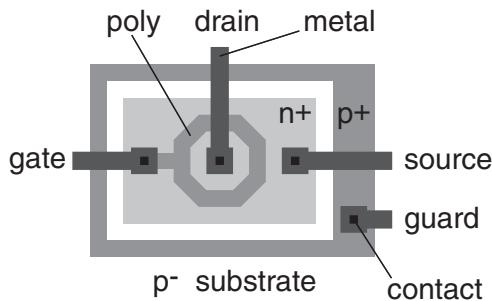
Figure 2.2:
Schematic layout of an NMOS transistor with enclosed polysilicon gate and p^+ guard ring [5].

interface is high enough to yield an inversion layer in the underneath thick field oxide, parasitic NMOS transistors may be induced with the threshold low enough to open up parasitic leakage current paths. To interrupt these current path, a design with enclosed NMOS devices separated by p^+-type guard rings of increased doping can improve the radiation-tolerance. Figure 2.2 is the principle of the radiation tolerance layout of an NMOS transistor with enclosed polysilicon gate and a p^+-type guard ring to protect against leakage currents between n-type wells in the design.

The radiation damage to the digital circuits is mainly due to the Single Event Effects (SEEs). When an incident particle passes though the substrate of devices, the deposited charges may change the status of the sensitive nodes resulting in a soft error. The SEEs can be classified into the Single Event Transient (SET), Single Event Upsets (SEU), and Single Event Latch-up (SEL). Some techniques, such as error correction and redundant circuits, have been devised to suppress the SEEs [7].

2.2 Candidate pixel technologies for ILD-VTX

The detector for particle physics started from the invention of the bubble chamber in 1960, and then promoted by the wire-chamber and the drift chamber in 1968 and 1975 respectively. However, these gaseous and liquid detectors feature a poor resolution ($\sim$50 μm) for particle tracking. In the early of 80's, the silicon micro strip detector was proposed to realize the spatial resolution in the order of 10 μm, allowing the identification of the secondary vertices and the precise measurement of the particles with short life time. Nevertheless, the medium spatial resolution, limited hit capacity and high material budget restrict its application in the detector near the interaction point. As another kind of silicon detectors, the pixel detector exhibits the unprecedented granularity that is very crucial to detect multiple tracks. Various pixel detectors have been proposed to match the physics goals and running conditions of the ILD-VTX. As presented in the ILC Technical Design Report (TDR), three sensor technology options are actively developed for the ILD vertex detector: Fine Pixel CCD (FPCCD) sensors, Depleted Field Effect Transistor (DEPFET) sensors, and CMOS Pixel Sensors (CPS) [8]. They have been shown to have the potential of meeting the detector requirements or to come close to them. Next, a brief review of the first two options are presented, followed by a comprehensive
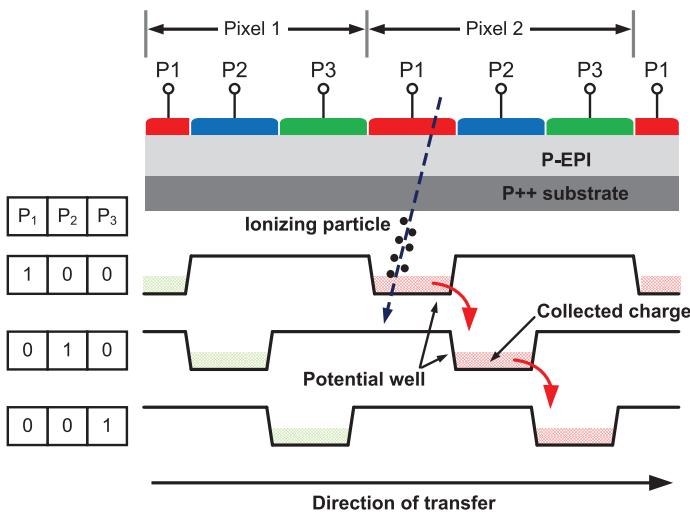
Figure 2.3:
Principle of a typical CCD. Within each pixel, three independent gates P1, P2 and P3 are driven by the appropriate voltage sequences. The charges generated by the incident particle are stored by the potential well, and then transferred along the column direction to the peripheral readout circuits.

discussion on CPS.

2.2.1 Fine Pixel CCD (FPCCD)

Charge coupled devices (CCDs), invented by Willard S. Boyle and George E. Smith at Bell Laboratories in 1969, are widely used in visible-light photographer, astronomy application and particle detection.

Figure 2.3 is the cross-section of a typical CCD. Within each pixel, three separated gates are controlled by the independent clock signals. When a positive voltage is applied to the gate P1, the silicon below is depleted that acts as a MOS capacitor. The electrons that are generated by incident particles are collected under the gate P1 and stored in the associated MOS capacitor. The holes due to the incident particles are dumped to the substrate. The other two gates P2 and P3 create the potential wells that restrict the diffusion of the charge below P1 to the neighboring area. In the next clock phase, the potential well moves from the silicon below P1 to P2. The charge under the P1 will also flow to the MOS capacitor associated with P2. Repeating the same procedures, this charge packet can be transported continuously from pixel to pixel by manipulating the potential on the gates, until it reaches the edge of the device, and then is read out by the peripheral electronics.

Evolved from CCDs, the Fine Pixel CCD (FPCCD) is designed by KEK, Japan. The pixel pitch of 5 μm results in a high granularity, allowing the detector to record all the hit information over a beam train without time stamps [9]. The procedures of signal processing of FPCCD, including the charge-to-voltage conversion, amplification, binary discrimination, and data readout, are finished between the consecutive bunch trains ($\sim$199 ms). The high-speed readout electronics are therefore not necessary for saving the power consumption. This special readout method also removes the interference of RF noise. Since the process of readout is between two consecutive bunch trains, no particle-induced signal will be lost during the

readout, and thus the dead time of the FPCCD can be ignored. The 15 µm epitaxial layer is fully depleted such drift is the dominant charge transport mechanism. The FPCCD is operated at a low temperature of −50 °C to suppress thermal noise [10].

However, the FPCCD is susceptible to both the total ionizing dose (TID) and the displacement damage effects. The ionizing radiation damage introduces some charge traps in the oxide to increase the flat band voltage and the surface dark current. The displacement damage reduces the charge transfer efficiency (CTE), enhances the dark current, and creates random telegraph noise (RTN) in pixels.

2.2.2 DEPFET sensors

The DEPFET sensors technology, invented by Kemmer and Lutz in the 80′s, is an active pixel sensors (APS) in which each pixel is integrated with an individual amplifying transistor [11]. Figure 2.4 is the cross-sectional view of a DEPFET layout. In each pixel, a P-channel field effect transistor is structured within a high-resistivity n-type silicon substrate. By the application of the side-wards depletion principle, the whole substrate is fully depleted for an optimum charge collection efficiency. Moreover, a potential minimum for electrons can be created just beneath the gate of the P-channel FET with a distance of ∼1 µm. An additional deep n-type doping is inserted at the position of this potential minimum. As soon as an ionizing particle traverses through the substrate, the generated electron-hole pairs will be drift by the depletion potential. The holes are driven to the backside p+ contact. Simultaneously, the electrons drift toward the internal gate due to its potential minimum for electrons. The presence of the additional charges in the position of the potential minimum influences the charge carriers in the channel of the p-type FET, thereby regulating the electrical conductivity. The deep doping with the potential minimum has the same function to channel current as the gate of the FET, thus this deep doping is called internal gate, and the gate of the FET is referred to as external gate.

The potential of the internal gate modulates the drain current of the p-channel FET. The increase of the drain current is proportional to the electrons existing at the internal gate. So the DEPFET provides an in-pixel amplification capability. The extremely small capacitance of the internal gate yields low noise for the sensor. Benefiting from the in-pixel amplification, DEPFET sensors show a superior SNR performance. Moreover, the readout speed and the radiation hardness of DEPFETs are better than those of CCDs [13]. The room temperature operation is also of benefit to a low material budget.

The charge collection capability strongly depends on accurately controlling the internal gates' potential minimum. The accumulated charges, produced by the particle-induced electrons and the thermal-generated leakage current, shield the internal gate to deviate from the potential minimum, thereby degrading the charge collection efficiency. A reset of the internal gate periodically therefore is necessary for the DEPFET sensors to avoid the saturation of the sensor. Applying the proper voltages on the gates "clear" and "cleargate", the charges on the
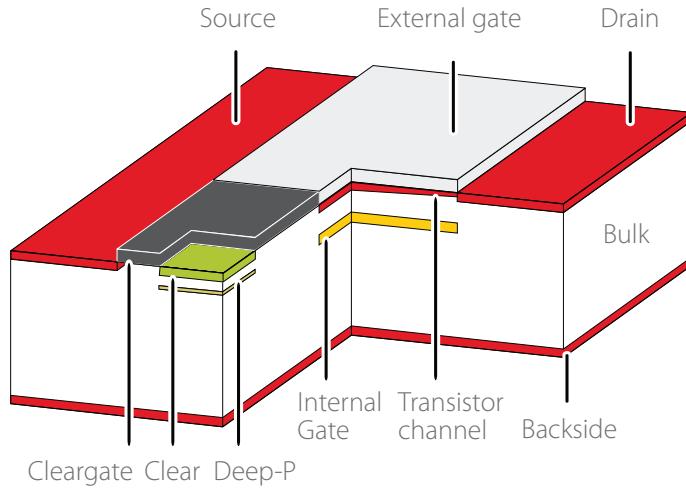
Figure 2.4: *Cross-sectional view of DEPFET pixel [12].*

internal gate can be removed.

To operate the DEPFET sensors, two specialized ASICs are required: one is responsible for steering the "FET gate", "clear", and "cleargate"; the other one reads out the current signals from the DEPFET sensors. However, these external chips complicate the system for the DEPFET sensors and introduce an additional insensitive area.

2.2.3 CMOS pixel sensors (CPS)

The sensors fabricated in standard CMOS VLSI processes, as the successors to CCD sensors, are favourably used to detect visible light, ranging from consumer electronics to industrial and medical imaging. They work for detection of ionizing particles as well as for visible light, referred to as CMOS pixel sensors (CPS). Since the content of this thesis concentrates on the design of CPS, a detailed discussion including operation principle, characteristics, typical architectures and development status are presented in this section.

2.2.3.1 Detection principle

The cross-sectional view of a typical CPS is depicted in Fig. 2.5, where the lightly doped p-type epitaxial layer, as the sensitive volume, is grown on the heavily doped p-type substrate. When the charged particle traverses the epitaxial layer, the electron-hole pairs are released along the track of this particle. The doping concentration of the p^{++} substrate and the p-wells for housing the NMOS transistors are several orders higher than that of epitaxial layer, thus a potential barrier is created at the boundaries among them. The particle-induced electrons and holes are reflected by this potential barrier and restricted within the epitaxial layer. The sensing diode, composed of the implanted n-well and the epitaxial layer, is reversely biased
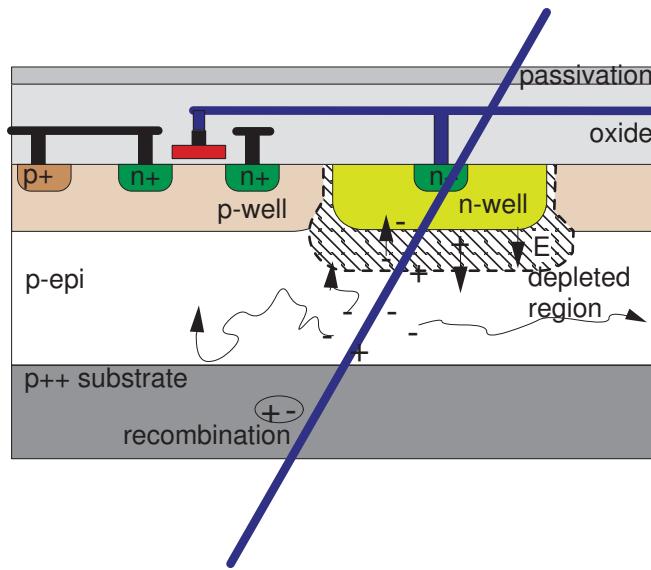
Figure 2.5: *Cross-sectional view and operation principle of a typical CPS. The undepleted p-type epitaxial layer, common in modern CMOS technologies, serves as the active volume of the sensor. The charges generated in this volume by a traversing particle diffuse thermally and then are collected by a n-well/p-epi diode. Typically, the thickness of the epitaxial layer is 10–15 μm [14].*

to collect the particle-induced charges. In CPS, the bias voltage of the sensing diode is limited by the power supply. As a consequence, the epitaxial layer is just partially depleted, and the charge collection mechanism is dominated by thermal diffusion. A part of the particle-induced charges will diffuse to the neighboring pixels and then get collected by the associated sensing diodes. The area distribution of the charges generated by one traversing particle creates a signal cloud called cluster, which is very crucial in calculating the hit position on the sensor. The current generated by the reverse-biased diode is integrated on the diode capacitor, leading to a voltage drop on the sensing node. This is a complete conversion from an incident particle to a measurable voltage signal.

2.2.3.2 Pros and cons of CPS

Compared with other sensor technologies, CPS demonstrate several appealing features adapted to the particle tracking:

- **High granularity** : A pixel pitch of 17 μm can provide the spatial resolution less than 3 μm with a binary output, which is sufficient to match the requirements of the ILD vertex detector [15]. Taking advantage of the analog output and the hit reconstruction from cluster, the spatial resolution can be improved to ~1 μm;
- **Low material budget** : CPS have a thin sensitive volume, typical around 10-15 μm. Thinning the wafer from ~700 μm to ~50 μm is possible without degrading the mechanical strength and detection performances;

- **Signal processing on the same substrate** : CPS fabricated in a standard CMOS process, allow to integrate both sensing elements and readout circuits on the same silicon substrate, which is of benefit for sensor miniaturization, flexible readout, and reliability;
- **Low cost** : Sensors are fabricated in the standard VLSI technologies. The processes are easily available through multi-project and engineering runs that allow cost-effective and relatively fast design-to-verification cycle in sensor design;
- **Others** : room temperature operation, and fabrication reliability.

Despite these features, CPS also suffer from a few apparent limitations:

- **NMOS only in pixel** : In the standard CPS, the additional n-wells to house the PMOS transistors attract a part of the particle-induced charges to compete with the sensing diode, leading to a degradation of the charge collection efficiency. The absence of PMOS transistors prevent the implementation of high performance circuits in pixels, such as a high gain amplifier;
- **No process optimization for radiation detection** : The parameters of the standard CMOS process, e.g. doping profile, thickness of epitaxial layer, feature size, and number of metal, are not optimized for radiation detection.

2.2.3.3 Basic architectures of CPS
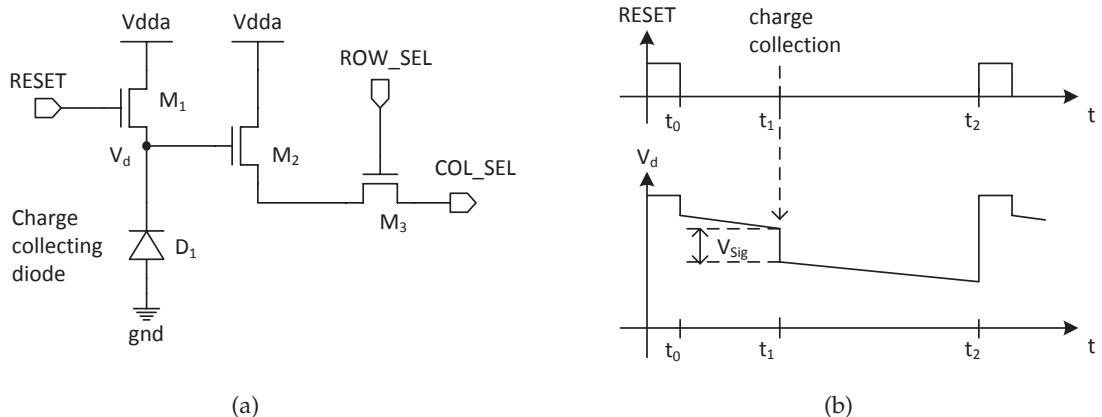
Figure 2.6: *The "three-transistor (3-T)" pixel cell, (a) schematic, (b) timing diagram showing the operation and the signal shape.*

The basic pixel structure, namely three-transistor (3-T) pixel, composed of three NMOS transistors and a reverse-biased n-well/p-epi diode, is shown in Fig. 2.6(a). The particle-induced current is integrated on the parasitic capacitor of the sensing diode, and thus results in a voltage drop at this node. The sensing diode is reset periodically with the NMOS switch M_1 by the control sequence, as shown in the Fig. 2.6(b). The particle signal is buffered by the source-follower (CS) transistor M_2, and then selected by the switch M_3 for readout. The bias current source of buffer is placed at the peripheral of the matrix and shared by a column of

pixels. This pixel structure is widely used in the visible-light image sensor. However, it suffers from a large reset noise in the order of kT/C_{diode}, where k is the Boltzmann constant, T is the absolute temperature, and C_{diode} is the sensing-diode parasitic capacitance. The leakage current of the sensing diode also contributes to the fixed pattern noise (FPN).

(a)   (b)
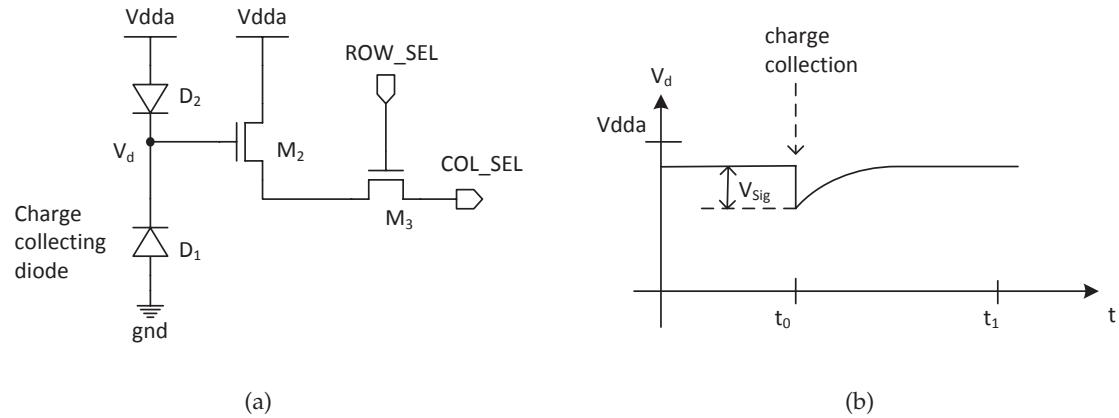
Figure 2.7: *Self-biased pixel cell (SB-pixel), (a) schematic, (b) timing diagram showing the operation and the signal shape.*

Another pixel scheme proposed for CPS is called self-biased (SB) pixel. The reset transistor in the 3-T structure is replaced by a high resistivity, forward-biased diode whose cathode is connected to the anode of the sensing diode. The SB pixel is especially suitable for applications which requires the detection of the weak signals with low signal intensity. The introduced diode is used to clear the signal on the sensing diode, and compensating the leakage current of the sensing diode. To prevent the gain loss due to a part of signal is removed before readout, the clear process should be very slow. Normally, the clear time lasts for several integration times in the order of several tens of microseconds. Compared with the 3-T structure, the SB pixel is free from reset noise and the leakage-induced FPN. However, a subtraction of the two signal samples from the two adjacent frames is necessary to derive the net signal from the incident particle. This signal processing is often referred to as correlated double sampling (CDS).

A typical architecture of a CPS with analog outputs is illustrated in Fig. 2.8. The individual pixels are arranged in a mosaic pattern called pixel matrices, which are read out by the peripheral readout circuits. The readout circuits are comprised by two shift register addressing circuits. The row addressing circuits selects one row of pixels in order to perform the special readout method called rolling shutter readout. The column addressing circuits label the pixels in one row with the address and read out them serially. The time required for the readout of the whole matrix of pixels is referred to as a frame time. Typically, a buffer is located at the end of the column of pixels to provide sufficient driving capability for the following analog readout or the digitalization.

According to the operational principle of CPS, for a CMOS process with a thickness of
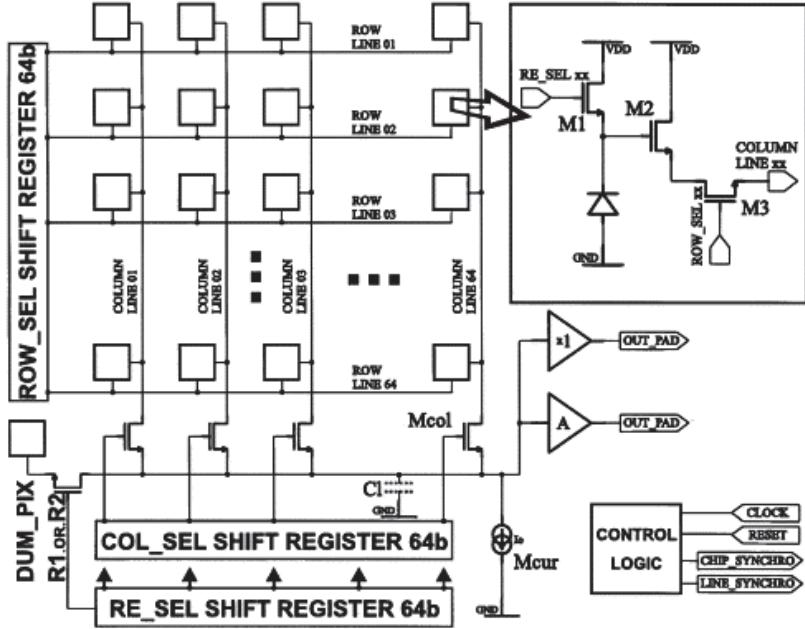
Figure 2.8: *Block diagram of a typical CMOS pixel sensor with analog outputs. The column and row addressing shift registers sequentially select pixels for readout [2].*

epitaxial layer of $\sim$10 µm, the voltage signal generated on the charge sensing node is restricted to the order of several microvolts. To ensure a sufficient SNR, the in-pixel amplifier is inserted within each pixel. In addition, the in-pixel CDS is also integrated to remove the pedestal voltage as well as the low frequency noise.
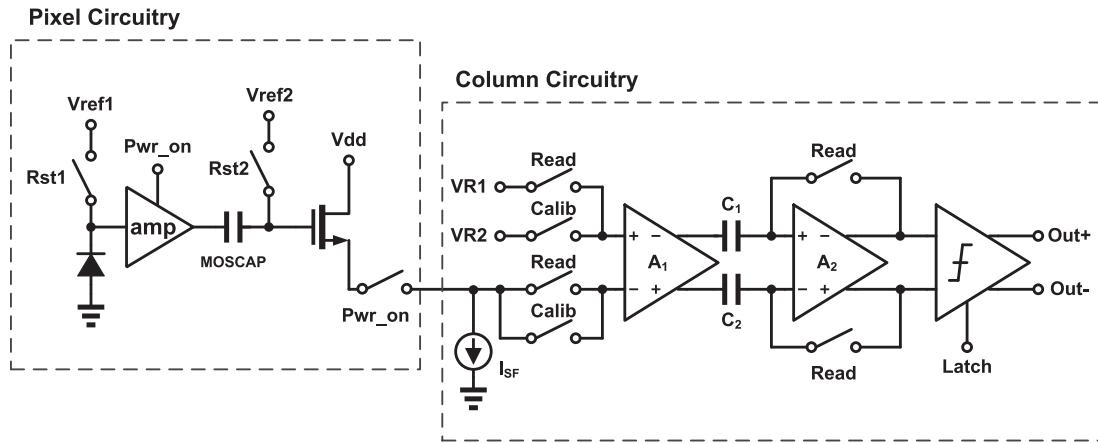
Figure 2.9: *Schematic diagram of a pixel cell and column-ended discriminator.*

The excellent performance of CPS with analog output have been verified with nearly 20 MIMOSA prototypes [16]. However, the frame rate of reticule sized sensors composed of several 10^5 pixels is limited to $\sim$1 kHz. The physics applications require higher readout speed, which asks for grouping the pixels in columns to read out in parallel and digitalizing the signals on chip. The signal discrimination implemented at the column level allows the sensor

to be read out in a high frame rate, up to 10 k frames/s [17]. A typical architecture of a pixel cell with a column-level discriminator is presented in Fig. 2.9. The particle signal processed by the in-pixel amplification and CDS, is connected to a discriminator located at the end of column. The discriminator circuit based on an offset compensated comparator, compares the particle signal with a threshold voltage to generate the binary result.

2.2.3.4 Development status of CPS

The application of CPS for particle tracking was inspired by the use of that in the visible-light imaging. A series of prototypes called MIMOSA (Minimum Ionizing particle MOS Active pixel sensor) has been designed, fabricated, and tested by the PICSEL group of IPHC in Strasbourg. Up to now, more than 40 prototypes have been implemented with a variety of pixel structures as well as different processes to exploit the optimum performances of CPS [16].

The MIMOSA-5 chip was the first full-reticle scale CPS prototype designed for particle tracking combining back-illumination and thinning technologies. In the MIMOSA-6 proto-type, an on-chip discrimination function was integrated on the pixel sensor. The self-biased pixel with feedback structure was introduced in the MIMOSA-16 chip to replace the 3-T and regular self-biased pixels for its merits in the radiation hardness and the less FPN. Moreover, the thick epitaxial layer option (~ 20 μm epi) also provided the prominent performances than ever before. A sensor with fast readout architecture sensor, namely MIMOSA-22, was integrated an on-chip zero suppression circuit to speed the readout up to 10 k frame/s. The development of the MIMOSA series chips represents the state-of-the-art of the CPS technology.

The CPS is a promising candidate for many high energy physics experiences. The STAR pixel detector (PXL) at RHIC/BNL is the first detector equipped with CPS. This detector has an array of 33 sensor ladders where each one with ten 2 cm $\times$ 2 cm sensors. The CPS designed for the STAR PXL, named ULTIMATE, features 890 k pixels with the pitch of 20.7 μm. The CPS are also operated well on the EUDET telescope project. As one of the options for the ILD vertex detector, CPS are foreseen to meet the requirements of this future linear collider. Additionally, some studies on CPS are also under development for other applications including the CBM-MVD at FAIR and the ALICE upgrade project at LHC.

Considered as a state-of-the-art CPS, the MIMOSA-26 is introduced as follows:

MIMOSA-26: CPS with data sparsification   The MIMOSA-26 is realized in the framework of the EUDET program aiming to explore the detector R&D for future accelerators, such as the ILC and LHC upgrade projects.

The MIMOSA-26 combines the studies of both prototypes: MIMOSA-22 allows particle detection with binary output and SUZE-0 performs the data sparsification and formatting function. The floorplan of the MIMOSA-26 is illustrated in Fig. 2.10, where the matrix features 1152 columns by 576 rows occupying an active area of $\sim$224 mm^2. The 18.4 $\times$ 18.4 μm^2 square
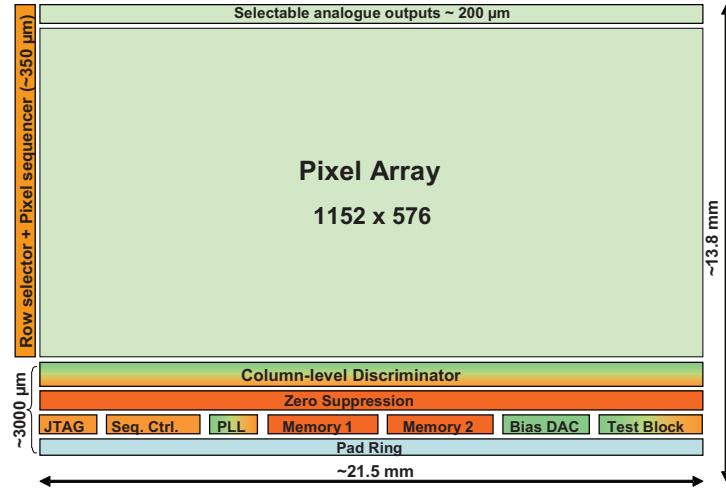
Figure 2.10: *Floorplan of MIMOSA-26 [18].*

pixel encompasses a sensing diode followed by an in-pixel amplifier and a CDS circuit. The whole matrix is read out in a rolling shutter mode steered by a row selection circuit on the left of matrix. Each column is terminated by a discriminator sharing the same pitch with the pixel, and the threshold is programmable with a JTAG interface. Total 1152 discriminators are operated in parallel to digitize the analog signals from the pixels. The readout time of the sensor is 112 μs driven by a clock frequency of 80 MHz to adapt the EUDET speed foreseen. With a 3.3 V power supply, the static power consumption of the full sensor is ∼300 mW translated to 520 μW for each column. Considering 1% occupancy, the dynamic power of the sensor amounts to ∼200 mW.

The binary data from the discriminators are pipelined through a data compression circuit, called zero suppression logic, at the sensor peripheral to stream the fired pixel in a sparse data format and then to store them in the on-chip memories. The memories are serially readout with two 80 Mbits/s LVDS serial links.

As discussed previously, the integration time of sensor is driven by the hit occupancy. A higher hit density requires a faster integration time to maintain the pixel occupancy at an affordable level. However, a short integration time generally gives rise to a huge raw data rate generated from the sensor. Because of the limitation of the output links in both number and speed, a data compression technique is required to extract the hit information from the sparse output data stream. Changing with the hit densities in various experiments, expected data suppression ability by a factor of 10 to 10000 can be achievable [19]. In MIMOSA-26, the zero suppression is based on the architecture of SUZE-1, to be compatible with the constraints of STAR and EUDET.

MIMOSA-26 has been fabricated with ∼10 Ω·cm low resistivity epitaxial layer with thickness of 14 μm (Std–14), and ∼400 Ω·cm high resistivity epitaxial layer with thickness of 10, 15,
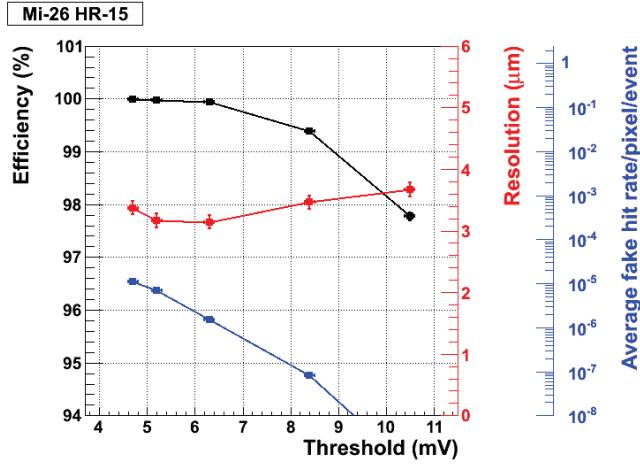
Figure 2.11:
Beam test results of MIMOSA-26 obtained at the CERN-SPS 120 GeV/c pion beam. The resistivity of epitaxial layer is ~400 Ω·cm, and the thickness is 15 μm (HR-15). The detection efficiency (black curve), the fake hit rate (blue curve) and the single point resolution (red curve) are shown for various thresholds of the discriminator [21].

and 20 μm (HR–10/15/20) respectively [20]. The charge-to-voltage conversion factor (CVF) is the ratio between the output voltage for a particular pixel and the number of electrons collected during the integration time. The laboratory tests with ^{55}Fe show that the MIMOSA-26 chip with low resistivity epitaxial (Std-14) exhibits a CVF of ~74 μV/e$^-$. The temporal noise is 0.6-0.7 mV translated into an ENC of ~12 e$^-$. The FPN that mainly originated from the column-ended discriminators is 0.3-0.4 mV corresponding to an ENC of ~6 e$^-$. The sensors with the high resistivity epitaxial layer exhibit a similar performance. The charge collection efficiency (CCE) is the ratio between the charge collected by the sensing diode and the total charge generated by an impinging particle. Tests with ^{106}Ru validate the estimation that the sensors with high resistivity epitaxial layer have a larger depleted volume, thereby leading to higher CCE. The signal-to-noise ratio (SNR) of the seed pixel for the sensors with standard epitaxial layer (Std–14) and with high resistivity epitaxial layer (HR–10/15/20) are 20, 35, 41, and 36, respectively, and therefore an optimized sensor with a 15 μm high resistivity epitaxial layer is arrived at.

The MIMOSA-26 is also tested with the 120 GeV/c pion beam from the CERN-SPS to simulate a real operation. The test results of HR-15 are shown in Fig. 2.11. The spatial resolution is ~3.5 μm. With a threshold voltage of ~5 mV corresponding to 6 times of the ENC, the detection efficiency of Std-14 is ~ 99.5 ± 0.1% together with a fake hit rate of ~10^{-4}. The sensor with a high resistivity epitaxial layer demonstrates a similar detection efficiency with the fake hit rate of ~10^{-5}, meanwhile it can stand a fluence of > 10^{13} n$_{eq}$/cm^2. After thinning to 120 μm thickness, a total of 62 sensors display a yield of 75%.

2.3 Conceptual considerations for the ILD-VTX based on CPS

As mentioned in Section 1.2.2, two geometries are under investigation as candidates for the ILD vertex detector: the VTX-SL featuring five single-sided layers and the VTX-DL with three double-sided layers. Both conceptual geometries are expected to be sufficient for the

specifications of the ILD vertex detector, whereas the VTX-DL gives a better impact parameter resolution for the high momentum tracks, as well as an enhanced performance in background rejection. In this thesis, the discussion therefore will only be dedicated to the VTX-DL geometry.

2.3.1 Overview of the VTX configuration

As presented in the previous sections, the compliance of CPS with the spatial resolution and material budget specifications of the ILD vertex detector are not questionable. The sufficient radiation hardness was based on the measurement of MIMOSA-26, and thereby is well adapted to the running conditions. The remaining issue involve whether the readout rate can accommodate the high hit rate due to the beam related background, as well as the power consumption is capable to comply with a low-mass cooling technique, such as forced air flow.

The VTX is composed of the ladders arranged in concentric cylindrical layers to form barrels surrounding the interaction point. Since the three double-sided layers feature the average radii of 17, 38, and 59 mm, the different sensor geometries and operating backgrounds ask for special sensor schemes dedicated to the innermost and the outer layers respectively.

The design of the sensors equipped on the innermost layer is motivated by the optimization of pixel occupancy, which not only relates to the hit density, but also depends on the time resolution, pixel size, cluster multiplicity, and thickness of sensitive volume. For the purpose to separate two hits without the loss of the particle information, which is crucial to the particle tracking reconstruction, it is necessary to keep the occupancy of pixel at an acceptable level. According to the former studies, the 1% occupancy with an assumption of 10 times safety factor is the upper boundary for effective particle tracking in the vertex detector [22].

The sensing area of a full scale CPS designed for the innermost layer is ∼25 mm (row) × 9.6 mm (column). Based on this matrix size, a sensor incorporating column-parallel readout and fine pixel size, the same as the architecture of MIMOSA-26, imposes a readout time of ∼100 μs. This architecture can cover the VTX requirements for a highly segmented ultra light sensor but requires a significant readout time shortening. Hence, the available CPS designs are not appropriate to the geometry of single sided ladder due to the limitation in sensor readout speed. To address this issue, the concept of VTX-DL is proposed to separate both spatial and time resolution requirements to two separated sensors, mounted on the both sides of the ladder respectively. As shown in Fig. 2.12, two types of sensors, one contributed to spatial resolution and the other one devoted to temporal precision, with ∼2 mm distance, can collaborate on recoding the tracks of the traversing particles in position and time simultaneously [23]. This geometry not only relaxes the design of the sensors, but also promotes the readout speed in one order of magnitude to match the possible upgraded energy of 1 TeV.

Taking advantage of the large distance from the interaction point, the outer layers suffer a much less hit density than the innermost layer, leading to a less demanding requirements
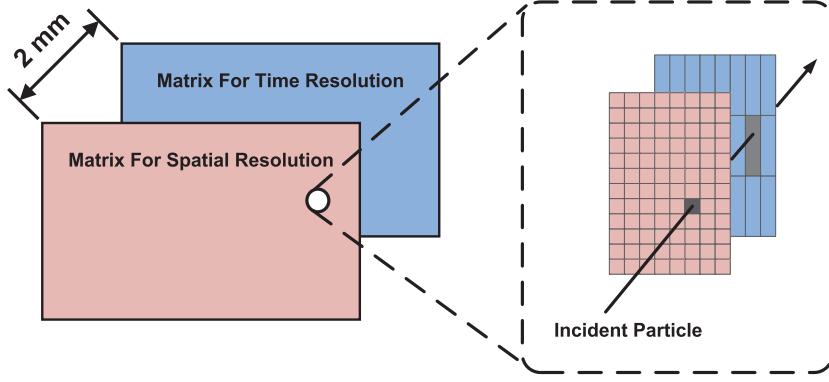
Figure 2.12: *Structure of the double-sided ladder for the innermost layer.*

in terms of spatial resolution and readout speed. However, the sensors equipped on the outer layers cover ~90% surface of the whole sensitive area in the VTX. Thus the corresponding sensors are designed giving the priority to the power consumption to allow a low-speed, air cooling scheme in VTX. The targeted parameters of the VTX-DL architecture are listed in the Table 2.1.

Ladder	σ_{sp} (µm) In / Out	$t_{r.o.}$ (µs) In / Out	Occupancy (%) In / Out	Power (W) Inst./Average
VTX-1	3 / 5-6	50 / 10 (2)	0.9 (4.5) / 0.1 (0.5)	250 / 5
VTX-2	4 / 10	100 / 100 (7)	0.3 (1.5) / 0.04 (0.2)	120 / 2.4
VTX-3	4 / 10	100 / 100 (7)	0.06 (0.3) / 0.01 (0.05)	200 / 4

Table 2.1: *Parameters of the 3-double-layer VTX equipped with the CPS at the luminosity of 0.5 TeV (the values for 1 TeV operational energy are in brackets). Sensors assumed to be fabricated in a 0.18µm process. VTX-1 is the ladder on the innermost layer. VTX-2 and VTX-3 are on the intermediate and outermost layer respectively. The parameters of the spatial resolution (σ_{sp}), readout time ($t_{r.o.}$), and pixel occupancy are dedicated to both sides of the ladder. The instantaneous power consumption is the peak value of the whole VTX. Considering a conservative assumption of a duty cycle of $\leq$2%, an average power consumption can be calculated [24].*

Next, we will discuss the sensors designed for both innermost and outer layers based on CPS, fully adapted to the collision energy ($\sqrt{s}$) of 0.5 Tev and 1 Tev respectively.

2.3.2 Innermost layer

The ability of particle reconstruction is defined by the impact parameter. For the purpose of improving the impact parameter resolution, the radii of the innermost layer should be minimized, thereby leading to a highest hit density suffered on this layer. The design of the innermost layer therefore gives a priority to the spatial and temporal resolutions to match the substantial beam background.

Collision energy $\sqrt{s} \lesssim 0.5$ TeV In the energy of $\sim$0.5 TeV, the sensors equipped on the inside of the ladders which compose the innermost layer of vertex detector, are demanded to fulfill a spatial resolution of $\lesssim 3$ μm and a relaxed temporal resolution of 50 ns. A sensor featuring the same pixel architecture as MIMOSA-26 but a slightly smaller pixel size of 16×16 μm^2 as well as a modified two-sided readout approach, can arrive at the targeted single point resolution as well as a twice as fast as the readout time of $\sim$50 ns. The cost is the double power dissipation and the additional insensitive area. Certainly, this issue can be compensated by implementing the design in an advanced CMOS process with a small feature size. Taking a 0.18 μm process for example, compared with the case in a 0.35 μm process, the estimated power dissipation will be reduced to 1/3 of previous one due to a lower power supply, while 25–50% reduction of the insensitive area is expected. Moreover, the smaller parasitic capacitance distributed on the interconnection metal may accelerate the readout time to 40 ns further.

The sensors mounted on the outside of the ladders are used to provide the time stamps of the hits. In terms of a sensor combining the rolling shutter readout mode and the column-parallel binary output, the frame time is only proportional to the number of the pixels in one column. For the sensor with a given size, enlarging the pixel size and thereby less number of row is efficient to speed up the readout. Therefore, to elongate the pixel size in column direction with a factor of 4–5 is expected to speed up the readout time to $\sim$10 ns by the same factor. The loss of spatial resolution can be compensated by the highly granular sensors mounted on the other side of the ladder.

In the PICSEL/IPHC group, several prototypes have been fabricated and measured to validate the concept addressed above. MIMOSA-22AHR, fabricated in a 0.35 μm OPTO process, includes the sub-matrices with the elongated pixel of 18.4×73.6 μm^2 placed in staggered arrangement. A MIP test (120 GeV π^- from CERN SPS) showed that the detection efficiency is approximate to 100%, meanwhile the spatial resolution maintains $\sim$5–6 μm. In 2011, a prototype, called MIMOSA-30, was designed to integrate with the actual size pixels for the innermost layer of the ILD vertex detector. The sensor, still implemented in the above mentioned 0.35 μm process featuring 4 metal layers and a high resistivity epitaxial layer ($\sim$400 Ω·cm resistivity, 15 μm thickness), is composed of two matrices. One matrix structured in 128 columns by 256 rows pixels with a standard pitch of 16×16 μm^2 devoted to the desired spatial resolution, and the other one features the 128 columns by 64 rows pixels to verify a 16×64 μm^2 elongated pixel. Each column of pixels is terminated by a discriminator for binary output. In addition, both sensors mirrored along the horizontal axis, can be read out in parallel to test the concept of the double-sided readout structure. The expected performance of the matrix with highly granular pixels are a spatial resolution of < 3 μm together with a readout time of $\lesssim 50$ μs. For the other matrix with elongated pixels, the spatial resolution is $\sim$6 μm and the readout time is $\sim$10 μs. These test results confirm the estimation.

Collision energy $\sqrt{s}$ **of 1 TeV**   In the enhanced collision energy of $\sim$1 TeV, the prominent boost in the hit density imposes a more demanding condition on the readout time. Compared with the 500 GeV baseline energy, the 3-5 times hit density induced by the upgraded energy forces the readout time to be accelerated by a factor of 5, meanwhile the spatial resolution is maintained. The previously mentioned sensor has a limited potential to reduce the targeted readout time from 10 ns to 2 ns, hence an advanced sensor, which features in-pixel discriminators as well as a highly parallelized rolling shutter configuration, was proposed to reach ultra-speed readout.

Based on a 0.18 μm CIS process, a sensor, named AROM-0, has been implemented to accommodate the demands in upgraded energy condition [25]. The 16×16 pixel matrix composed of the in-pixel discriminators within the elongated pixels of 22×33 μm^2, is expected to achieve a twice faster than the previous design shown in MIMOSA-30. A possible double-row readout method was also explored for further promoting the readout speed.

2.3.3 Outer layers

The outer layers face the reduced beamstrahlung induced hit density, which is one and two order of magnitude less for the intermediate and outermost layers respectively than that of the innermost layer, thereby asking for a less demanding requirements in terms of spatial resolution and readout speed. However, the good coverage of the outer layers demands the sensors to occupy $\sim$3000 cm^2, which is almost 10 times larger than that in the innermost layer. The foreseen power consumption of the outer layers is 3 times less than that of the innermost layer [21]. As a result, the constraint on power dissipation motivates a special sensor design dedicated to the outer layers.

Collision energy $\sqrt{s} \lesssim$ **0.5 TeV**   A spatial resolution of $\sim$4 μm and readout time of $\sim$100 μs are considered as adequate at $\sqrt{s} \lesssim$ 500 GeV. For a given sensor size, which is generally decided by the physics demands of the detector, there exists an obvious compromise between pixel size, frame rate, and power consumption. A small pixel size is better for improving the spatial resolution but at the expense of lower frame rate as well as more power consumption. In the rolling shutter readout, the power consumption is proportional to the number of columns. An intuitive method to squeeze the power consumption is enlarging the pixel size, thereby a less number of columns. Taking into account of the trade-off between the above factors, the sensors adapted to the outer layers are read out on one side and composed of pixels with a size of 35×35 μm^2, i.e. around 4 times larger than the pixels of the innermost layer. The loss of the spatial resolution due to the large pixel size can be compensated by replacing the discriminators with ADCs.

The spatial resolution of a sensor relies on several factors including pixel pitch, quantization resolution, cluster shape, and hit reconstruction algorithm, whereas the first two items are dominant. With respect to the pixel size of 35×35 μm^2, it lacks the measured results on the

spatial resolution varying with the various quantization levels. Therefore, an estimated spatial resolution is interpolated from tests of previous MIMOSA sensors, as listed in Table 2.2. A pixel pitch of 35 μm equipped with a 3-4 bits ADC is expected to provide a spatial resolution ~3–4 μm. This value is derived from the sensor fabricated in a 0.35 μm process, and a better result can be expected if the design is migrated to a 0.18 μm process.

Pitch (μm)	20	20	30	35	40
Number of bits	12	4	12	3-4	12
Epi-layer	low-res	low-res	low-res	high-res	low-res
$\sigma_{s.p}$ (μm)	1.5	1.7	2.1	$\leqslant 4$ (extrapolated)	3

Table 2.2: *Measured and calculated single point resolution as a function of pixel pitch, ADC resolution and resistivity of the epitaxial layer [26].*

The power dissipated by a column of pixels is ~520 μW which is given by the tests of MIMOSA-26. Assuming the power consumption of one column of pixels and a column-level ADC is less than 1 mW, the instantaneous power dissipation of the full VTX is estimated to be 700 W. Taking into account of the beam time structure of the ILC (0.5% duty cycle), and employing a conservative assumption of duty cycle of ~2%, the estimated average power consumption of the full VTX is $\lesssim$15 W, which allows for an air flow cooling system with low circulation speed [27]. Therefore, the power consumption of the ADC should be less than 500 μW.

Based on the above proposal, a prototype MIMOSA-31 has been submitted at 2011. It features the pixels of 35 μm pitch, arranged in 48 columns and 64 rows, as well as the 4-bit ADCs at each column. The measured temporal noise and FPN of the ADCS are 0.96 mV and 0.40 mV, respectively. At a sampling frequency of 6.25 MS/s, the power consumptions of an ADC are 486 μW during idle time, and 714 μW when a hit is detected [28].

Collision energy $\sqrt{s}$ of 1 TeV   At a collision energy of 1 TeV, the beamstrahlung induced hit density is expected to increase by a factor of 3 to 5 with respect to its 500 GeV value. The double-sided ladder structure used in the innermost layer can be extended to the outer layers to deal with the increased hit rate but at the cost of more power consumption.

2.4 Conclusion

This chapter addresses the detector technology dedicated to the application of the VTX in the ILD. The function of the VTX relies on the highly precise measurement of the particle tracks close to the interaction point, which asks for the sensor to feature a high granularity and a strong radiation tolerance. The silicon-based pixel sensor is well suited to meet the desired requirements. The discussion starts from the introduction of the operational principle of the silicon detector. The knowledge covers the events behind the interaction between silicon and incident particles, how the particle energy is converted to the charge, and then to

be collected by the sensing element for the further processing. Operating in the high luminosity circumstance within the VTX, the silicon damage because of the radiation deserves a detailed discussion. According to the difference in mechanism, the radiation damage can be categorized into the bulk and surface damage which due to the non- and ionizing radiation, respectively. Some approaches to alleviate such damage are also presented as a guide in the pixel design.

Several detector techniques are under development as the candidates with the respect to the ILD-VTX. In this chapter, some typical structures are discussed for the reader to better understand their pros and cons. The discussion especially concentrates on the CPS that was proposed by our group (IPHC/CNRS, Strasbourg) for more than ten year ago. Besides the better spatial and time resolution, the radiation tolerance of CPS is also promoting because of the advance of the CMOS process. Advantage to the other techniques, the CPS has a prominent merits on the fabricated cost and the high integration density.

In the last part, the VTX requirements driven by the physics background are provided. The configuration with the double-sided ladder is proposed. Since the different operational circumstances, the innermost and outer layers ask for the different specifications. In the innermost layer, two types of sensors feature the various pixel geometries are designed to be mounted on the different sides of ladder. The sensors on the outer layers adopt the scheme of multi-bit quantization for the low power consumption. Therefore, this VTX architecture can reach a better balance between the various requirements.

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3

Study of CPS with Pixel-level ADCs

The framework of this thesis is motivated by the specifications adapted to the outer layers of the ILD-VTX. As indicated in the previous chapter, the CPS integrated with ADCs allows a good balance between spatial resolution and power consumption. A variety of ADC topologies (e.g. SAR, pipeline) and configurations (e.g. chip-level and column-level) have been exploited in the past, and the targeted specifications are partially satisfied. The performances of ADCs are possible to be improved further by architectural upgrades combined with the use of advanced CMOS technologies with smaller feature size. Therefore, we propose the architecture of pixel-level ADCs to be used in CPS. It demonstrates some features which are particularly attractive for particle detection.

This chapter starts with an introduction in the performance metrics of ADCs. The various topologies of ADCs are then overviewed. The typical architecture of pixel-level ADCs is introduced followed by a discussion on its pros and cons. By reviewing the state-of-the-art of the ADCs used in pixel sensors, it is possible to highlight the existing tendencies imposed to the ADCs, thereby guiding the sensor design.

3.1 Performance metrics of ADCs

A good understanding of the specifications of ADCs is critical in designing the converters to meet the expected performances. In this section, the general information used for describing an ADC will be presented, which is important not only in the processing of circuit design, but also in the circuit measurement. Generally, the specifications of ADC can be defined into two categories: static specifications and dynamic specifications.

The ideal input-output characteristic of a 3-bit ADC is a staircase with the uniform steps over the entire dynamic range. Within the full-scale range of analog input, the output codes of the ADC range from "000" to "111". The width of the step is defined as one least significant bit (LSB), whose value represents the analog resolution. The static errors which degrade the accuracy of the ADC when it is converting a static signal, can be described by differential non-linearity (DNL), integral non-linearity (INL), offset error and gain error. Additionally,

since the ADCs used in the particle tracking usually feature a small LSB, the temporal noise is crucial to the SNR of ADCs. All these metrics are introduced as follows:
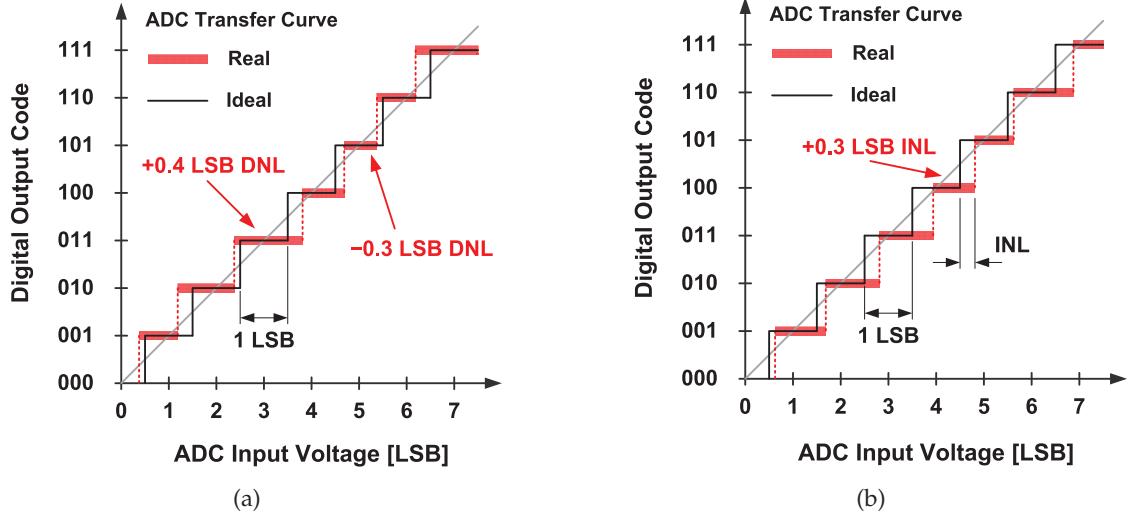
Figure 3.1: *Non-linearity of a 3-bit ADC: (a)DNL, and (b)INL.*

Differential non-linearity: The DNL as shown in Fig. 3.1(a) describes the deviation between the actual position of the transition step from the ideal one. For two adjacent codes "D_i" and "D_{i-1}", the corresponding analog signals at the transition edges are $X(D_i)$ and $X(D_{i-1})$, respectively. In the ideal case, the different of those two signals, $\Delta_{ideal}=X(D_i)-X(D_{i-1})$, is equal to one LSB. In the actual case, the transition step is deviated leading to a new differential value Δ_{actual}. The DNL at the code of "D_i" is defined by

$$DNL(D_i) = \frac{\Delta_{actual} - LSB}{LSB} \ . \tag{3.1}$$

Each pair of adjacent codes has a corresponding DNL value. For an n-bit ADC, total (2^n-1) DNL values compose a set of complete error distribution. The DNL is usually represented in the unit of LSB. To guarantee that there is no missing code and the transfer function is monotonic, the DNL should be less than 1 LSB.

Integral non-linearity: Both of INL and DNL are the criteria to describe the deviation of the input-output transfer curve between the ideal and actual ADCs. In contrast to the DNL that measures the deviation between two adjacent codes, the INL depicts the accumulated errors due to the DNL. As shown in Fig. 3.1(b), the INL is defined by the different of the transfer curve between the ideal and the actual cases. The INL can be calculated by integrating the

DNL. The INL for the code "D$_i$" is

$$INL(D_i) = \sum_{j=0}^{D_i} DNL(j) \, . \tag{3.2}$$

Gain error: The gain error is defined as the difference between the ideal and actual gain points on the transfer function after the offset error has been corrected to zero. Generally, this error can be removed by trimming the references of ADCs.

Offset error: The offset is a systematic deviation between the ideal and actual code transition. Comparing the transfer curves of an ideal ADC with an actual one, due to the offset, there is a shift between these two curves. Generally, the offset is measured at the zero code. The offset can be reduced by the circuits with the offset suppression techniques as well as a better layout.
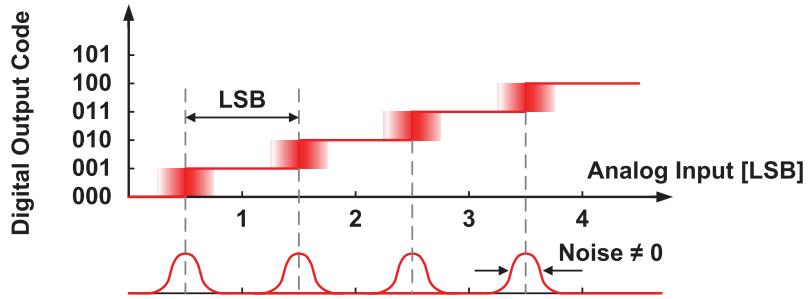
Figure 3.2: Effect of temporal noise on the ADC transfer curve.

Temporal noise: The temporal noise modeled as a noise source connected in series with the input of a noise-free ADC, results in an uncertainty of the ADC code for a given analog input. The effect of the temporal noise on the ADC transfer curve is shown in Fig. 3.2. As the analog input is increased, the ideal ADC maintains a constant output code until the transition region is reached. A noiseless ADC demonstrates a transition region width equal to zero. Considering the temporal noise in ADCs, this transition region is widened, which depends on the value of the noise.

Within the circuits of ADCs, three noise sources are dominated: thermal noise, low-frequency noise, and shot noise. Two types of low-frequency noise exist in CPS: $1/f$ noise and random telegraph noise (RTN). The detailed description of these noise sources can refer to [1,2].

3.2 ADC architectures

The ADC architecture determines how well the CPS can meet the targeted performance for our application. As indicated previously, the adopted ADC architecture should have fea-
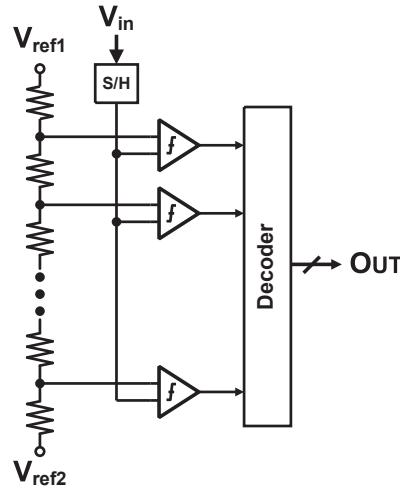
Figure 3.3:
Topology of a typical flash ADC. A group of parallel comparators compare the analog signal with the linear-distributed references that can be generated by a resistor ladder.

tures including high speed, low power consumption, and small area. In order to arrive at the optimum architectures, an overview of some general ADC architectures is given in this section.

3.2.1 Flash converter

The most intuitive and direct approach to digitalize an analog signal is to compare it with the fixed references which are equal to transient points between each pair of adjacent steps as illustrated in the staircase transfer curve. Flash ADCs are based on this concept. Figure 3.3 is the diagram of a typical flash ADC.

Flash ADCs feature a extremely fast sampling rate compared with other types of ADCs. However, a huge number of comparators are required. For an n-bit resolution, total 2^n comparators are demanded, meanwhile the extension of per bit in resolution results in a double number of the comparators. In addition, the input analog signal suffers large parasitic capacitances at the input of the comparators. As a result, the exponential growth of power, area, and input capacitance of flash ADCs as a function of resolution make them impractical for resolutions above 8 bits, calling for other topologies that provide a more relaxed trade-off between these parameters.

3.2.2 Pipeline converter

The pipeline architecture is composed of a cascade of individual stages that each one undertakes a sub-task of conversion. A generic schematic view of the pipeline ADC is illustrated in Fig. 3.4. Because the each stage operates individually, the whole converter is configured in a pipeline. The equivalent conversion time is only one clock period, but exists an output delay which is proportional to the number of stages. For the case of the single bit quantization in each stage, an n-bit resolution of ADC only consists of n comparators.
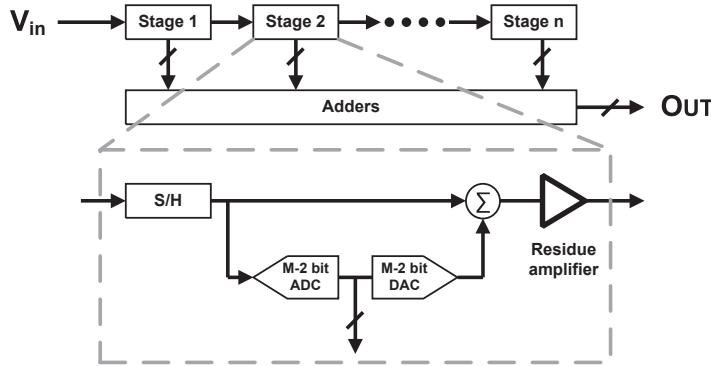
Figure 3.4:
Topology of a typical pipeline ADC. The input analog signal is firstly digitalized by the first stage, and provides the MSB code. This code is converted back to the analog value and then subtracted from the analog input. The residue is then input to the second stage to generate the MSB-1 code. Same operation is repeating until the LSB is achieved.

Compared with the flash architecture, pipeline ADCs exhibit a good trade-off between speed and power consumption. Furthermore, the advanced fabrication process and the digital correction and calibration promote the pipeline to achieve a resolution better than 8-bit at the operational speed of gigahertzes. However, the complicated circuits and large power consumption due to the high accuracy amplification blocks prevent the implementation of pipeline ADCs in the CPS.

3.2.3 Sigma-delta (Σ-Δ) converter

Unlike Nyquist converters, the Σ-Δ ADC features a sampling frequency that is several times of its Nyquist frequency, thus termed as oversampling converter. The block view of a typical first-order, single-loop Σ-Δ ADC is shown in the Fig. 3.5, where the circuit consists of an anti-aliasing filter, a Σ-Δ modulator, and a decimator. Benefiting from the oversampling and noise shaping techniques, the quantization noise is great attenuated by the Σ-Δ modulator. The output of the modulator is a high rate, n-bit data stream, hence a digital decimator follows to reduce the bit rate down to the Nyquist frequency.
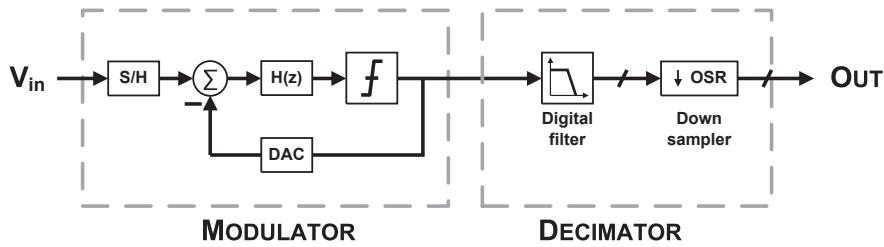
Figure 3.5: *The block diagram of a typical Σ-Δ ADC. The input signal is passing through the modulator with a low-pass function, unit-gain transfer functions STF. Meanwhile, the transfer functions of quantization noise NTF is high-pass like. Thus, the following decimator filters the quantization noise without affecting the analog signal.*

Σ-Δ ADCs are the good choice for the low-speed, high resolution applications. But the complicated structures in both modulator and decimator prevent the area-limited implemen-

tation.

3.2.4 Slope converter

Slope ADCs are the time-based converters that do not code the analog signal directly, but convert it into the intermediate timing information. The amplitude of the input signal is represented by the duration of a pulse. By computing the timing space of both rising edge and falling edge of this pulse, the duration time can be calculated by a digital counter or a time-to-digital converter (TDC). Figure 3.6 is the generic block schematic of a single-slope (SS) converter. As a simplest converter, it is only composed of a comparator as well as a digital counter.
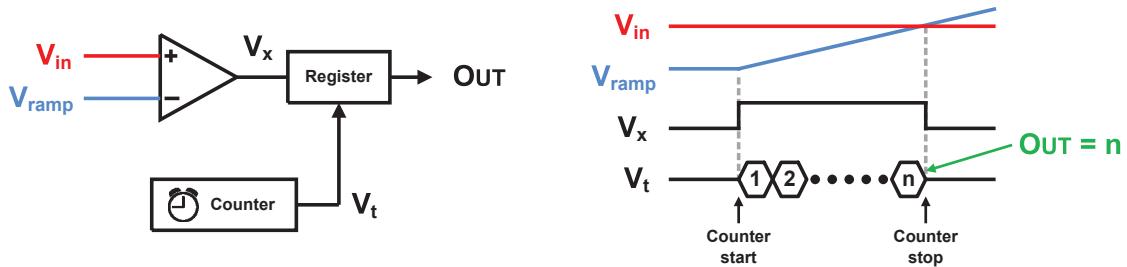
Figure 3.6: *Principle of single-slope ADCs. At the beginning of the conversion, the counter starts, meantime the ramp reference increases linearly. As soon as the ramp crosses the analog signal, the comparator records the counter codes as the final digital results.*

The slope type ADC employing the simple circuits to realize a high resolution typically in the range of 12-16 bits, is very suitable to implement an ADC within a small chip area for high density integration. The main drawback is the inherited slow conversion speed. For an ADC resolution of n-bit, 2^n clock cycles are required for a single-slope ADC. Thus slope ADCs are generally used in the low speed applications.

Wilkinson ADCs, as the variant of slope ADCs, have been used in pixel sensors. In the Wilkinson ADC, the threshold reference is not climbing up with time but constant. The input signal decreases linearly, and is compared with the threshold. Generally, the linearly dropped input signal is realized by integrating the analog signal on a capacitor, and then discharge it by a constant current. The accuracy of the Wilkinson ADC therefore greatly depends on the quality of capacitance, and the output accuracy of the current source. The dispersion of both the capacitor and current source results in the FPN.

Besides, other types of time-based ADCs including double-slope ADCs and pulse frequency modulation (PFM) ADCs have been explored in pixel sensors [3].

3.2.5 Successive approximation register converter

In contrast to slope ADCs which compare the input signal with the reference scanning from LSB to MSB one by one, SAR ADCs employ the ingenious principle based on the binary search algorithm. This algorithm has been known since the 1500s, but was first introduced in the commercial converter by Bernard M. Gordon in 1954. With the rapid progress in the integrated circuits, SAR ADCs are widely used in the low-to-medium speed applications to reach an 8-10 bits desired resolution. In addition, SAR ADCs exhibit more time efficiency than slope ADCs, and more component efficient compared to flash ADCs.
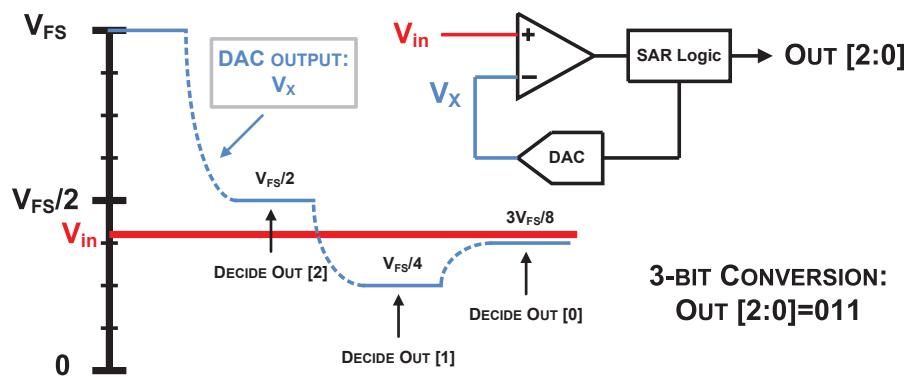
Figure 3.7: Principle of SAR ADCs.

The block diagram of a SAR ADC is shown in Fig. 3.7. Without loss of generality, we assume the SAR ADC has the resolution of 3 bits. The input signal V_{in} is firstly sampled by the sample-and-hold circuits at the Nyquist rate to perform the discrete conversion in the time domain. The DAC output, as the input threshold of the comparator, is initially reset to the midscale of the scale input range V_{FS} by the SAR logic circuits. If the V_{in} is larger than the $V_{FS}/2$, the first bit in the 3-bit register is set to "1". Meanwhile the threshold of the next comparison is chosen to midscale of the upper half of the full scale, i.e. 3/4 V_{FS}. On the contrary, if the output of the comparator is low, the associated bit in the 3-bit register is "0", and the threshold of the next comparison is assigned to 1/4 V_{FS}. Based on the chosen threshold, second comparison is performed according to the same principle. The same operation is successively repeating until the LSB is decided. Finally, the digitalized codes of the input signal can be read out from the 3-bit register.

The significant advantage of the SAR ADC is that there is a good trade-off between the circuit complexity and the conversion speed. In the framework of the SAR ADC, despite of a comparator, only a DAC and a SAR control circuit are necessary. It is possible to implement the SAR type ADC within a small silicon area. Moreover, this architecture exhibits the fast conversion speed. For a resolution of n-bit, the number of the comparisons is n, which is much faster than the slope type ADC. Besides the merits in the circuit complexity and conversion speed, the SAR ADC also shows a moderate power consumption.

3.3 Characteristics of pixel-level ADC technology

In pixel sensors, ADCs act as the bridges to connect the sensible, nature world to electronic devices. Driven by the advancement of CMOS processes, the architecture of ADCs has evolved from the chip- and column-level, to the latest pixel-level integration. In this section, the characteristics of pixel-level ADCs are introduced. Then, the promoted CMOS process required by the pixel-level ADCs is presented, followed a review of the state-of-the-art designs involved pixel-level ADCs.

3.3.1 Merits offered by pixel-level digitization
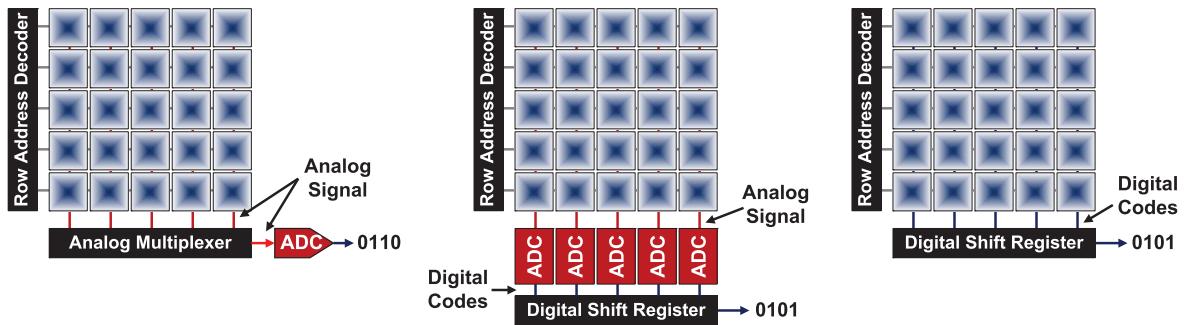
Figure 3.8: *Integration structures of on-chip ADCs. The ADCs are on chip-level (left), column-level (middle), and pixel-level (right).*

With respect to the pixel sensors equipped with the on-chip digitalization function, the ADCs are permitted to be implemented in chip-, column-, and pixel-level, as illustrated in Fig. 3.8. A comparison of them is necessary to reveal their pros and cons.

3.3.1.1 Chip-level digitalization

In the sensor integrated a chip-level ADC, the analog outputs from the pixels are selectively read out by a multiplexer, and then digitalized one by one. The only ADC is shared by all the pixels. This architecture featuring a simple structure, is well developed in the past decade and widely used in many commercial devices, such as the sensor in the visible-light digital camera.

The chip-level architecture shows some apparent merits. First, the ADC does not need to match the specified layout size such as pixel pitch, hence an large chip area can be occupied by the ADC with the complicated circuits. Additionally, the simple pixel circuits permit a high fill-factor to increase the charge collection efficiency. Moreover, since only one ADC is shared by all pixels, the uniform response of ADC is achieved, and thus less FPN.

However, the sensor with a chip-level ADC suffers several problems. First, this architecture

shows a poor SNR. This is because the outputs of the pixels need to be transmitted along the long column buses and then selectively read out by the multiplexer. In this procedure, the noise may be coupled to the weak pixel outputs to degrade the noise performance. Second, the readout speed of the sensor is greatly limited. Since the ADC operates in a time-division mode to digitalize the signal from each pixel, the readout time of one frame is equal to the product of the ADC conversion time and the number of pixels in the sensor. The ADC conversion speed usually is the major factor to slow the frame rate. This issue is even serious in the large-scale sensor. For instance, if a full-scaled sensor ($\sim$2$\times$2 cm^2) for the outer layers ILD-VTX is equipped with a chip-level ADC, the 35 µm pixel pitch and 160 ns/row readout time asks the ADC to operate at a sampling rate of more than 3 GS/s. Such high speed demands a large power consumption which is unacceptable for the constraint of power consumption. Additionally, the readout speed of sensor is also limited by the settling time of the pixel output to driven the large parasitic capacitance on the long column bus and multiplexer. Generally, the architectures of high speed ADCs, such as pipeline ADCs and time-interleaved ADCs are preferred by the chip-level ADC in pixel sensors.

3.3.1.2 Column-level digitalization

The column-level (also called column-parallel) ADC architecture was proposed to deal with the above mentioned weaknesses existing in chip-level ADCs. As shown in Fig. 3.8, the analog outputs from the pixels are sent to a battery of ADCs, each dedicated to one or more columns of pixels. The highly parallel operation relaxes the speed requirement on the ADCs. Benefiting from advanced processes, it is possible that the ADCs match the limited pitch size, and maintain the minimum inter-column crosstalk. The low-speed ADCs also alleviate the demand on the power consumption. The above advantages are at the cost of some insensitive area at the periphery of sensor. The deterioration in SNR still exists since the analog outputs transfer a long column bus. Moreover, a large FPN is provided by the sensor with column-level ADCs.

3.3.1.3 Pixel-level digitalization

For the sensor with chip-level or column-level digitalization, the pixel only contains a sensing diode that converts particle-induced charges into voltage, and some simple readout circuits (e.g. buffer and amplifier) to read the voltage signal off the pixel array. Other signal processing functionalities (e.g. CDS, shaping, and digitalization) are performed in the peripheral of sensor. Taking further advantage of the technology scaling, there exists a trend that the analog components in sensors are replaced by the digital counterparts as many as possible. Based on this concept, the so-called Digital Pixel Sensor (DPS) was proposed, as the foundation of the smart sensor. The means of the term "smart" cover collecting and interchanging the information, sensing the local events and the circumstance, and making the independent

decisions, all of which give more intelligence to pixels. The in-pixel signal digitalization is the key to implement the above-mentioned functionalities. Therefore, pixel-level ADCs are the important block in DPS and thus deserve a comprehensive study.

Compared with chip- and column-level ADCs, pixel-level ADCs exhibit several advantages:

- The pixel output featuring the binary format, is insensitive to the disturbance from the noise, hence promotes the SNR.
- The digital pixel output allows replacing the strong analog buffer in pixel with the digital one to drive the large parasitic capacitance distributed on the column metal line. In contrast to the analog buffer which is typically based on the source-follower, the digital buffer – inverter, consumes only a small dynamic power. Consequently, pixel-level ADCs usually result in a better power-efficiency. Moreover, the inverter also exhibits the features of the small area and easy-to-design.
- In the conventional pixel sensor operated in row-by-row rolling shutter mode, the frame rate is restricted by the pixel readout time and the scale of sensors. Pixel-level ADCs permit reading out several rows in parallel. Therefore the frame time is not limited by the row number, and a less frame time is easily achieved. Furthermore, benefiting from the increase of the readout speed, the ADCs can operate in a slower frequency for saving the power [4].
- This structure features the scalability, which has two meanings. The first one referred to the adaption to the large scale pixel sensor. Due to the great reduction of the analog signals, the design can easily extent to the desired scale without the significant correction. The second meaning is the ability of migrating to the new fabrication process, such as the 3-D vertical integration.

The main issue with pixel-level ADCs is the limitation of the pixel size that prevents the integration of a large number of transistors. Moreover, the high integration density increases the possible of the crosstalk between the different circuits, especially the sensing diode and the readout circuits. Both drawbacks can be solved by employing the advanced CMOS process with small feature size. In addition, an optimized layout is also helpful to reduce the crosstalk.

3.3.2 Requirements of process

To integrate the pixel-level digitalization in the pixel sensors also suffers from the limitation of the process. As the explanation in Section 2.2.3.1, the principle of the CPS relies on the N-well diode to catch the thermal diffusion electron-hole pairs that generated by the impinging particle in the silicon epitaxial layer. As illustrated in Fig. 3.9(a), the additional N-wells that for housing the PMOS will act as the competitor to absorb the electrons that original should be obtained by the N-well diode. This case that degrades the CCE should be avoided. However, PMOS transistors are indispensable in pixel-level ADCs to construct crucial circuits, such as high-gain operational amplifier, digital circuits, memory, and large-swing switch. At
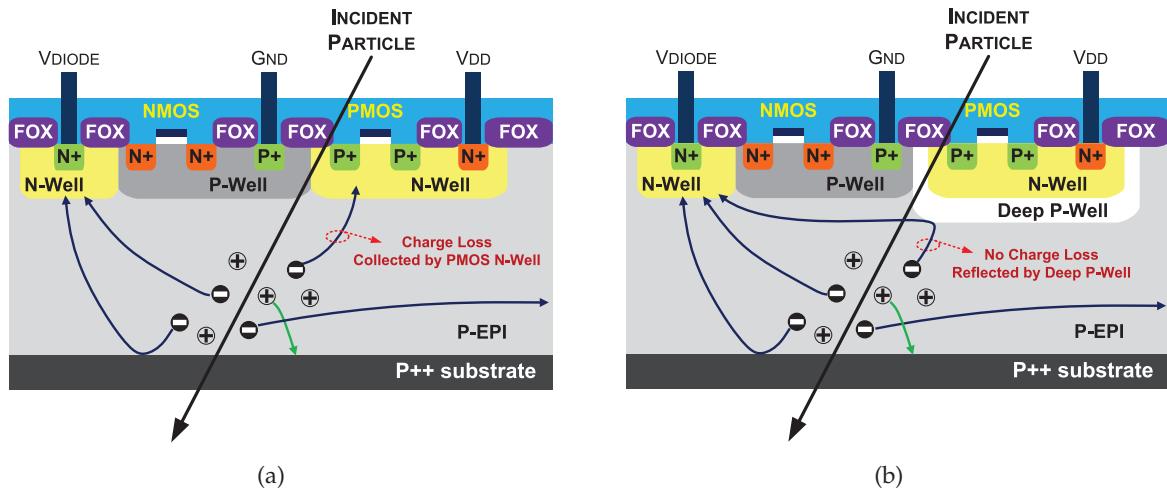
Figure 3.9: *Charge collection principle in (a) a standard dual-well process, and (b) a DPW process. In the dual-well process, some charges are collected by the N-well belonging to the PMOS resulting in a charge loss in collection. In contrast, the additional DPW underneath the PMOS prevents the charge loss.*

present, four techniques can be employed to handle this problem: Deep N-well (DNW), Deep P-well (DPW), SOI, and 3D vertical integration.

The solution of the DNW uses the deep n-well/p-substrate which provided in the triple-well process, as the sensing diode. Although this scheme is compatible to the standard CMOS process, the detection efficiency of the sensor is degraded which is inversely proportional to the size of n-well introduced by the PMOS. Two special processes — SOI and 3D integration process allow the in-pixel integration of PMOS without degrading the detection performance, but both of them are not compatible to the standard CMOS process, and demonstrate high cost and low yield presently.

Some foundry can provide the process with the option of the DPW which is originally used to isolate the active regions from the substrate to reduce the noise coupling. This feature is very useful for CPS. As illustrated in Fig. 3.9(b), the additional p-well underneath the PMOS transistors, can shield the associated n-well. The charges generated by the impinging particles are reflected by the potential existing at the interface between the deep p-well and epitaxial layer. Consequently, the integration of the PMOS within the pixel do not affect the CCE.

The MIMOSA series pixel sensors developed by PICSEL/IPHC/CNRS in Strasbourg started using the AMS 0.35 μm OPTO process from 2004 because of the superior performance in particle sensing and the low cost. But this dated process impedes the CPS development to meet the requirements of several upcoming vertex detectors (ILD-VTX, ALICE-ITS, CBM-MVD, SuperB factories). A new advanced CMOS process – Towerjazz 0.18 μm CMOS image sensor (CIS) process is exploited to replace the precedent AMS 0.35 μm process. This new process provides several attractive features as follows.

Firstly, this 0.18 μm process provides the DPW option which allows implementing PMOS

transistors in pixels without degrading the CCE. For its epitaxial layer, the resistivity varies from 1∼5 kΩ·cm and the thickness from 18-40 μm [5]. The high resistivity epitaxial layer will be more depletion biased by the sensing diode, hence provides a better charge collection. The measured results of the MIMOSA-32, which is fabricated with the ∼18 μm thickness, high-resistivity epitaxial layer, shows a good performance confirming the estimation. The additional DPW and PMOS in the pixel do not degrade the CCE [6].
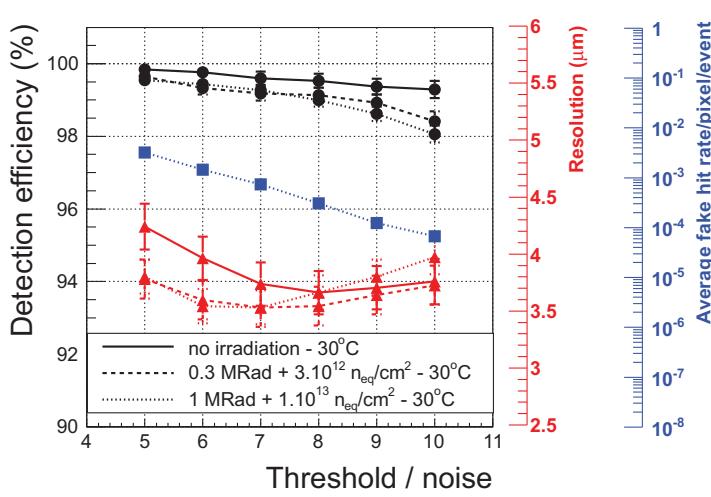
Figure 3.10:
Measurement results of MIMOSA-32 fabricated in Towerjazz 0.18 μm process. The detection efficiency (black bullets), the fake rate (blue squares) and the spatial resolution (red triangles) evolutions with the discriminator threshold (in units of noise) are displayed for three different radiation loads and at the highest coolant temperature of 30°C.

Secondly, this process shows an improved radiation tolerance. In the 0.18 μm process, the oxide gate thickness is only ~ 3.0 nm, which is much thinner than the ~ 7.5 nm in the 0.35 μm process. So the TID hardness of the new process is expected to be improved. The test displays that no significant deration of the distribution of the sensor exposing to a TID of 3 MRad. Thus a radiation dose of $\lesssim 1$ MRad/year can be sustained. In order to access the NIEL hardness together with performances such as the detection efficiency, and fake rate, MIMOSA-32 has been tested in the CERN-SPS with 60-120 GeV particles. As shown in Fig. 3.10, the detection efficiency still maintains $\sim$98 % with a worst condition of 30 °C operational temperature and exposed to 1MRad combining with 10^{13} n_{eq}/cm^2 radiation [6].

Thirdly, the 0.18 μm process provides up to 6 metal layers. The feature size for the Metal-1 layer is only 0.53 μm. So a high density design and routing can be realized beneficial for the integration of complicated circuits in the pixel. Moreover, the low supply voltage is in favor of a less power consumption.

According to the above reasons, the Towerjazz 0.18 μm CIS process is a proper choice for implementation of CPS with pixel-level ADCs.

3.3.3 State-of-the-art

A great variety of ADCs designed for the pixel sensors have been proposed, most of which is implemented in chip-level and column-level. Within the advanced CMOS process

node ($\leqslant 0.35$ µm), the technique of the pixel-level ADCs is more attractive to the design of pixel sensor, meanwhile shows a tremendous development potential. In order to better present this technique, some publications related to the pixel-level ADCs are reviewed here.

The concept of the pixel-level quantization is firstly proposed for infrared focal-plane arrays (IR-FPA) because of an acceptable large pixel as well as the demand on the high frame rate. A small scale (16×2) prototype was implemented in a 2 µm process featuring a pixel-level Σ–Δ modulation as a part of 10-bit ADC [7]. Several sensors were implemented soon after, sharing the same structure [8–11]. For a high SNR, the large oversampling ratio (OSR) restricts the sampling rate less than 100 Hz. The dated process also prevents high density integration, as well as results in a poor FPN. The various Σ–Δ structures have been exploited [12, 13]. In [14], besides the modulator, a decimator was realized in an independent pixel to compose a complete ADC. The 0.18 µm process permits to contain 298 transistors within a 38×38 µm^2 pixel. The frame rate is 30fps at the OSR of 1000 with the effective number of bits (ENOB) of ∼7.4-bit. The slow conversion speed and the complex structure are the main drawbacks of the $\Sigma - \Delta$ scheme.

To avoid the shortcomings of $\Sigma - \Delta$ architectures, the time-based architectures were studied to meet the pixel integration. D.Yang *et al.* presented a so-called multichannel bit-serial (MCBS) ADC architecture, which is similar to the slope ADC [15]. The pixel size is 10×10 µm^2, and each ADC is responsible to digitalize a group of 2×2 pixels. F.Andoh designed a sensor with the 8-bit in-pixel ADC based on the Wilkinson scheme in a 0.35 µm process [16]. However, the ADCs suffers a high random temporal noise and the FPN. Some following designs were presented based on the similar architecture [17–21]. All the previous works were designed for the visible light image. In the field of IR and X-ray detection, larger pixel is acceptable to reduce the particle-induced charge diffused to the neighboring pixels. In [22], a 2D prototype, which is transferrable to 3D vertical integration, was proposed using Wilkinson architecture. The 50 µm pixel pitch can be accomplished to fit the size of the IR sensor. As an example of the X-ray imager, the pixel-level ADC is also attractive for the large pixel size up to 150 µm×121 µm [23].

Since the SS ADC has a simplest architecture, it is the suitable choice for the pixel-level implementation. S.Kleinfelder *et al.* employed a 0.18 µm process to realize a large scale 352×288 pixel array that each one integrated a photogate, an 8-bit single-slope ADC as well as eight 3T DRAM cells [24]. The pixel, only 9.4×9.4 µm^2, incorporates 37 transistors meanwhile reach an ADC conversion time of ∼25 µs. C.Lai *et al.* designed an 8-bit single-slope ADC within a 9.4 µm pixel, and only consumes 81 µW power [25]. The designs with the single-slope architecture that implemented in each pixel [26–29] or a group pixels [30] have been studied to fit the various applications. In addition, some designs have successively realized the FPM ADC within each pixel [31–34].

Due to the features of fast conversion speed and the moderate resolution, SAR ADCs have been implemented in the pixel sensor mainly in the chip- and column-level. The obstruction

to design the pixel-level SAR ADC is coming from the large area required. The promotion of the CMOS process provides the possible to solve it. Until now, seldom works have been presented on the in-pixel SAR ADC. The sensor, named Qpix, merged SAR ADC in the pixel for measuring the deposited charge in the TPC readout belonged to the high-energy physics experiments [35, 36]. A 10-bit SAR ADC is contained in a 200 µm square pixel to occupy 70×140 µm^2 area [36]. The conversion rate is 10 MSps with the pixel power consumption of 187.5 µW. The measured results show the ENOB can reach 8.4-bit but a large offset. In the other application, a direct photon-counting X-ray image sensor hybridized a photoconductor for medical imaging was proposed, where a successive-approximation-like (SAL) ADC is integrated to quantization the photon energy [37].

Most of the reported designs with the pixel-level are summarized in Table 3.1.

REFs	Year	Tech. [µm]	Archi.	Area [mm^2]	ENOB [bit]	Conv. Rate [Hz]	Power [µW]	Appli.
[13]	2001	0.5	ΣΔ	9×10^{-4}	8.5	156k	4×10^{-2}	Vis. light
[38]	2006	0.35	ΣΔ	1×10^{-4}	9.6	7.61k	8.8×10^{-4}	Vis. light
[12]	2012	0.35	ΣΔ	1×10^{-4}	8.0	1k	6×10^{-2}	Vis. light
[14]	2013	0.18	ΣΔ	1.44×10^{-3}	7.2	0.05k	–	Vis. light
[15]	1999	0.35	SS	4.4×10^{-4}	8	0.515k	–	Vis. light
[24]	2001	0.18	SS	8.84×10^{-5}	8	40k	–	Vis. light
[25]	2006	0.25	SS	8.84×10^{-5}	8	10k	8.2×10^{1}	Vis. light
[26]	2007	0.13	SS	1×10^{-4}	10	–	–	Vis. light
[27]	2007	0.5	SS	6.35×10^{-4}	6	122	–	Vis. light
[30]	2008	0.35	SS	1.23×10^{-3}	10	1k	0.4	FPA
[28]	2008	0.18	SS	3.03×10^{-3}	7	5k	9.7	FPA
[29]	2009	0.18	SS	3.24×10^{-4}	8	–	–	Vis. light
[32]	2006	0.13	PFM	2.5×10^{-3}	15	500	1.8	Vis. light
[33]	2006	0.18	PFM	5.29×10^{-4}	10	–	0.25	Vis. light
[34]	2008	0.18	PFM	4.5×10^{-3}	10	1k	0.26	Vis. light
[39]	2009	0.09	PFM	9×10^{-4}	16	100	0.26	FPA
[16]	2000	0.35	Wilkinson	2.5×10^{-3}	8	3.84k	0.26	Vis. light
[17]	2003	0.18	Wilkinson	1.68×10^{-4}	8	50k	0.18	Vis. light
[18]	2004	0.35	Wilkinson	2.21×10^{-3}	8	–	–	Vis. light
[19]	2004	0.35	Wilkinson	9×10^{-4}	8	237k	–	Vis. light
[22]	2006	0.18	Wilkinson	4×10^{-4}	8	3k	7	FPA
[20]	2009	0.25	Wilkinson	9×10^{-3}	9	4k	7	Vis. light
[23]	2011	0.13	Wilkinson	1.39×10^{-2}	8	500k	634	X-ray
[40]	2012	0.18	Wilkinson	9×10^{-4}	14.3	12.8k	0.5	FPA
[35]	2010	0.18	SAR	2.8×10^{-2}	6	10M	350	HEP,GEM
[36]	2011	0.18	SAR	4×10^{-2}	10	10M	187	HEP,GEM
[41]	2012	0.13	SAR	3.6×10^{-3}	1.5	1M	4.6	X-ray

Table 3.1: Performance survey of the pixel-level ADCs published in the literature related to pixel sensor applications. It is sorted according to the ADC architectures and the publish date.

As indicated in Table 3.1, the pixel-level designs are tended to employ the process with small feature size to increase the integration density, most of which chosen the 0.18 μm process or even more advanced. Based on the applications, the sensor can be classified into two categories – the monolithic sensor that integrates the sensing element as well as the readout circuits on a same substrate, and the hybrid sensor that fabricates the sensing elements and the readout circuits on the different silicon, and connects them by the bonding pads. For the monolithic sensor, the selection of the process is mainly decided by the sensing elements, not the readout circuits, hence the ADC design cannot benefit the promotion of the process completely. While for the hybrid sensor, it has more freedom in the process selection.

In this thesis, two architectures – SAR ADCs and SS ADCs are chosen to be implemented in the pixel-level. The SS ADCs have the simple architecture that are very suitable for the area-limited design. In addition, the resolution and the conversion time can satisfy the requirements of our application. Until now, the pixel-level SAR ADC lacks the comprehensive study. How to reduce the layout area is the main issue faced by the designers. An improved SAR ADC structure is proposed to meet the requirement on pixel-level integration.

3.4 Conclusion

In this chapter, the basic fundamentals of the ADC have been introduced as a preparation work to guide the circuit design to be done in the next step. The parameters to evaluate the ADC performances are described, which is important for both design and test works. Then several generally-used ADC architectures are presented. The characteristics of them are emphasized especially for the in-pixel integration implementation.

Next, the discussion was focused on the features of the pixel-level ADC technique. The potential advantages within it was analyzed together with a comparison with the traditional chip- and column-level structures. Additionally, a detailed survey on the column- and pixel-level ADC was given which is useful in the optimization of the ADC architecture.

The next chapter will discuss the circuit design of a CPS equipped with the pixel-level ADCs, which is using the SAR ADC architecture.

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4

Design of CPS with pixel-level SAR ADCs

As pointed out in the previous chapter, pixel-level ADCs demonstrate some apparent merits compared with the chip- and column-level architectures. In order to validate the proposed concept of pixel-level ADCs, a prototype chip called MIMADC has been implemented, which is adapted to the outer layers of ILD vertex detectors. To arrive at an optimization of the ADC configuration, three independent pixel matrices were implemented on this chip with various topologies: one with SAR ADCs, and the rest two with single-slope (SS) ADCs. For the convenience to be distinguished with other two matrices, the matrix featuring pixel-level SAR ADCs is referred to as MIMADC-SAR throughout this thesis. This chapter presents the detail design of MIMADC-SAR ranging over sensor architecture, circuit design, and layout implementation.

4.1 Specifications of design

The design starts from the estimation of the sensor specifications. The complete specifications are given as follows:

- **Pixel size**
  As discussed in Section 2.3.3, taking into account of the trade-off between frame rate, power consumption, and spatial resolution, the 35 µm pixel pitch is a compromised choice.

- **Resolution**
  Extrapolating the test results from the previous MIMOSA series sensors, 3-4 bits resolution is possible to provide a spatial resolution $\leqslant 4$ µm at a pixel size of 35×35 µm^2. In the MIMADC-SAR, the resolution is initially set to 3-bit, and upgradable to 4-bit in the furture prototype.

- **Conversion time**
  The full scale sensor ($\sim 2 \times 2$ cm^2) read out in rolling shutter mode at the frame time of ~ 100 µs, translates into a conversion time of ~ 160 ns for each ADC.
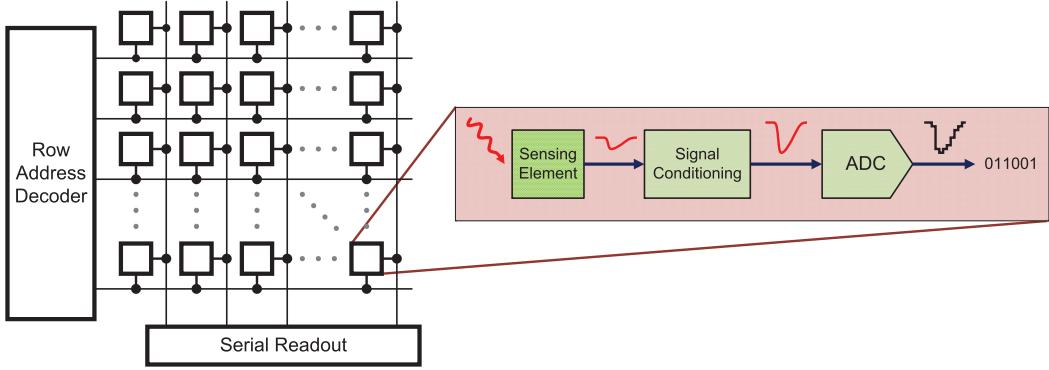
Figure 4.1: *Generic architecture of a CPS integrated with pixel-level ADCs.*

- **LSB**

  The preliminary LSB is set to 1 mV which is equal to the noise of sensing element. This value may be pessimistic, and can be relaxed according to the results from the experiments. For an ADC resolution of 3-bit, the dynamic range is 8 mV.

- **Power consumption**

  Calculating from the specifications of the outer layers ILD vertex detector, a power consumption less than ~1 mW/pixel is sufficient. In our design, this item can be derived from the other prototype MIMOSA-31 which is also designed for the same application but the integration of column-level ADCs. Each ADC in MIMOSA-31 dissipates 784 μW at 3 V power supply [1]. Assuming the following relation is established as

$$\frac{P_{total}}{V_{supply}^2} = \text{const} , \tag{4.1}$$

  where P_{total} is power consumption and V_{supply} the power supply. In the 0.18 μm process, the supply voltage for core circuits is fixed to 1.8 V. From Eq. (4.1), the desired power consumption of an ADC can be calculated from that of the MIMOSA-31. Therefore, the power consumption of an ADC should be less than 250 μW. I should mention Eq. (4.1) is valid only for digital circuits, but the calculated result can also provide a reference to guide our design.

- **Reference clock**

  To simplify the setup of test system, the clock is set to 100 MHz to be compatible with the MIMOSA series sensors.

4.2 Sensor architecture

The most obvious characteristic of the CPS with pixel-level ADCs is that an independent ADC is implemented for each pixel (or a group of pixels). A generic sensor diagram is illus-

trated in Fig. 4.1, where the pixel is composed of a sensing element, a signal conditioning circuit, and an ADC. The outputs of the matrix are only in the digital format.

4.2.1 Readout strategy

The readout method is very important for the pixel sensor. Currently, two schemes are widely used in reading out a pixel matrix: rolling shutter and global shutter. Both readout methods can be employed in the CPS with pixel-level ADCs, but exhibit the different influence on frame rate and power consumption.

- **Rolling shutter**
  The operation of rolling shutter originated from the mechanical shutter is commonly used in the digital camera to control the integration time, and further the exposure value. The electronic shutter inheriting the same principle is naturally used to read out CPS.
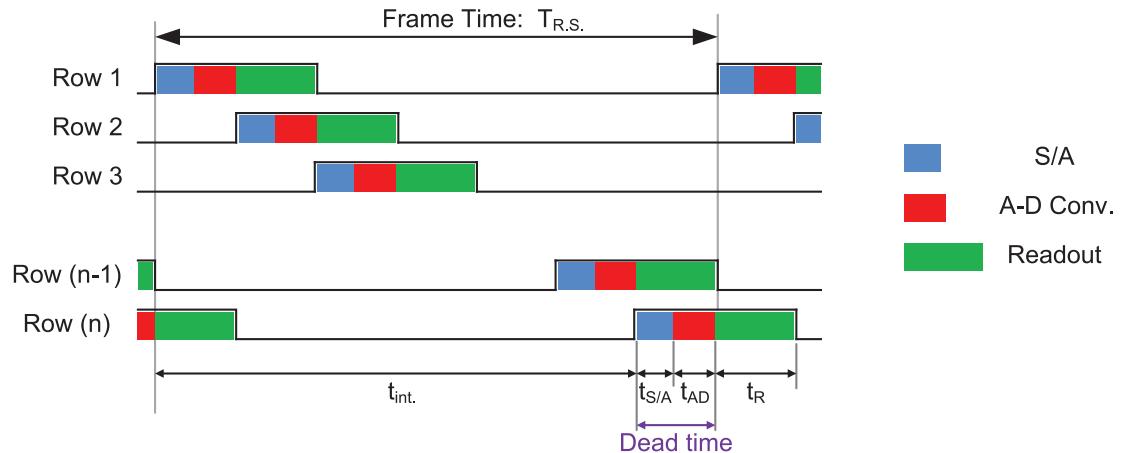
Figure 4.2: Principe of the rolling shutter readout.

As illustrated in Fig. 4.2, in the rolling shutter, the readout starts from the top row of pixels. During the readout, the pixel performs signal sampling and amplification, A/D conversion, and data readout. As soon as all these are finished, the readout shifts to the next row, and then repeats the same operation row by row until the last row is read out.

- **Global shutter**
  The proposition of global shutter initially aims to deal with the image distortion in imaging applications. In global shutter, all the pixels perform sampling and A/D conversion at the same instant, and then the results are saved in the local memories. After the capture, each pixel is sequentially read out row by row that is similar to the rolling shutter mode. The operation of global shutter is depicted in Fig. 4.3.

The rolling shutter and global shutter exhibit different performances in speed, power consumption, and dead time, which are important for CPS. Next, a detailed comparison between
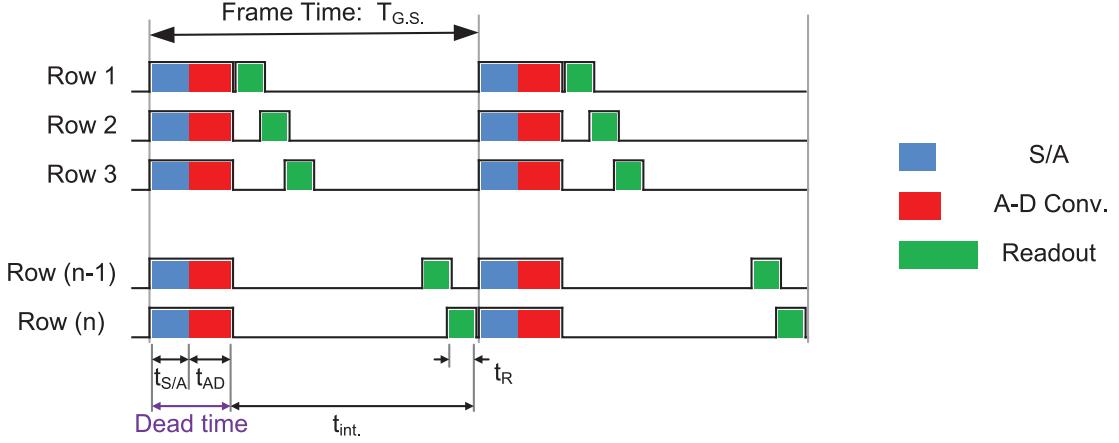
Figure 4.3: *Principe of the global shutter readout.*

them will be presented.

The operation of a pixel with digital output can be categorized into three phases: Sampling/Amplification (S/A), Analog/Digital (A/D) conversion, and readout. In S/A phase, the charge deposited on the sensing diode is sampled and amplified, and then held by the sampling capacitor. During the following A/D conversion phase, this particle signal is digitalized by the discriminator or ADC. At last, the digitalized pixel outputs are read out in sequence during the readout phase.

With respect to a pixel matrix consisting of n rows of pixels, the frame time and the power consumption can be calculated for rolling shutter and global shutter respectively. In the rolling shutter, the frame time $T_{R.S.}$ is given by

$$T_{R.S.} = n \cdot (t_{S/A} + t_{AD}) \,, \tag{4.2}$$

where $t_{S/A}$ and t_{AD} are the time taken by the S/A and A-D conversion, respectively.

The average power dissipated during a frame time is given by

$$
\begin{aligned}
P_{R.S} &= P_{S/A} \cdot n \cdot \frac{t_{S/A}}{T_{R.S.}} + P_{AD} \cdot n \cdot \frac{t_{AD}}{T_{R.S.}} + P_R \cdot n \cdot \frac{t_R}{T_{R.S.}} \\
&= P_{S/A} \cdot \frac{t_{S/A}}{t_{S/A} + t_{AD}} + P_{AD} \cdot \frac{t_{AD}}{t_{S/A} + t_{AD}} + P_R \cdot \frac{t_R}{t_{S/A} + t_{AD}} \,,
\end{aligned}
\tag{4.3}
$$

where $P_{S/A}$, P_{AD} and P_R are the power consumption of one pixel in the phases of S/A, A-D conversion, and readout, respectively. The time spent in the readout phase is t_R.

The t_{AD} varies with the different ADC architectures. Generally, the relation $t_{AD} > t_{S/A}$ is established for the low-to-medium speed ADCs, such as SAR and slope ADCs. The power consumption $P_{S/A}$ is only contributed by the sensing element and S/H amplifier, while P_{AD} has an additional power consumed by the comparator. To reach a high sampling rate, the comparator usually has a large bandwidth but at the cost of a large power consumption.

Consequently, it is reasonable to consider that P_{AD} is much larger than $P_{S/A}$. In the all-digital readout architecture, the power dissipated in the readout phase is so small that it can be ignored. As just mentioned, Eq. (4.3) can be simplified to

$$P_{R.S.} = P_{AD} \cdot \frac{t_{AD}}{t_{S/A} + t_{AD}} \ . \tag{4.4}$$

Using the similar method, the frame time and power consumption can also be calculated for the global shutter mode. Its frame time is

$$T_{G.S.} = t_{S/A} + t_{AD} + n \cdot t_R \ . \tag{4.5}$$

According to the timing diagram shown in Fig. 4.3, the all-digital readout facilitates the t_R to be speedy, whereas for a large matrix with a great number of rows, the last item in Eq. (4.5) is more dominant than other two items. Thus Eq. (4.5) can be rewritten as

$$T_{G.S.} = n \cdot t_R \ . \tag{4.6}$$

The average power consumption associated with the global shutter can be obtained as

$$
\begin{aligned}
P_{G.S.} &= P_{S/A} \cdot n \cdot \frac{t_{S/A}}{T_{G.S.}} + P_{AD} \cdot n \cdot \frac{t_{AD}}{T_{G.S.}} + P_R \cdot n \cdot \frac{t_R}{T_{G.S.}} \\
&= P_{S/A} \cdot \frac{t_{S/A}}{t_R} + P_{AD} \cdot \frac{t_{AD}}{t_R} + P_R \\
&\approx P_{AD} \cdot \frac{t_{AD}}{t_R} \ .
\end{aligned}
\tag{4.7}
$$

From Eqs. (4.2), (4.4), (4.6), and (4.7), we can conclude that in both shutter modes, the following relation is established as

$$T \cdot P = \text{const} \ , \tag{4.8}$$

where T is the frame time, and P the average power consumption of sensor.

Equation (4.8) implies that the product of frame time and power consumption is a constant value no matter which readout method is employed. Consequently, there exists a trade-off between frame rate and power consumption. The single-row rolling shutter and the global shutter represent two extreme cases. The single-row rolling shutter has the lowest power consumption and frame rate. In contrast, the global shutter exhibits the highest power consumption and frame rate. Meanwhile, the case of multi-row readout lies in between the above two extremes.

For the sensors equipped on the outer layer of ILD-VTX, the large pixel size relaxes the frame time to $\sim$100 μs. Nevertheless, a stringent requirement of power consumption is desired to minimize the material budget contributed by the additional cooling components. Therefore, in our design, the single-row rolling shutter is adopted to reach a best power efficiency. For

the future upgrade of high luminosity, the frame rate of rolling shutter can be accelerated further by multi-row readout at the cost of the slightly increase of power consumption.

In addition, there is a great difference in the power distribution between rolling shutter and global shutter. In global shutter, a great number of pixels operating simultaneously draw a large current from the power supply network, thereby leading to a great IR drop. A detailed analysis of this issue will be given in Section 4.4.2.

In conclusion, the readout strategy strongly affects the performances of CPS especially in frame rate and power consumption. Since our design gives the priority to the low power consumption, the rolling shutter readout method is an appropriate choice.

4.2.2 MIMADC-SAR architecture

In the MIMADC-SAR, the SAR ADC is selected to implement the in-pixel data conversion due to its high conversion speed as well as the relatively simple architecture. However, the conventional architecture of the SAR ADC is not optimum in area and power consumption. An improved architecture therefore is proposed to fulfil the requirements of the in-pixel integration. This section starts from a review of the conventional SAR ADC architecture, and then the proposed architecture is presented.

4.2.2.1 Conventional SAR ADC architecture

As illustrated in Fig. 3.7, in a typical SAR ADC, the references compared with the input signal is generated by the DAC. The binary weighted charge-redistribution (CR) structure as shown in Fig. 4.4 is widely used to constitute the DAC in SAR ADCs. Several merits are resulted from this CR-based DAC. First, the principe of the CR DAC relies on charging and discharging the binary weighted capacitor array. Hence, no static current is consumed during its operation. Second, the capacitors can be implemented with a standard CMOS process, and meanwhile the area can be scaled down due to the promotion of process. However, the matching of the capacitors restricts the resolution of DAC, and then affects the ADC performances. It is well-known that the mismatch of capacitors is mainly given by the precision of process, and inversely proportional to the occupied chip area. As a result, the precision of the ADC can be improved by enlarging the area of capacitors, but at the expense of large area, input capacitance, and static power consumption.

For an n-bit SAR ADC with the CR-type DAC, the number of the unit capacitor N_{cap} is increased exponentially with the resolution as

$$N_{cap} = 2^n .$$
(4.9)

For a resolution of 3-bit, total $2^3 = 8$ units of capacitors are required. In the TowerJazz 0.18 μm CIS process, only the MIM capacitor is provided, and the design rule limits the minimum
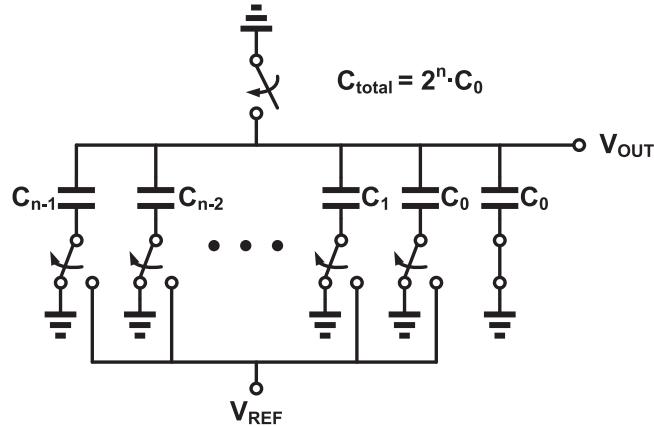
Figure 4.4: A typical scheme of binary weighted charge-distribution DAC.

capacitor area to be 4×4 µm^2. The 8-unit MIM capacitors will occupy more than 128 µm^2 pixel area. Even worse, this process forbids placing devices below the MIM capacitor as well as routing on top of it. Consequently, implementing the CR DAC in the pixel will worsen the layout congestion.

The SAR logic controls the ADC operation to conform the binary weighted search algorithm. In the 0.18 µm process, the large size of the digital standard cell also results in a large area occupied by the SAR logic.

In brief, the DAC and SAR logic existing in the conventional SAR ADC occupy large chip area, which is unacceptable for pixel-level ADCs. In the MIMADC-SAR, an improved architecture was proposed to solve these drawbacks.

4.2.2.2 Proposed CPS with pixel-level SAR ADCs

As discussed above, the conventional DAC and SAR logic circuit occupy a large chip area, preventing the in-pixel integration. Therefore, the major challenge in terms of pixel-level SAR ADCs is how to implement the DAC and SAR logic within an area-limited pixel. In order to solve these issues, an improved architecture has been proposed. The concept is to maximize the circuit reuse among the various pixels. Some circuit blocks which can be shared by all pixels is relocated from pixel to the column-ended or even on-chip. As a consequence, only the minimum and necessary circuits are remained in pixel.

According to this concept, a circuit based on analog multiplexer is used to reach a compact in-pixel DAC. In our design, the resolution of ADC is only 3-bit, and only $2^3 - 1 = 7$ reference levels are demanded in comparison. The limited number of references allow us to generate these 7 references by the on-chip voltage source or even input from test board. The references are then distributed to each pixel and shared by them. In the pixel, an analog multiplexer acts as a DAC to select one reference according to the digital control signals. As a result, the large capacitor array required by the conventional CR DAC can be replaced by several small MOS

switches, greatly reducing the occupied pixel area.

Inspired by the architecture of column-level ADCs, the SAR logic can be moved to the end of column to free the pixel area. In rolling shutter, the pixels are read out row by row, hence the column-shared SAR logic is allowed. Although the SAR logic is not realized in pixel, the output of the pixel is remained to be digital. The advantages of the pixel-level ADCs mentioned previously are still effective in this architecture.
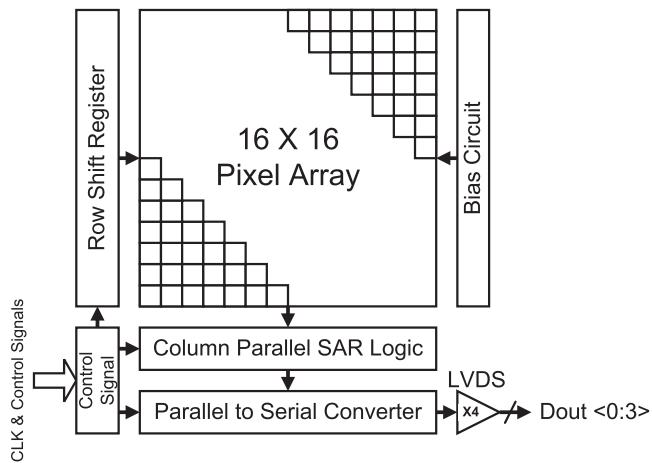
Figure 4.5: *Architecture of the MIMADC-SAR pixel matrix.*

The architecture of the MIMADC-SAR is shown in Fig. 4.5, where the matrix is composed of the 16×16 pixels. The row shift register circuit drives the sensor operating in the rolling shutter mode. The digitalized pixel outputs are formatted by the parallel-to-serial circuits and then transmitted via the LVDS links.

The block diagram of this sensor is shown in Fig. 4.6, and the principle of operation is given as follows. During the integration time, the electrons released by the incident particles are collected by the reverse-biased diode. If the row is activated, the voltage signal integrated on the capacitor of the sensing diode is amplified by the following in-pixel amplifier, and then sampled and amplified further by the S/H amplifier. The output of the S/H amplifier gets compared with the DAC output to generate the binary code. Meanwhile, this code is feed into the SAR logic via a column bus. The state machine in SAR logic outputs the 7-bit one-hot codes, and then feed them back to drive the in-pixel DAC for the next comparison period. As soon as the A-D conversion is finished, the 3-bit ADC result saved in the SAR logic are read out serially. Figure 4.7 illustrates the readout structure. The output data format is compatible with the MIMOSA-31 for sharing a similar test system.

The timing of the rolling shutter is depicted in Fig. 4.8, where the signal "Pwr_on" is the power for the sensing element, and "Sel_row" is for the rest of circuits, including the S/H amplifier, DAC, and comparator. There exists an overlap of the "Sel_row" signals between two neighboring rows. This additional time reserved for the sensing element provides a sufficient time for the circuit reaching the stable state before the following signal processing.
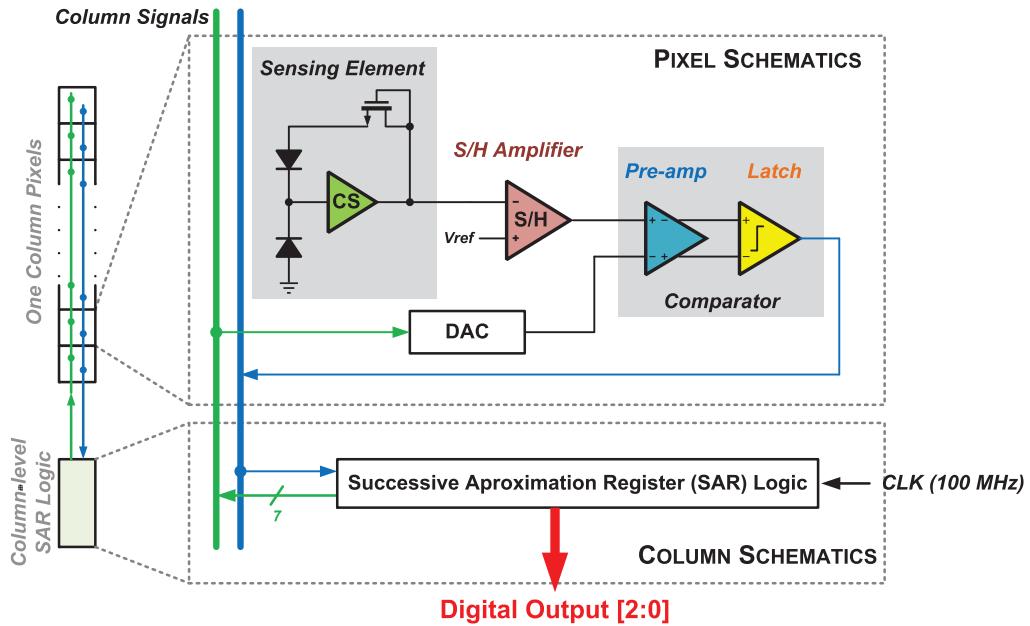
Figure 4.6: *Block diagram of MIMADC-SAR circuits. Only one column pixel as well as the corresponding column-ended SAR logic is shown. The pixel circuits is composed of a sensing element, an S/H amplifier, a comparator, and a DAC. The comparator consists of a pre-amplifier and a latch. The pixel and the column-ended SAR logic are connected via a data bus.*
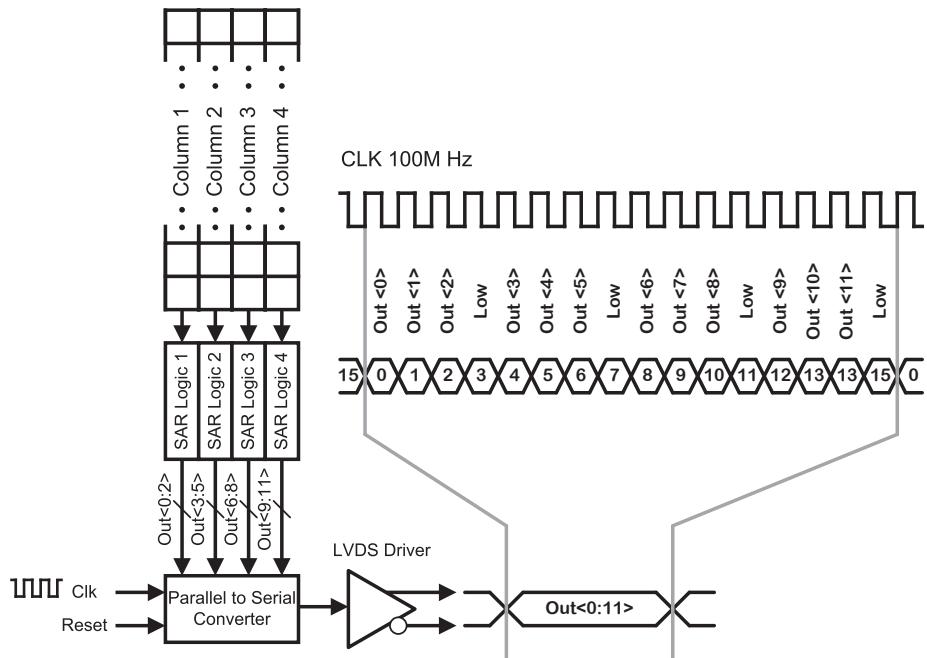
Figure 4.7: *Scheme of the data readout. Every 4 columns are grouped and transmitted by a parallel-to-series convertor together with a LVDS link at a speed of 100 Mbps*
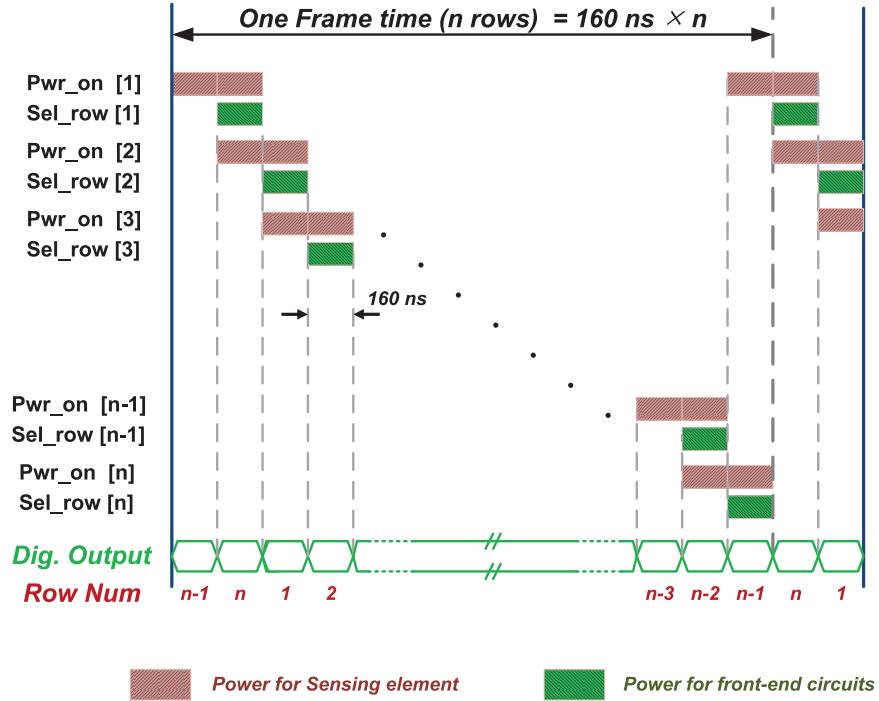
Figure 4.8: *The timing of the rolling shutter mode in MIMADC-SAR. The "Pwr_on<n>" is the power-on signal only for sensing element in n^{th} row, and "Sel_row<n>" is for the S/H amplifier, DAC, and comparator.*

4.3 Design of building blocks

In this section, the design and simulation results of the main building blocks are discussed in detail.

4.3.1 Sensing diode with in-pixel amplifier

The sensing diode together with the following in-pixel amplifier, referred to as "sensing element" in this thesis, converts the collected charge to the electrical signals which can be processed by the electronics. It determines some key specifications of CPS such as SNR, CCE, and radiation tolerance. In the MIMADC, the design of the sensing elements is referred to that in the MIMOSA-32Ter which is designed by A. Dorokhov. Therefore, a brief introduction is presented here, and the reader interested in this aspect can find proofs in [2–7].

The design of the sensing element should follow the targets:
- to maximize the SNR for a given sensing architecture;
- to minimize the power consumption;
- to reduce the pixel-to-pixel dispersion due to process variation and ionizing radiation.

Improving the SNR is the primary task for the sensing element, which determines the detection efficiency ϵ_{det} and the average fake hit rate FH_{rate}. The output signal is decided

by the voltage generated at the diode node as well as the voltage gain in the following in-pixel amplifier. Without considering the leakage current of the sensing diode, the noise is only contributed by the in-pixel amplifier. In consequence, to promote the SNR relies on the reasonable designs of both sensing diode and amplifier.

In the silicon-based pixel sensors, a variety of diodes can be used for collecting the charges introduced by the impinging particles. The pinned diode featuring a lightly doped intrinsic region between a heavily doped p- and n-type silicon, is widely used as the photodiode. Because the pinned diode depends on the charge transmission in the pixel, its performance is sensitive to the radiation, which prevents the pinned diode from the use in the high radiation circumstance. In the CPS adapted to particle tracking, the n-well/p-epi diode is suitable due to the low diode capacitance as well as the prominent performances on noise and conversion gain.

Thermal diffusion is the dominant mechanism of the charge collection in CPS. For a given depletion depth, the quantity of the charge collected by a diode, i.e. $Q_{collected}$, strongly depends on the size of the sensing diode. Enlarging the diode can promote the probability in the charge collection, but at the cost of a large diode capacitance, hence a small CVF. These is a trade-off between $Q_{collected}$ and CVF. In order to maximize the output voltage, an optimization in diode size exists. The studies for the various diode-topologies show that a medium size sensing diode ($\sim$10 µm^2) can reach a balance in both the charge collection efficiency and conversion gain [2]. On the basis of the studies of the MIMOSA-series sensors, an octagonal n-well/p-epi diode is implemented in our design with the area of $\sim$10.96 µm^2.
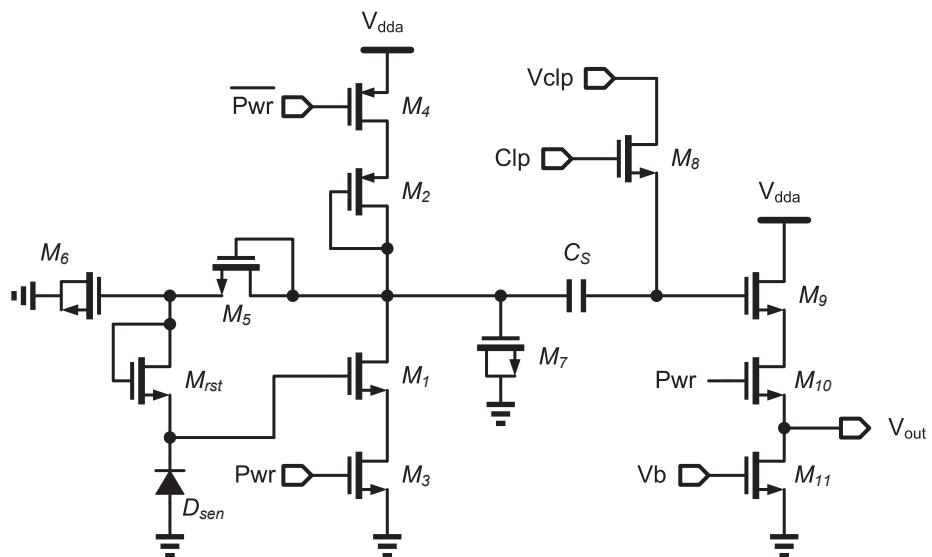
Figure 4.9: *Schematic of the sensing diode together with the in-pixel amplifier.*

The schematic of the sensing element is presented in Fig. 4.9, where it encompasses a sensing diode, an in-pixel amplifier, as well as a source-follower. The voltage deposited on the diode is amplified by the in-pixel amplifier to reach a sufficient amplitude. The source-follower

drives the large capacitance load from the next circuits.

As the first-staged amplifier in the whole pixel circuits, the in-pixel amplifier contributes the most noise than other circuits. Moreover, the longest power-on period also calls for a restriction of power consumption. Benefiting from the small voltage swing range existed at the diode node (typically few mV), the common-source (CS) amplifier is an appropriate choice due to its merits on power consumption and noise.

The deep p-well available in the Towerjazz 0.18 μm process allows us to use the PMOS in the pixel. The in-pixel amplifier consists of the a NMOS (M_1) as the input stage, and a PMOS (M_2) as load. The transistors (M_3 and M_4) act as switches to power off the circuits during the integration time. A diode-connected transistor (M_{rst}) compensates the leakage current of the sensing diode (D_{sen}), and meantime removes the pedestal voltage remained by the previous incident particles.

However, some drawbacks are exhibited by the CS in-pixel amplifier and the leakage current compensation circuits. Firstly, gain, noise, and power consumption of the CS amplifier are sensitive to the DC operation points. Any parameter variation in the CMOS process is directly translated into the dispersions of the output response among the pixels, and then results in a large FPN. In addition, since leakage current compensation is uniform to all diodes, the dispersion of the leakage current resulting from the irradiation also contributes to the FPN. To deal with these drawbacks, a structure enhanced by the negative feedback and self-bias is introduced.

The negative feedback path consisting of the transistor M_5 and the MOS capacitor C_{M6} formed by M_6, constitutes a low-pass filter to bias M_{rst}. The low-frequency negative feedback stabilizes the DC operation point of the diode node to compensate the variation of the fabricated process. The time constant of this low-pass filter is C_{M6}/g_{m5}. Increasing the time constant is more efficient to filter the noise which is fed back to the diode D_{sen}. In conclusion, this architecture is less sensitive to the operational point variations resulted from the process variation and the radiation effect.

To limit the noise at the output of CS amplifier, a small MOS capacitor (M_7) is added to reduce the bandwidth. The capacitor C_0 and clamping switch transistor M_8 carry out the CDS to provide an stable operation point for the following buffer. The source-follower buffer comprised of M_9-M_{11} is used to drive the large input capacitance of the following S/H amplifier.

4.3.2 Sample-and-hold amplifier

The CVF of the sensing element is typically $\sim 50\,\mu V/e^-$. The LSB of $20\,e^-$ only corresponds to an output voltage ~ 1 mV. This value is so small that cannot be digitalized directly by the ADC. An amplification is required to provide a sufficient amplitude to meet the input range of the ADC. In addition, a sampling circuit is indispensable for the ADC to quantize the input signal in the time domain. Both functions can be realized by a sample-and-hold (S/H)

amplifier. In contrast to the in-pixel amplifier in sensing element, the S/H amplifier ask a relaxed noise requirement because of a large input, but a higher linearity is demanded. Next, a detailed analysis of this circuit will be presented.

4.3.2.1 Specifications

The main specifications are explained as follows

Gain   The choice of gain value depends on the features of the input signal and the dynamic range required by the following ADC. In our design, the LSB is set to an ENC ($\sim$20 e$^-$) achieved from the sensing element, corresponding a input voltage of the S/H amplifier in the range of 1-2 mV. This signal amplified by the S/H amplifier should be large enough to suppress the noise from the comparator and the DAC. Meanwhile, the maximum gain is restricted by the dynamic range of the ADC. As a consequence, a gain in the range of 4–10 is appropriate.

Offset   In our design, the operational point of the S/H amplifier can be set by the external reference voltage input from the board. Thus the offset can be compensated manually. Although the offset value of each pixel is not important, but the dispersion of that, i.e. FPN should be minimum. The CDS technique is used to remove the offset.

Noise   The low noise design is crucial to maintain a high SNR, especially for the weak signal detection. The noise of S/H amplifier should be less than that of the sensing element in order to achieve a reasonable SNR.

Linearity   According to the center of gravity algorithm, the position of the particle is decided by the sum of the weighted factor times the coordinate of each pixel in a cluster, where the weighted factor is the ADC output of the pixels. A linear weighted factor is crucial for establishing a correspondence relation between the collected charge number and the ADC output. Any deviation in the linearity will result in an error in the position of incident particles. Therefore, a good linearity is essential for the ADC design.

In addition, other specifications such as low power and small area are also required in the design.

4.3.2.2 Architecture selection

The architectures of S/H amplifier can be categorized into two types: the open-loop structure and the closed-loop structure.
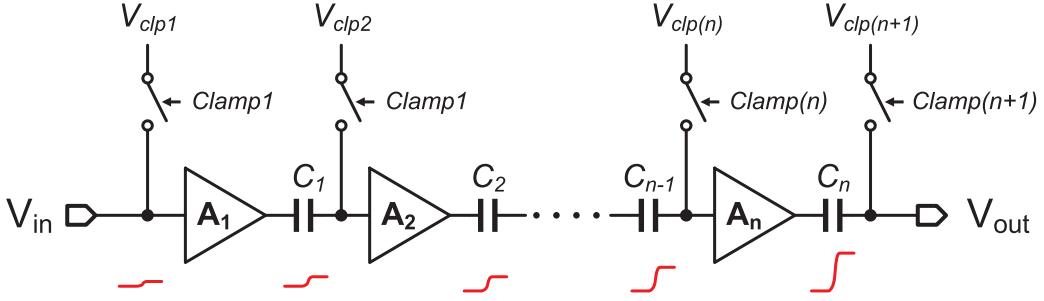
Figure 4.10: *A typical open-loop S/H amplifier, features a multi-stage, cascaded amplifier. The inter-stage switches and capacitors perform the CDS to remove the offset.*

One possible implementation of the open-loop structure is shown in Fig. 4.10, where several low-gain amplifiers are cascaded to form a multi-stage amplifier. This architecture can provide a fast operation speed as well as a high gain. The gain-bandwidth product of a n-stage cascaded amplifier can be obtained as follows

$$GBW_{cascade} = |A_{1-stage,DC}|^{n-1} \sqrt{\sqrt[n]{2} - 1} \cdot GBW_{1-stage} \, , \tag{4.10}$$

where $A_{1-stage,DC}$ and $GBW_{1-stage}$ are the DC gain and the gain-bandwidth gain of single stage amplifier, respectively [8]. The cascading structure extends the gain-bandwidth product as the number of stages increases. Moreover, in a cascaded amplifier, the input noise is mainly decided by the first stage. Benefiting from the low noise of the single-stage amplifier, the total noise of the cascaded amplifier is generally much less than the closed-loop structure. However, the open-loop architecture suffers several drawbacks. A poor linearity is primary. Its gain depends on the parameters of the transistor which generally exhibits a poor linearity. Moreover, its performances are also sensitive to the mismatch of components.

In contrast, the gain of the closed-loop amplifier is only set by the ratio of the passive components. In the modern CMOS process, the ratio of the passive components presents a high precision, and meantime suffers less influence from the process, voltage, and temperature (PVT) variations.

4.3.2.3 Circuit implementation

In the closed-loop amplifier, the passive components used in the feedback circuits can be realized by either resistors or capacitors. Compared with the resistance feedback, the capacitance structure contributes no thermal noise, and the AC coupling allows to set the operational point for the amplifier freely. In addition, the capacitance feedback architecture is compatible to the switched-capacitor circuits.

The architecture of the S/H amplifier employed in our design is illustrated in Fig. 4.11. It
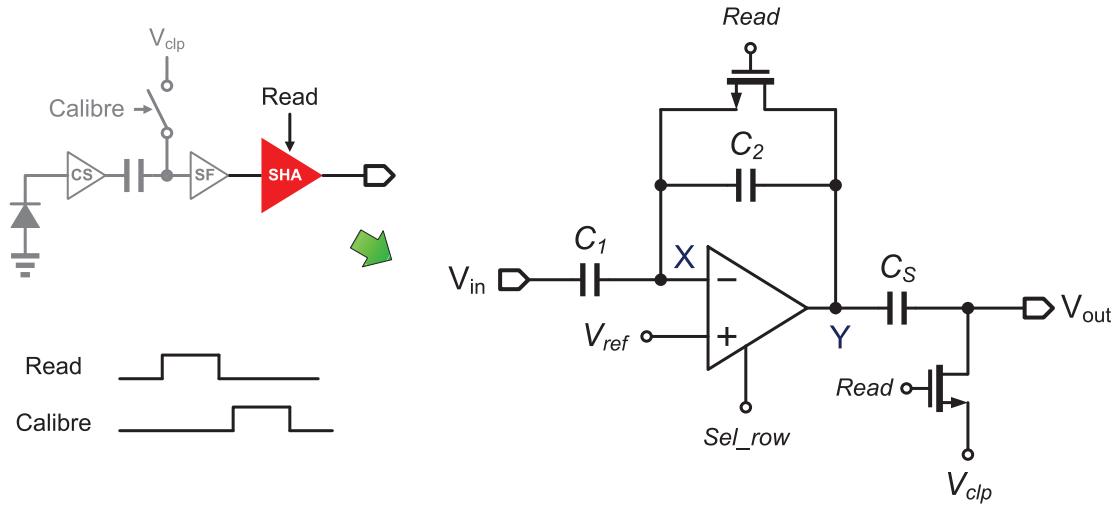
Figure 4.11: *Architecture diagram of the S/H amplifier used in MIMADC-SAR.*

is comprised of an operational amplifier (A_1), and two capacitors (C_1 and C_2). The capacitor C_s is used for the CDS operation.

The timing diagram of the S/H amplifier is also shown in Fig. 4.11. In the "Read" phase, the input signal is deposited on the capacitor C_1. Meantime, C_2 is reset. In the following "Calibre" phase, the input signal is reset by clamping the previous source-follower. The amplifier is operated in the amplification mode, and the charge deposited on C_1 is transferred to the feedback capacitor C_2.

The detailed operation can be analyzed based on the principle of the charge re-distribution. In the "Read" phase, the equivalent circuit of the S/H amplifier is illustrated in Fig. 4.12(a), where the voltage source V_{off} represents the input offset of the operational amplifier A_1. Setting the DC gain of A_1 to A_v, the input/output voltage of A_1 obeys the following relation:

$$(V_{off} + V_{ref} - V_x) \cdot A_v = V_x . \tag{4.11}$$

The charge deposited on the capacitors can be computed as follows

$$\begin{cases} Q_{C1} = (V_{in,read} - V_x) \cdot C_1 \\ Q_{C2} = 0 \\ Q_{Cs} = (V_x - V_{ref}) \cdot C_s . \end{cases} \tag{4.12}$$

During the "Calibre" phrase, the equivalent circuits is depicted in Fig. 4.12(b), and the input/output of A_1 is given by

$$(V_{off} + V_{ref} - V'_x) \cdot A_v = V'_y . \tag{4.13}$$
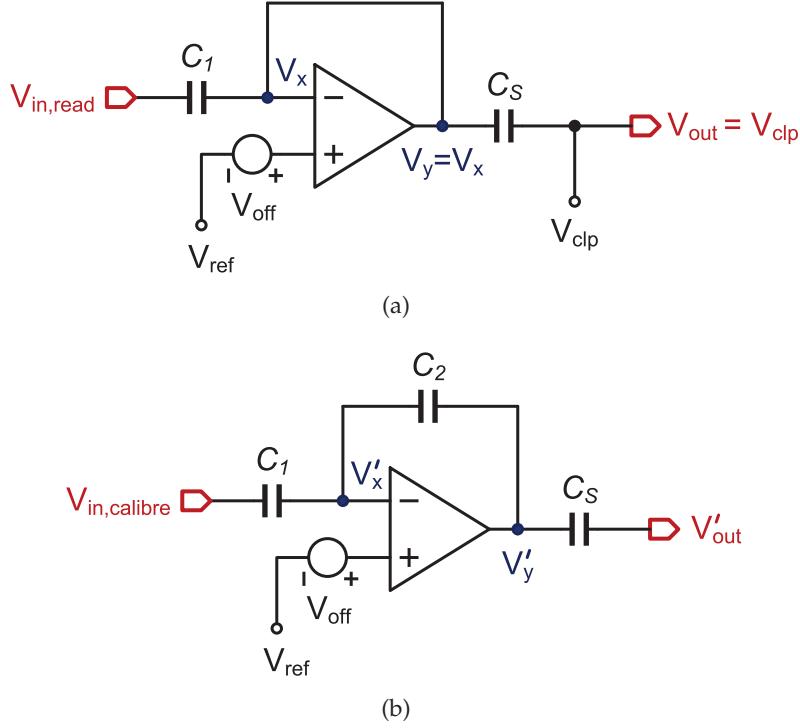
Figure 4.12: *Equivalent circuits of the S/H amplifier in (a)"Read" phase and (b) "Calibre" phase.*

The charges stored in the capacitors are obtained as follows

$$
\begin{cases}
Q'_{C1} = (V_{in,cali} - V'_x) \cdot C_1 \\
Q'_{C2} = (V'_x - V'_y) \cdot C_2 \\
Q'_{Cs} = (V'_y - V'_{out}) \cdot C_s \, .
\end{cases}
\tag{4.14}
$$

According to the charge conversation rule, the total charges stored on the C_1 and C_2 are constant during both "Read" and "Calibre" phases. Similarly, the charge on C_s is also constant. Both of relations can be written as follows

$$
\begin{cases}
Q_{C1} + Q_{C2} = Q'_{C1} + Q'_{C2} \\
Q_{Cs} = Q'_{Cs} \, .
\end{cases}
\tag{4.15}
$$

Substituting Eqs. (4.11), (4.12), (4.13), and (4.14) into Eq. (4.15), in the "Calibre" phrase, the A_1 output node V'_y can be resolved as follows

$$
V'_y = \frac{C_1 V_{in,cali} - C_1 V_{in,read} + (1 - C_1)(V_{off} + V_{ref}) + \frac{A_v}{1 + A_v} C_1 (V_{off} + V_{ref})}{\frac{1 - C_1}{A_v} + C_2} \, .
\tag{4.16}
$$

Since the gain A_v is generally very large, the relations of $(1 - C_1)/A_v \approx 0$ and $A_v/(1 + A_v) \approx 1$

are established. We can approximate Eq. (4.16) to

$$V_y' = \frac{C_1}{C_2}(V_{in,cali} - V_{in,read}) + V_{off} + V_{ref} \ . \tag{4.17}$$

Equation (4.17) indicates this circuit only amplifies the difference of the input signals appearing during the "Calibre" and the "Read" phases, which is the net signal generated by the incident particles. The baseline voltage set by the previous source-follower is removed to reach an uniform output response. The gain provided by the S/H amplifier is only defined by the ratio of two capacitors C_1/C_2 thereby leading to a high accuracy as well as a good linearity.

In Eq. (4.17), the amplified signal is stacked on the voltage of ($V_{off} + V_{ref}$). If A_1 is an ideal operational amplifier, the input offset voltage V_{off} is neglected, and the common-mode voltage is equal to the reference V_{ref}. In practice, the offset voltage V_{off} deviates from the desired value, and the dispersion of V_{off} results in the FPN. Therefore, an additional CDS operation is performed by the capacitor C_s and the associated clamping switch M_s to eliminate the offset due to A_1.

Applying the charge conservation rule to the C_s can obtain

$$V_{out}' = \frac{C_1}{C_2}(V_{in,cali} - V_{in,read}) + V_{clp} \ , \tag{4.18}$$

where V_{clp} is the clamping reference for the CDS operation. From Eq. (4.18) we can obtain the offset voltage V_{off} is completely removed by the CDS, and the baseline voltage is only defined by V_{clp} that can be regulated on board.
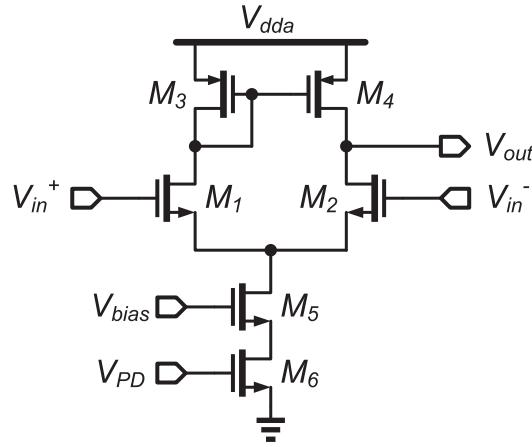
Figure 4.13: Schematic of the operational amplifier in the S/H amplifier.

The performances of the S/H amplifier directly relies on the operational amplifier A_1. For the purpose to limit the noise contributors, a circuit composed of less components is preferred. In addition, the simple structure generally has less current paths, hence exhibits a better power-efficiency. For this reason, as illustrated in Fig. 4.13, an operational amplifier

featuring a differential input and a single-ended output is employed.

As stated before, the noise sources in the CMOS circuits can be categorized into two parts: thermal noise and $1/f$ noise. The low-frequency $1/f$ noise can be reduced by the CDS operation. The thermal noise directly depends on the bias current. In the low-power design, the static current should be minimized, which results in a large thermal noise. Therefore, in order to optimize both noise and power consumption, the priority lies on promoting the utilization of current.

The transconductance over drain current ratio (g_m/I_D) is generally used to judge the current utilization in the CMOS circuits. It indicates the efficiency of translating current, and hence the power consumption, into the transconductance. In the CMOS circuits, the transistor can operate in three region: strong, moderate, and weak inversion. As illustrated in Fig. 4.14, if the current is so small that the transistor is in weak inversion region, the g_m/I_D ratio is saturated and reaches a maximum value. With the increase of inversion, the g_m/I_D reduces progressively. As a result, the transistor operated in the weak inversion region exhibits best power efficiency.
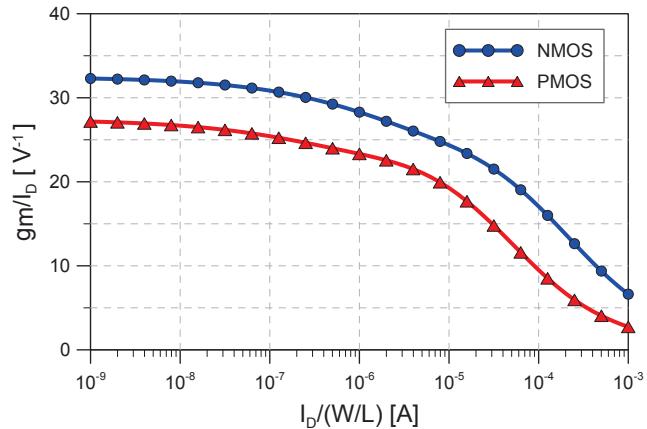
Figure 4.14: *Ratio g_m/I_D at the different bias current for NMOS and PMOS respectively.*

Since the g_m/I_D is an indicator of the region in which the transistor operates, for the convenience of the calculation, the inversion coefficient (IC) is proposed [9]. The IC for a transistor is defined as

$$IC = \frac{I_D}{I_S} . \tag{4.19}$$

Here I_S is the moderate inversion characteristic current given by

$$I_S = \frac{2\mu C_{ox} V_T^2}{\kappa} \cdot \frac{W}{L} , \tag{4.20}$$

where V_T is the thermal voltage with a value $\sim$26 mV. κ is the sub-threshold gate coupling coefficient with a typical value of $\sim$0.7. Derived from the EKV model, the g_m/I_D and IC have

a relation which is valid in all operation regions [10]:

$$g_m/I_D \approx \frac{\kappa}{V_T} \cdot \frac{2}{1 + \sqrt{1 + 4 \cdot IC}} \,. \tag{4.21}$$

By calculating the IC, we can determine a transistor operates in which region. The operational region and the corresponding IC are depicted in Fig. 4.15.
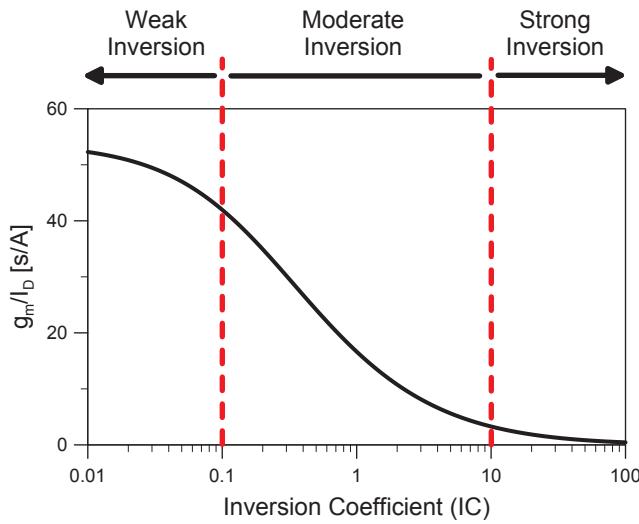
Figure 4.15:
g_m/I_d *versus the inversion coefficient (IC). As IC<0.1, the MOS-FET is in the weak inversion region that $g_m \propto I_D$. As IC>10, it is in the strong inversion region that $g_m \propto \sqrt{I_D}$. As IC ranged between the 0.1 and 10, it is in the moderate inversion region, and the g_m is related between the I_d and $\sqrt{I_D}$.*

The transistor in the weak inversion region has the best power efficiency. But in order to maintain a small bias current density, a large aspect ratio W/L and hence a large area is required. The moderate inversion region can provide an interesting compromise [11]. The current is smaller than that in the strong inversion, and the aspect ratio W/L is more acceptable than weak inversion. Moreover, for a given current, its transconductance g_m is only slightly less than that in weak inversion. Therefore, the moderate inversion region is suitable to our design.

Table 4.1 lists the operational points of the op-amp A_1 in the S/H amplifier.

Devices	W/L (μm)	I_D (μA)	Inversion coefficient	g_m/I_D (V^{-1})
M_1, M_2	9.0/1.0	14.7	2.55	15.42
M_3, M_4	3.5/0.5	14.7	18.31	6.48
M_5	3.0/0.5	29.4	10.46	8.71

Table 4.1: Transistor aspect ratios and operational points of the op-amp used in the S/H amplifier. The IC and the g_m/I_D of each transistor are calculated according to the simulation results.

Generally, the input transistors contribute the most noise, thus they are biased in the moderate inversion region with the IC of ∼2.55. Additionally, aiming to reduce the offset, the transistor length L of M_1 and M_2 should be at least 3–5 times of the feature size. In order to reach high current efficiency, low noise, and small transistor size, input transistors M_1 and

M_2 are operated in moderate inversion region. The strong inversion region is chosen for the current-mirror loads M_3 and M_4 to achieve a reasonable output swing range. Transistor M_5, as a current source to bias the operational amplifier, contributes much less noise. Taking into account a large output impendence as well as an acceptable area, M_5 is biased in the boundary of moderate and strong inversion region.

The simulation results of the operational amplifier A_1 shown in Fig. 4.13 is summarized in Table 4.2. The open-loop gain is $\sim$42 dB (125.9 V/V) leading to a gain error $<$ 3 %.

Parameter	Value
Gain@DC	42.05 dB
-3dB Bandwidth	2.04 MHz
Phase margin	55.89 $^\circ$
Common-mode input range	0.627–1.8 V
Output range	0.107–1.657 V
Offset	2.077 mV
Static current	29.4 µA

Table 4.2: *Summary of the simulation results for the op-amp in S/H amplifier. The output load is a 120 fF capacitor and the offset is calculated via 500 Monte-carlo simulations.*

4.3.2.4 Noise analysis

The noise analysis is divided into two parts. In the first part, the equivalent input noise only for the operational amplifier is calculated. Then, in the second part, the feedback capacitors are included to access the total noise of the S/H amplifier.
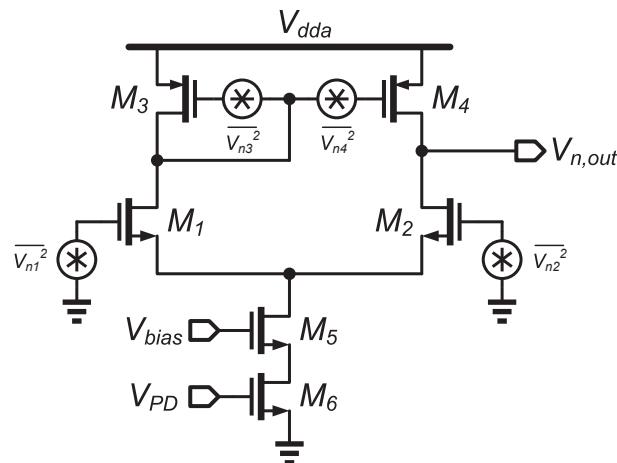
Figure 4.16: *Noise equivalent model for the operational amplifier in the S/H amplifier.*

The noise equivalent model for the op-amp A_1 is illustrated in Fig. 4.16. For each transistor, both thermal noise and $1/f$ noise are represented by a noise voltage source connected serially

at the gate of the transistor. The input-referred noise of this op-amp can be represented by a thermal noise item and a $1/f$ noise item respectively:

$$\overline{V^2_{n,total}} = \overline{V^2_{n,thermal}} + \overline{V^2_{n,1/f}} . \tag{4.22}$$

In Eq. (4.22), the first item only contributed by the thermal noise is given by

$$\overline{V^2_{n,thermal}} = \frac{32}{3}kT\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g^2_{m1}}\right) , \tag{4.23}$$

and the $1/f$ noise item can be written as

$$\overline{V^2_{n,1/f}} = \frac{2}{C_{ox}}\left(\frac{K_N}{W_1 L_1 f} + \frac{K_P}{W_3 L_3 f}\frac{g^2_{m3}}{g^2_{m1}}\right) . \tag{4.24}$$

From Eqs. (4.23) and (4.24) we can see that if we set the transistors to be $g_{m3} \ll g_{m1}$, the noise contributed by M_3 and M_4 can be minimized. Because the current passing M_1, M_2 are equal to M_3, M_4, we can size the transistors by $(W/L)_3$, $(W/L)_4 \ll (W/L)_1$, $(W/L)_2$. The transistors M_1, M_2 are operated in the weak inversion region, and M_3, M_4 are biased in the strong inversion region. The transistor size listed in Table 4.1 agrees with the above conclusion in the noise analysis. In addition, since the electron mobility in NMOS is normally 2–3 times higher than the hole mobility in PMOS, for a given current and aspect ratio, the transconductance of NMOS is larger than that of PMOS. Therefore, NMOS are selected as the input transistors and PMOS as the loads, which is in favor of reducing the noise.

In the closed-loop amplifier, the feedback network also affects the noise performance. The input-referred noise of the S/H amplifier is given by

$$\overline{V^2_{n,preamp}} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 \cdot \overline{V^2_{n,total}} , \tag{4.25}$$

where C_{in} is the parasitic capacitance at the gate of the input transistor M_1.

As indicated in Eq. (4.25), the capacitance feedback structure increases the input noise by an attenuation coefficient $[(C_1 + C_2 + C_{in})/C_1]^2$. This effect can only be ignored if $C_1 \gg C_2$, C_{in}. However in our preamplifier, this condition cannot be established because of the limitations of the small pixel area and the desired closed-loop gain. The parasitic capacitor C_{in} not only increases the noise, but also acts as a voltage divider to attenuate the input signal. Based on the simulation, the aspect ratio of W/L=9 µm/1 µm is chosen for the input transistors, which corresponds to the $C_{in} \sim$30 fF. The capacitors C_1 and C_2 are set to 130 fF and 30 fF respectively. The attenuation coefficient of the input noise is $\sim$2.13, which means the feedback network doubles the input noise power of the op-amp A_1.

Figure 4.17(a) is the input-referred noise of the op-amp A_1 via the small-signal noise simulation. Within the frequency range from 1 mHz to 1 GHz, the input-referred noise voltage is
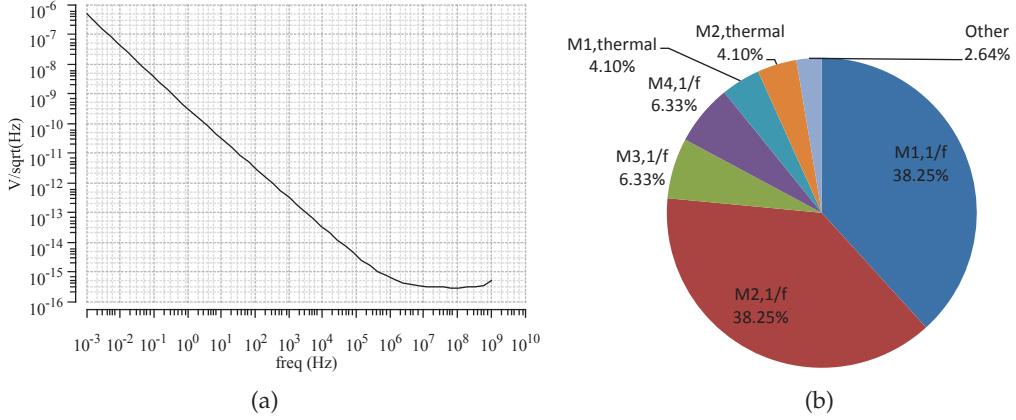
Figure 4.17: *Simulation results of the noise of the op-amp in the S/H amplifier: (a)the input-referred noise, and (b) the noise contribution of each transistor.*

equal to ~0.196 mV. The noise contribution of each transistor is drawn in Fig. 4.17(b). Since the gate area of all the transistor is limited, the $1/f$ noise is dominated. By sizing the transistors M_3 and M_4 in the strong inversion region, the associated noise contribution is much less than the input transistors.

The noise of the S/H amplifier can be evaluated by the transient noise simulation (TNS). Total 1000 times TNS was performed within the same frequency range as the previous AC noise simulation. The simulated rms noise is ~1.747 mV. Considering the gain of $C_1/C_2 \approx 4.3$ obtained by the simulation, the input-referred noise is ~0.406 mV.

The input noise of the S/H amplifier is larger than the noise of the op-amp. The attenuate coefficient is ~2.07, which well agrees with the estimated value of ~2.13 according to the above analysis.

4.3.3 Pre-amplifier in comparator

The Comparator, as an indispensable block, exists in all kinds of ADCs to quantize the analog signal into the digital code. The comparator should follow some fundamental requirements given as [12]:

- high resolution to discriminate a small differential input;
- fast conversion rate to minimize the propagation delay;
- large dynamic range to match the various input signals;
- small offset dispersion;
- small kickback noise coupled from latch to pre-amplifier.

A typical operational amplifier featuring a high open-loop gain can be used as a simple comparator, but the slow response prevents it from the high-speed application. As given in Fig. 4.18, a high-speed comparator is generally composed of a pre-amplifier and a latch. This architecture offers a faster response speed as well as a good resolution. The small differential
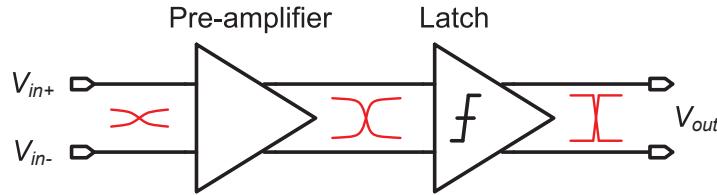
Figure 4.18: *A typical comparator architecture. It is comprised of a pre-amplifier following a latch.*

input is firstly amplified by the pre-amplifier in a logarithmic response, and then extended further to the power rails at an exponential rate. The total response time of this achitecture is much less than using the pre-amplifier or latch only.

The pre-amplifier is a crucial block that determines the performance of the comparator. Firstly, the resolution of the comparator is limited by the offset and the noise from the latch. The large gain provided by the pre-amplifier can compensate the influence of this offset and noise. In addition, the high-speed latch will generate kickback noise coupling to the previous circuits. The pre-amplifier can isolate the latch from the previous circuits such as S/H amplifier to prevent the disturbance due to the kickback noise.

With respect to the pre-amplifier, the design focuses on the high gain and the fast response, and meanwhile the linearity can be relaxed. The cascaded amplifier which can easily reach a high gain-bandwidth product, is widely used to implement the pre-amplifier.

4.3.3.1 Specifications

The main specifications of the pre-amplifier are explained as follows:

Gain In comparator both offset and noise can trigger the latch to toggle a wrong code. So the signal input to the latch should be large enough to compensate the errors due to the offset and the noise. The smallest input signal which can be distinguished by the comparator is expressed as follows

$$|V_{in}| = |V_{dis}| + |V_{off}| + |V_n| \, , \tag{4.26}$$

where V_{off} and V_n are the input offset and noise for the latch respectively. V_{dis} is the least input voltage that can be discriminated by an ideal latch. Assuming the distribution of offset and noise are Gaussian, to remain a small error code probability, the value of V_{off} and V_n in Eq. (4.26) are selected to be 3 times of their standard deviation, corresponding to the error code probability less than 10^{-6}.

In the standard CMOS process, the V_{off} of latch is much larger than V_n and V_{dis}. In a typical dynamic latch, the offset may be up to 30 mV. To guarantee no code loss, the resolution of the comparator used in ADCs is limited to $1/2 \cdot LSB$ which is translated into $\sim$2 mV in our design. Instituting this value into Eq. (4.26), the required gain is $\sim$15.

Speed   The settling time of the pre-amplifier determines the conversion speed of the comparator. Since the input signal features a small amplitude and a limited dynamic range, it is reasonable to assume that the pre-amplifier is operated in the small signal region. So the settling time is mainly limited by the bandwidth. In the MIMADC-SAR, the conversion time preserved for the comparator is only 2 clock cycles, i.e. 20 ns. The required bandwidth of the amplifier can be calculated by the classic equation as

$$BW \cong \frac{0.35}{t_r} \ . \tag{4.27}$$

Assuming the rise time t_r is the half of the conversion time, the bandwidth is computed to be $\sim$35 MHz.

4.3.3.2 Architecture selection
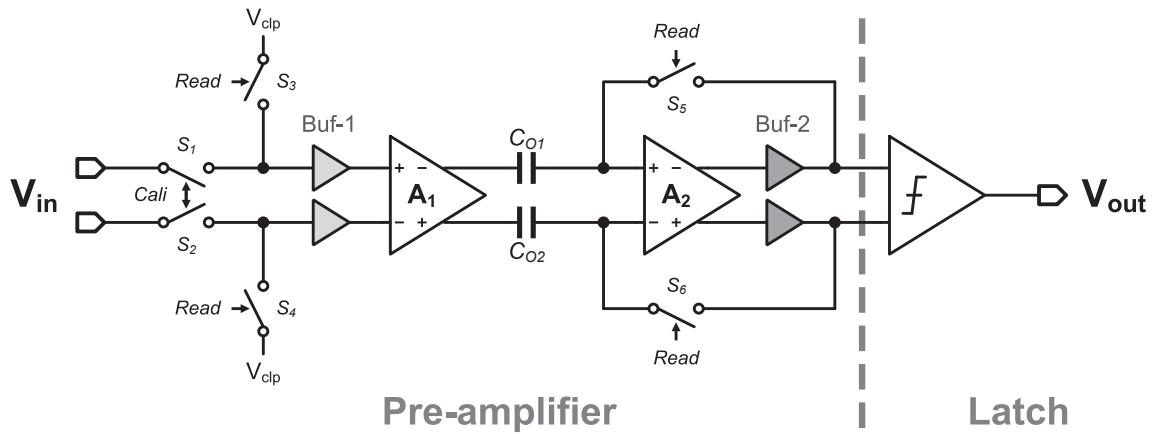
Figure 4.19: *Block diagram of the comparator. It is composed of an offset-compensated pre-amplifier and a latch.*

Figure 4.19 presents the proposed architecture of the comparator. As stated before, the required gain of the pre-amplifier is $\sim$15. Therefore a cascaded architecture of two amplifiers is used, and each amplifier exhibits a voltage gain $\sim$4. The pre-amplifier is composed of two low-gain amplifiers (A_1 and A_2), two pairs of buffers ("Buf-1" and "Buf-2"), two coupling capacitors (C_{O1} and C_{O2}) and several switches. An offset compensated architecture is employed to reduce the offset of the amplifiers A_1 and A_2. The buffers are added to reduce alleviate the effects from the input feedthough and the kickback noise. The principles of these structures will be discussed in details in this section.

Offset cancellation: The high-precision comparator demands offset cancellation in the pre-amplifier. Because of the compatibility to the switched-capacitor circuits, the techniques of the input-offset suppression (IOS) and the output-offset suppression (OOS) are generally used to remove the offset of the pre-amplifier [12].

Considering the pros and cons of the IOS and OOS, the pre-amplifier of our design hybridizes both techniques: the amplifier A_1 adopts the OOS, and A_2 uses the IOS. The architecture displays several merits than using unique type of offset suppression technique. Firstly, the OOS provides a perfect removal of the offset in the amplifier A_1, as well as an excellent attenuation of the charge injections contributed by the switches. Moreover, with respect to the second amplifier A_2, the input bias is generated by unit-gain connection of the amplifier during the cancellation phase. This self-bias guarantees A_2 operating in the proper region in the amplification phase. Last, this structure only one pair of coupling capacitors C_{O1} and C_{O2} is required, which saves a large pixel area.

The operation of the pre-amplifier can be divided into three phases: cancellation, amplification and latch phases. In the cancellation phase , signal "Read" is high and "Cali" is low, which results in S_3–S_6 are on and S_1, S_2 off. The amplifier A_2 is connected to the unit-gain mode. The offset voltages of the A_1 and A_2 are stored on the positive and negative plates of C_1 and C_2. Then in the following amplification phase, the sampling switches S_1 and S_2 are on and the rest ones are off. Both A_1 and A_2 amplifies the input differential signal in open-loop mode. As soon as the output of the pre-amplifier is stable, the latch toggles the amplified signal and generates the corresponding digital code.

The transfer function of the pre-amplifier can be calculated at the all the all three phases based on the charge conservation principle (the detailed calculation of the this transfer function is in Appendix B). The output voltage of the pre-amplifier at the end of amplification phase is

$$V_{out} = A_{v1}A_{v2} \cdot V_{in} - \frac{A_{v2}}{1 + A_{v2}} V_{OSA2} + A_{v2}\left(\frac{q_5}{C_{O1}} - \frac{q_6}{C_{O2}}\right), \tag{4.28}$$

where A_{v1} and A_{v1} are the open-loop gain of amplifier A_1 and A_2 respectively. V_{OSA2} is the input offset voltage of A_2. The charges q_5 and q_6 are due to the charge injection from the switches S_5 and S_6.

As given in Eq. (4.28), the differential input signal is amplified by both A_1 and A_2. However, an offset is also introduced by the amplifiers and switches. In the case that coupling capacitors C_{O1} and C_{O2} are perfectly matching (i.e. $C_{O1} = C_{O2} = C_O$), and the offset of the latch is also considered, the equivalent input offset of the pre-amplifier can be obtained:

$$V_{OS,in} = -\frac{V_{OSA2}}{A_{v1}(A_{v2}+1)} + \frac{\Delta q_{5,6}}{A_{v1}C_O} + \frac{V_{OSL}}{A_{v1}A_{v2}}, \tag{4.29}$$

where $\Delta q_{5,6}$ is the charge injection mismatch between S_5 and S_6, and V_{OSL} is the offset of the latch.

As indicated in Eq. (4.29), the offset of A_1 and the mismatch of the charge injection from S_1–S_4 are perfectly removed, since the OOS is applied to the first stage amplifier A_1. Furthermore, the offset of the A_2 is greatly attenuated by the gains of both A_1 and A_2. The offset contributed by the charge injection mismatch from S_5 and S_6 depends on the coupling capacitor. Thus

the MOS capacitor is used to implement these capacitors for a high value. Additionally, as mentioned previous, the offset of the latch is reduced by the gain of the pre-amplifier.
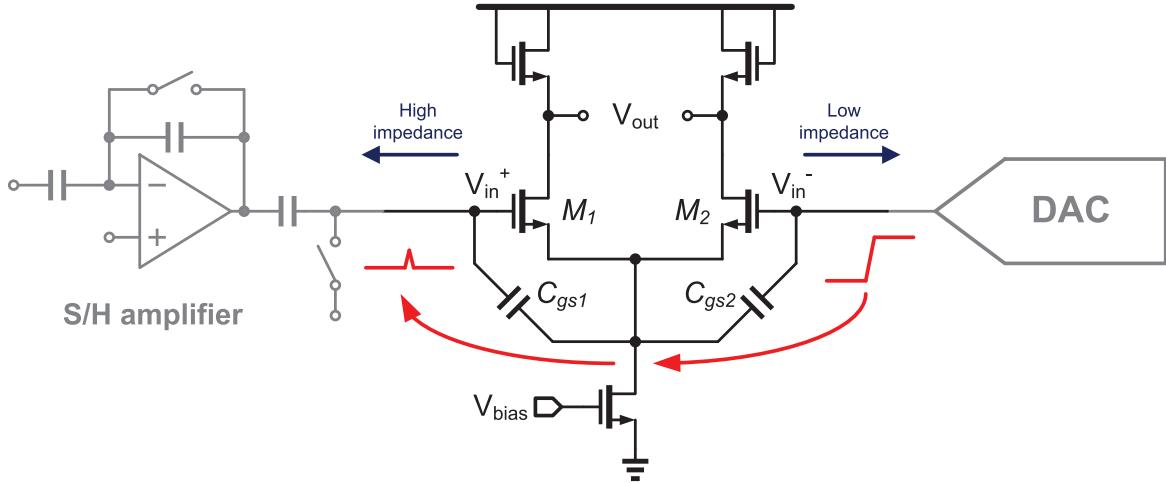
Figure 4.20: *Principle of the input feedthrough. Both input ports of the first-stage amplifier in the pre-amplifier are connected to the outputs from the S/H amplifier and the DAC respectively.*

Input feedthough: The input feedthrough existing at the input ports of the pre-amplifier may degrade the accuracy of the signal sampled by the comparator. As illustrated in Fig. 4.20, the signals input to the amplifier A_1 (shown in Fig. 4.19) are generated from the S/H amplifier and the DAC respectively. In MIMADC-SAR, the output of the multiplexer DAC is buffered, and thus exhibits a low impendence. While the output of the S/H amplifier, via a coupling capacitor, shows a high impedance. In the operation of the SAR ADC, a rapid voltage variation appearing at the DAC output will couple to the other input node via the parasitic gate-source capacitance of the input transistors. Because of the high output impedance of the S/H amplifier, this voltage coupling between two input ports, termed as *input feedthrough*, will result in a voltage glitch at the output of the S/H amplifier.

The input feedthrough can change the charge stored on the capacitor permanently and results in a voltage deviation at the output of the S/H amplifier. One method to deal with this error is to shrink the gate area of the input transistor. However, this approach is often limited by the requirements on the $1/f$ noise and the matching of input transistors. The other method is to insert a source-follower before the input of the pre-amplifier, which leads to a reduction of the output impedance of the S/H amplifier. Consequently, the amplitude of the glitch introduced by the input feedthrough is greatly reduced. To maintain both input node has a same voltage drop from the buffer, two same source-followers ("Buf-1" in Fig. 4.19) are implemented in the front of the pre-amplifier.

Kickback noise: The kickback noise is an important factor to degrade the accuracy of the comparator. In Fig. 4.21, during the regeneration phase, the latch toggles the input signals. The
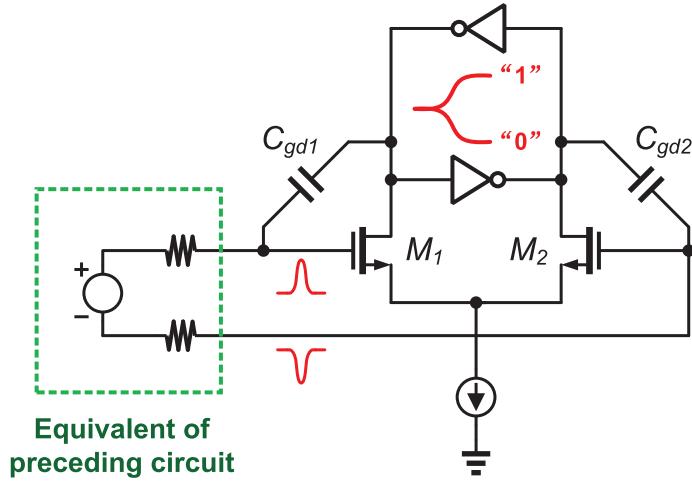
Figure 4.21: *Principle of the kickback noise.*

two cross-coupled inverters acting as a positive feedback to drive the output nodes toward ground or power rail. The acutely voltage variation at the output nodes are coupled via the gate-drain parasitic capacitors of the input transistors to the input nodes. In practice, the circuit preceding the latch does not exhibit a very low impedance, thus the inputs of the latch suffer a disturbance. This disturbance that can be seen as a noise appearing at the latch input, is usually termed as *kickback noise*.

The solutions to deal with the kickback noise are similar for the input feed-through, which are reducing the gate area of the input transistors and adding the buffers to reduce the output impedance. Following the same reason as the case of input feedthrough, a pair of source-follower ("Buf-2" in Fig. 4.19) are added before the latch to alleviate the kickback noise.

4.3.3.3 Circuit implementation

Sampling switches   The MOS switch formed by a single transistor has a limitation in the input voltage range. The complementary switches can cover a larger input range, but at the cost of an additional transistor. In the switched-capacitor circuit, the switches can be classified into two categories. One type is the clamping switches whose input voltage is fixed to a constant value. The single transistor switch is enough to cover the required dynamic range. The other type of switches exist in the signal path to handle a time-variant signal. Thus, switches with a large input dynamic range are required, and at the same time the on-resistance should be low enough to match the signal bandwidth.

In Fig. 4.19, the switches S_1 and S_2 are in the signal path. The input voltage set by the S/H amplifier has a baseline value of $\sim$1.2 V, and increases with incident particles. Considering the possible signal range, the PMOS switch with the aspect ratio of W/L=2.0 μm/0.18 μm can meet the requirements on both the dynamic range and the response time. The rest of switches

S_2–S_6 are realized by the NMOS transistors with the size of W/L=1.0 μm/0.18 μm.

Source-follower buffer In Fig. 4.19, both "Buf-1" and "Buf-2" act to reduce the output impedance. Hence, the same schematic is used as illustrated in Fig. 4.22. The source-follower has a simple architecture, as well as good power efficiency and low noise. Moreover, the output impedance is equal to the inverse of transconductance which can be tuned by the bias current. The drawback is that there exists a voltage drop between the input and output, and its value changes with the bias current and the input/output voltage.
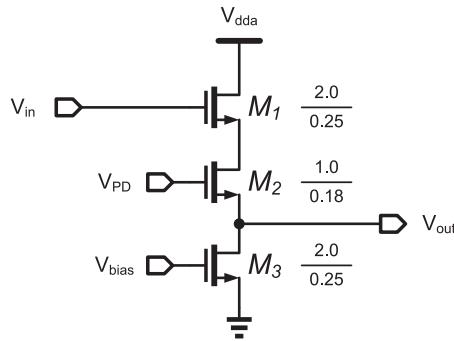
Figure 4.22: Schematics of the source-follower in the "Buf-1" and "Buf-2".

The simulated results of the source-follower are listed in Table 4.3.

Gain@DC	0.86 V/V
Input Noise (1 mHz – 1 GHz)	0.11 mV
Input range	0.56–1.80 V
Output range	0.07–1.13 V
Static current	5.0 μA

Table 4.3: Summary of the simulation results of the source-follower.

Single-stage amplifier As analyzed previously, the amplifier used in pre-amplifier requires a low gain ($\lesssim$ 5 V/V), a high bandwidth (> 35 MHz) together with a noise as low as possible. The single-stage fully differential amplifier is a proper choice. The NMOS input transistors can match the input dynamic range.

The schematics of the amplifier is depicted in Fig. 4.23. The gain can be calculated as follows

$$A_v = \frac{g_{m1}}{g_{m5} + g_{ds1} + g_{ds5}} ,$$ (4.30)

where g_m is the transconductance, and $1/g_{ds}$ is the small-signal output impedance. Generally,
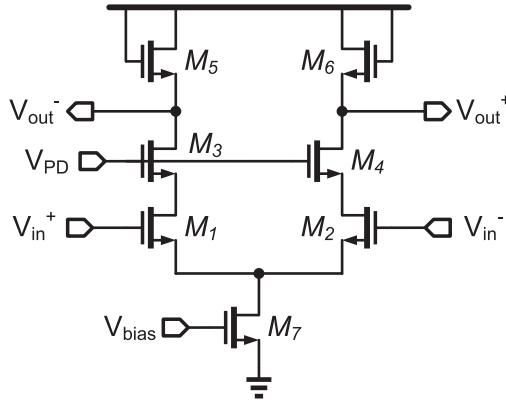
Figure 4.23: Schematics of the amplifier in the pre-amplifier.

$g_m \gg g_{ds}$, so Eq. (4.31) can be rewritten as

$$A_v = \frac{g_{m1}}{g_{m5}} = \sqrt{\frac{2\mu C_{ox} \cdot (\frac{W}{L})_1 I}{2\mu C_{ox} \cdot (\frac{W}{L})_5 I}} = \sqrt{\frac{(\frac{W}{L})_1}{(\frac{W}{L})_5}} \, , \tag{4.31}$$

in which the gain can be directly defined by the aspect ratio of the input and the load transistors.

Since the signal input to A_2 has been amplified by A_1, A_2 demands a larger input range. Operating in the open-loop mode, the CS amplifier has a low gain that is inversely proportion to the common-input range. Therefore, A_1 is designed with a high gain to achieve a high SNR, and at the same time the reduced input range is acceptable. In contrast to A_1, A_2 is designed with a smaller gain together with a larger input range.

The performances of both amplifiers are summarized in Table 4.4.

Items	A_1	A_2
Gain@DC	4.97 V/V	4.15 V/V
-3db Bandwidth	73.19 MHz	101.00 MHz
Input noise (1 mHz–1 GHz)	0.14 mV	0.27 mV
Input common-mode range	0.51–1.80 V	0.40–1.80 V
Output swing range	0.84–1.52 V	0.81–1.52 V
Input offset	6.11 mV	6.14 mV
Static current	6.35 µA	3.47 µA

Table 4.4: Summary of the simulation results of the amplifier.

4.3.3.4 Simulation results

The simulation results of the pre-amplifier are presented as follows.
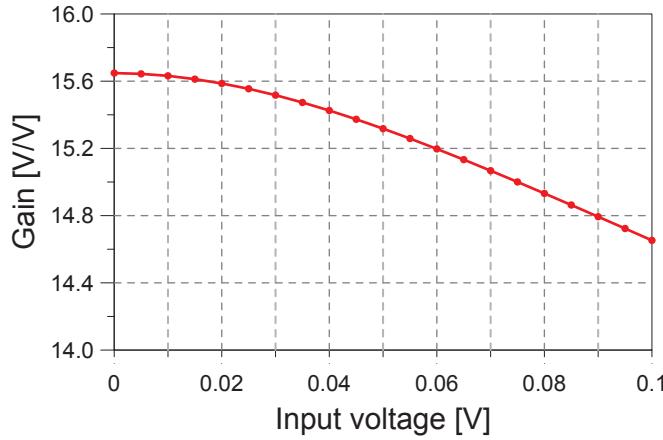
Figure 4.24: Simulated gain of the pre-amplifier with a input voltage swept from 0 to 100 mV.

Gain   Figure 4.24 is the simulated gain of the pre-amplifier. The open-looped CS-type amplifier is sensitive to the variation of the operational point, and its gain is generally a function of the input signal amplitude. The common-mode input voltage of the comparator is set by the reference "V_{clp}" in the S/H amplifier (see Fig. 4.11) and the reference "V_{ctrl}" in the DAC (see Fig. 4.30). The simulation result shows the pre-amplifier has a gain of ∼15.6 V/V for a small input. Additionally, for a large input voltage of 100 mV, the gain still remains above 14.6 V/V. The simulated gain of the pre-amplifier is less than the product of the gains provided by A_1 and A_2. This gain loss is due to the source-followers and the capacitance divider at the input of A_2. When the input voltage exceeds 100 mV, the gain will reduce further. However in this case, the amplitude of the input signal is large enough to trigger the latch with the correct code no matter how large the offset and noise are.

Noise   The pre-amplifier is a dynamic circuit driven by the control signal in a given sequence. The conventional AC noise simulation is not comprehensive to take into account the influence of CDS on the temporal noise. The transient noise simulation (TNS) can effectively analyze the noise in the dynamic circuits. Figure 4.25 shows the equivalent input noise of the pre-amplifier acquired via 1000 times TNS. By counting the voltage at a fixed time, the calculated rms noise of the pre-amplifier is ∼0.47 mV, which is much less than the least input signal.

Offset   Total 1000 times Monte-carlo simulations of the pre-amplifier are performed to calculate the input equivalent offset voltage as shown in Fig. 4.26. To reduce the offset, the offset suppression technique is employed in pre-amplifier. To compare the effect of the offset suppression technique, the results with and without this structure are plotted in the same figure. It is obviously the offset is greatly reduced from nearly 4 mV to less than 1 mV.
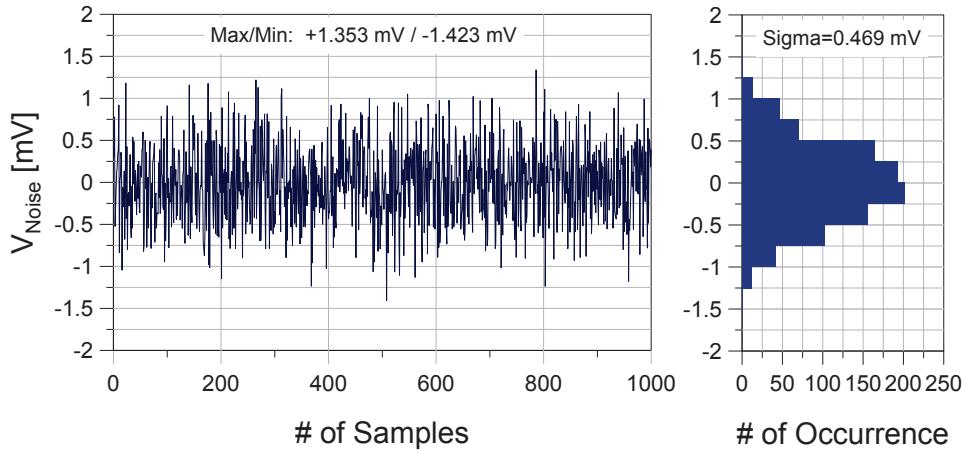
Figure 4.25: *Equivalent input noise of the preamplifier by 1000 times transient noise simulation.*
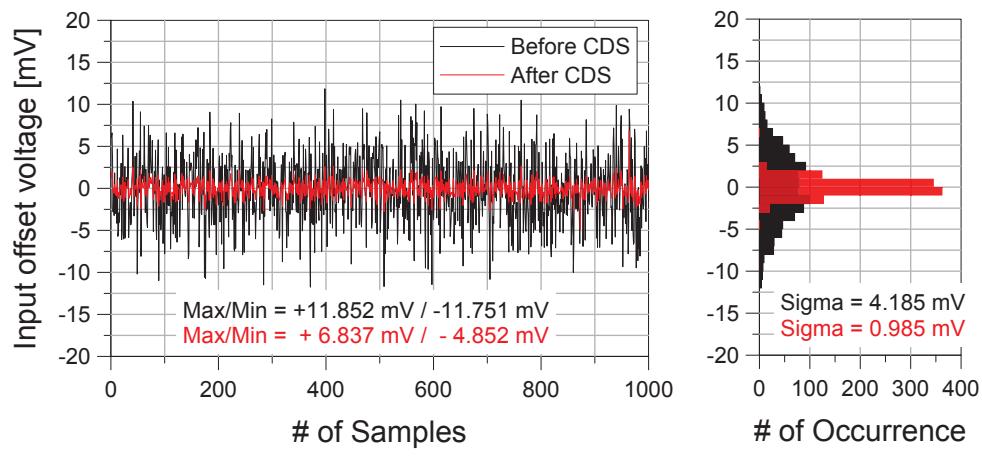
Figure 4.26: *Equivalent input offset of the preamplifier in case of w/o CDS by 1000 times Monte-carlo simulation.*
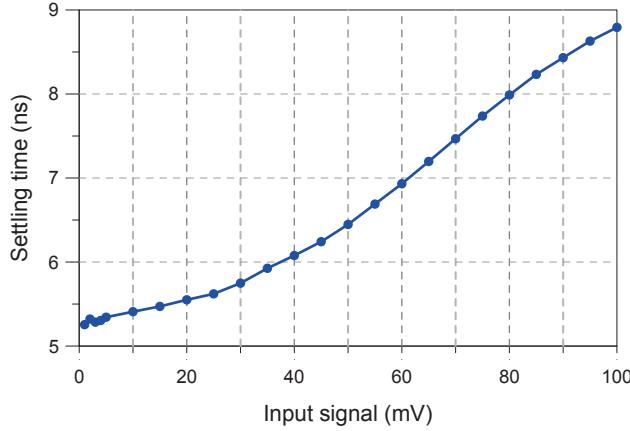
Figure 4.27: Settling time of the pre-amplifier versus input signal.

Settling time   Settling time is defined as the time elapsed from the change of the input to the output that stabilizes within a certain range of the final value. This place, we adopt the time of the output to settle within +/–10% of the final value. The settling time not only includes the propagation delay, but also contains the time for the output to recover from the overload condition associated with slewing, and finally settle to within the specified error [13]. The settling time is crucial because the conversion speed of ADC depends on the settling time of the pre-amplifier. Additionally, the settling time also depends on the input signal amplitude. Fig. 4.27 is the simulation for the settling time versus input. Even for the 100 mV large input, the settling time is less than 9 ns that is less than the half of the conversion period, i.e. 20 ns.

4.3.4 Latch

In the comparator, the latch operates synchronously with the clock to toggle the differential inputs and then export a binary output. In a high-speed system, the latch equipped with a positive feedback mechanism is generally used to regenerate the analog input into a full-scale digital code.

4.3.4.1 Architecture selection

Usually, the latch can be divided into three categories: static latch, class-AB latch and dynamic latch. A detailed description of these architectures can be found in [14]. They demonstrate a great difference in terms of power consumption, speed and kickback noise. A comparison among them are summarized in Table 4.5.

The problem of kickback noise has been resolved by inserting the buffers after the pre-amplifier to limit the output impedance. Therefore, the selection of architecture concentrates

	Static latch	Class-AB latch	Dynamic latch
Power consumption	high	medium	low
Speed	slow	medium	fast
Kickback noise	small	medium	large

Table 4.5: Comparison of the typical latch architectures in terms of power consumption, speed and kickback noise, respectively.

on the optimization of power consumption and speed. Considering these criterions, the dynamic latch is chosen in the design.

4.3.4.2 Circuit implementation
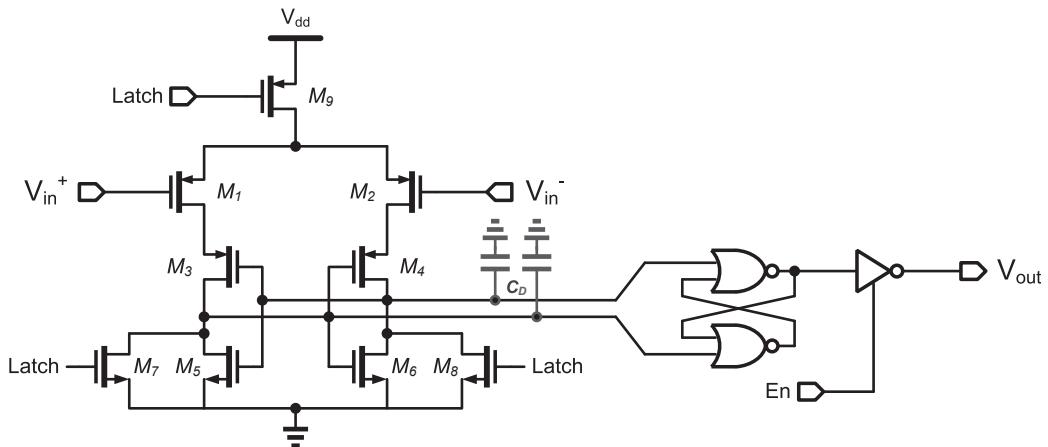
Figure 4.28: Schematic of the latch.

Figure 4.28 is the schematic of the latch that includes a dynamic latch, a R-S digital latch and a buffer with output enable. The dynamic latch is selected because of the superior features in speed and power consumption. The source-followers in the last stage of the pre-amplifier drops the common-mode voltage to $\sim$0.5 V. The PMOS transistor M_1 and M_2 as the input stage is capable to cover the low common-mode voltage. Two cross-coupled inverters formed by M_3/M_5 and M_4/M_6 realize the regeneration function. M_7, M_8 and M_0 are the switches to initialize the latch in the reset phase.

The operation of dynamic latch starts from the reset phase where the "latch" is high. M_9 cuts off the current biasing of the circuits, and meantime, the reset switch M_7 and M_8 pull down the output nodes to the ground. In consequence, M_1–M_6 are in the cutoff region. In the regeneration phase, the "latch" signal turns to low. The current flows again via M_9 into the differential input transistors. Due to the voltage difference at the inputs, there is a slight distinction in current flowing through M_1 and M_2. The positive feedback load composed of the cross-coupled inverters pushes both output nodes to the ground and power rail respectively. No static current passes though the latch, but only the dynamic power is dissipated at the

beginning of the regeneration phase.

The offset of the latch can be estimated by only considering the input transistor M_1/M_2, and the charge injections by the switches M_7/M_8. By calculating the derivative of the currents in the saturate region, the input offset of the latch is obtained as

$$\Delta V_{GS} = \frac{1}{2}(V_{GS} - V_{TH})\left(\frac{\Delta L}{L} - \frac{\Delta W}{W}\right) + \Delta V_{TH} + \frac{\Delta Q}{C_D} \,, \tag{4.32}$$

where $\Delta L/L$ and $\Delta W/W$ is the relative dimension mismatches in M_1/M_2, ΔV_{TH} is the standard deviation of the threshold voltage, ΔQ is the mismatch of the charge injection from M_7 and M_8, and C_D is the load capacitor. Increasing the gate size as well as reducing the overdrive voltage of the input transistors can reduce the input offset. But the enlarging of gate size costs the additional silicon area. According to the Eq. (4.32), the offset can be calculated with a typical value in the order of several 10 mV, in which the transistor size mismatch that is represented by the second item in Eq. (4.32) is the dominating contributor.

The output impedance of the regeneration latch is defined by the parallel cross-coupled transistor M_3/M_4 and M_5/M_6 that each one exhibits a negative output impedance of $-1/(2g_m)$ respectively. By this result, the regeneration time constant of the latch can be obtained as follows

$$\tau_R = \frac{C_D}{g_m} \,, \tag{4.33}$$

where g_m is the transconductance of input transistors. The transconductance of the input is reverse proportional to the regeneration speed. Reducing the overdrive voltage of input transistor limits the offset, but at the cost of the slowing down the speed of the latch.

Moreover, the offset also depends on the load capacitor mismatch [15]. The offset due to load mismatch is equal to

$$V_{off} = \frac{1}{2}\frac{\Delta C_D}{C_D}(V_{out,0} - V_S) \,, \tag{4.34}$$

where the $\Delta C_D/C_D$ is the relative mismatch of the load capacitor. $V_{out,0}$ is the initial output voltage at the beginning of the regeneration phase. V_S is the input voltage for the cross-coupled inverter that the PMOS current is equal to the NMOS.

The output of the dynamic latch is initialized to the ground periodically during the reset phase. In order to record the binary result generated in the regeneration phase, a R-S digital latch is added following the dynamic latch to store the result generated until the arriving of the next regeneration.

4.3.4.3 Simulation results

Latch is a non-linear circuit that only has a binary output with "one" or "zero". Typically, the distribution of offset is Gaussian. The offset can be calculated by scanning the input and performing the Monte-carlo simulations. The probability of event "one" can be achieved. Fit-
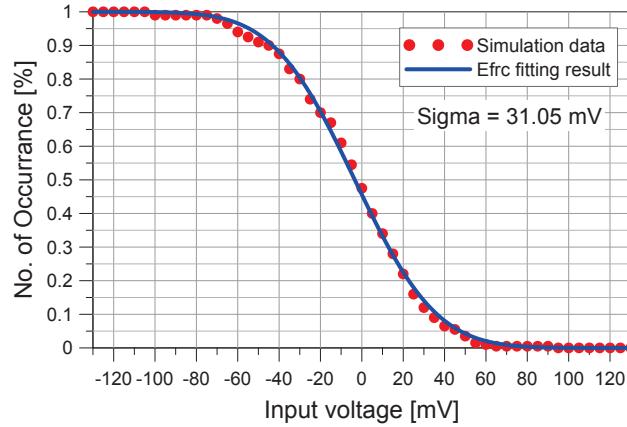
Figure 4.29: *Simulation result of the normalized response of the latch. The statistical result is fit by the complementary error function (erfc). The standard deviation is rms input offset.*

ting these data with the complementary error function (erfc), the rms value of input offset can be computed. Figure 4.29 shows the simulation result of the latch input offset. The rms value is ∼31 mV. Taking into account the gain of pre-amplifier, the input offset voltage of comparator contributed by the latch is only ∼2 mV. This result proves the necessity of the pre-amplifier used to compensate the latch offset.

4.3.5 Multiplexer DAC

In a typical SAR ADC, the DAC is composed of a binary-weighted capacitor array, and its output voltage is generated following the charge-redistribution principle. But for the CPS with pixel-level ADCs, a large chip area occupied by the capacitor array is forbidden. Because there are a large number of ADCs operating synchronously under a same system clock, some circuits in the DAC can be shared by all ADCs to reach a simple pixel circuit.

In our design the ADC resolution is limited to 3-bit, thus total 7 references are required by the SAR ADCs. As a result, we proposed a DAC based on the multiplexer structure to realize the maximum circuit-sharing among all pixels.

The schematic of the proposed DAC is shown in Fig. 4.30. An analog multiplexer consists of only MOS switches is integrated in each pixel to select one reference from 7 different voltages. In the MIMADC-SAR, these references are generated on the test board. Since the minimum reference voltage approximates 1.2 V, the switches are implemented by the PMOS transistors to match the input voltage range.

The control signals V_{ctrl}<0:6> are generated by the SAR logic posited at the end of column. The pixels belonging to the same column share the same control signals. The signal
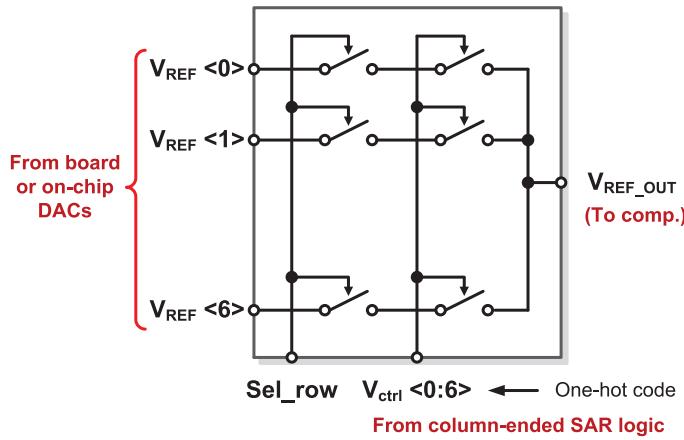
Figure 4.30: *Schematics of the multiplexer DAC.*

"Sel_row" disables the DAC during the integration time by disconnecting the references from the DAC inputs. The proposed structure of in-pixel DAC ensures that only the digital signals are transferred along the column buses.

All the PMOS within the DAC has an aspect ratio of W/L=1.25 µm/ 0.18 µm. The switch-on resistance should be small enough to reduce the time constant of the output response. The simulation shows when the switch is opened by the control signal, the output can reach a stable value within ∼6 ns, which is sufficient for a conversion period of 20 ns.

It should noted that the proposed DAC architecture only suits the low resolution ADC. With the increase of resolution, the number of the required control signals also increase at an exponential rate, which causes a great difficulty during the layout. For the high-resolution application, an encoding circuit is possible to be integrated in the pixel to reduce the number of the control signals.

4.3.6 SAR control logic

SAR control logic is a finite state machine to control the DAC operation based on the comparator output. Only three inputs are required for this blocks. The clock signal "clk" synchronizes the logic circuits at positive edge of the clock, and the "reset" signal initializes the circuits asynchronously at the beginning of operation. The "in" signal is the comparator output generated from the pixels. The outputs of SAR logic includes two parts: one is the signals to control the DAC; the other one is the 3-bit ADC results. The controls signals feed back to the DAC is in format of the one-hot code.

The SAR logic circuit only consists of the digital standard cells. In the 0.18 µm process, the provided digital cells are still too large for the in-pixel integration. For example, a simplest D-type flip-flop with only positive output presents a height of 5.6 µm with a 10.65 µm width. Benefitting from the rolling shutter readout, only one ADC in a column is operating at a given

moment. Therefore, we place the SAR logic on the column-end, sharing by all the pixel in a column. This architecture ensures the sufficient pixel area reserved for the ADC circuits, and only the pixel output is still digital, which is the essential difference compared with the conventional ADC architecture. The main drawback of this structure, as same as the multiplexer DAC, is that the allowed ADC resolution is limited. One possible resolution is to encode the output. In addition, the advanced process may allow to contain this logic circuit in the pixel if the standard cell is small enough.
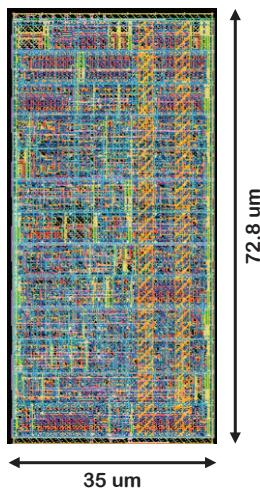

Figure 4.31: *Layout of the column-ended SAR logic. The width is 35 µm to match the pixel pitch.*

Figure 4.31 is the layout of the SAR logic. The size is 35.0 µm (width)×72.8 µm (height) for matching the pixel pitch. Except the metal for the power routing, three metal layers are used in the layout, where the metal M_2 is routed in horizontal direction and M_3 in vertical direction.

4.4 Layout implementation

The proposed CPS, i.e. MIMADC-SAR, was implemented by the TowerJazz 0.18 µm CIS process. Total 6-layer aluminum metals, named M_1–M_5 and top layer TOP_M, can be used for routing. Among them, the TOP_M is thicker (∼0.94 µm) than the rest of the metals (∼0.54 µm), so TOP_M is suitable for routing the power and ground signals. Two-layer polys are provides that one for MOSFET gate, and the other one for poly resistor. Regrettably, no Poly-Insulator-Poly (PIP) capacitor is offered in this process. As a substitution, three Metal-Insulator-Metal (MIM) capacitors can be used, which are the standard, the high-density and the stacked MIM capacitors. The most attractive type is the stacked one that is comprised of two parallel-connected high density MIM capacitors in M_4/M_5 and M_5/TOP_M respectively. The capacitance density of stacked type is ∼3.4 fF/µm^2, double of the high density capacitor. However, neither metal lines nor devices is permitted to be placed under the MIM

capacitor. With respect to the layout of the pixel-level ADCs, the existence of MIM capacitor in pixel blocks the routing pathes in both horizontal and vertical directions. Therefore, a careful routing plan is necessary.
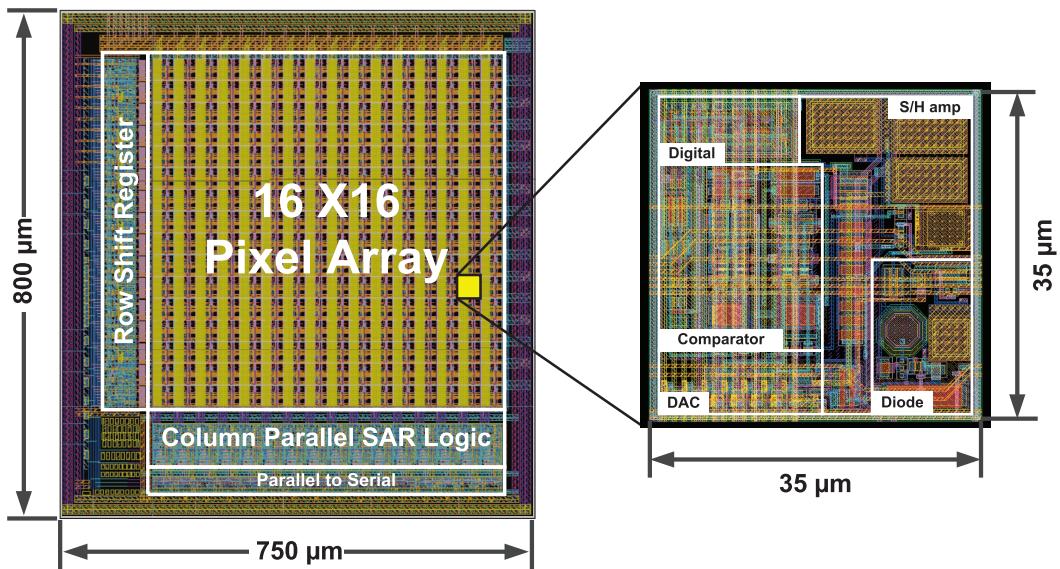
Figure 4.32: *Layout of the MIMADC-SAR pixel matrix combining with a zoomed view of the pixel.*

The layout of the MIMADC-SAR is presented in Fig. 4.32. The sensor includes a 16×16 pixels with a square pixel size of 35 µm$\times$35 µm. At the end of the pixel matrix, a group of 16 column-ended SAR logics are placed. The 3-bit digital results generated by the SAR logic will be read out by the parallel-to-series converters. Every 4 SAR logics share a serialization converter to rearrange total 12-bit data to a 1-bit stream. The data from the MIMADC-SAR is transmitted by the LVDS drivers to the external data acquisition system. At the left side of the matrix is a row shift register circuit to perform the rolling shutter readout.

A zoomed view of the pixel layout is also shown in Fig. 4.32, which consists of a sensing element, a S/H amplifier, a comparator and a multiplexer DAC. The additional deep p-wells are placed under the n-wells of PMOS to prevent a competition with diode in charge collection.

The reasonable signal and power routing plans are very important in reducing the FPN, especially in a large-scale matrix. A detail discussion will be provided in the next sections with respects to the layout of the MIMADC-SAR sensor.

4.4.1 Signal routing plan

In the design of pixel-level ADCs, one of major challenge is to optimize the layout to minimize the parasitic parameters and then the crosstalk to ensure that the ADCs are operated in a desired speed.

In order to reach an optimum layout within a complicated pixel circuit, a thoughtful rout-

ing plan before the implementation is necessary. Within the available 6 metal layers, the bottom layers M_1 and M_2 are reserved for the routing in the circuit blocks. Metals M_3 and TOP_M are routed in vertical direction, and M_4 in horizontal direction. This crossed routing not only increases the success of routing, but also reduces the parasitics capacitance between the metal lines on the different layers. Since the digital control signals and the sensitive voltage references are routed on M_4 and TOP_M respectively, the intermediate layer M_5 is preserved deliberately to form a ground plane for isolating M_4 and TOP_M.
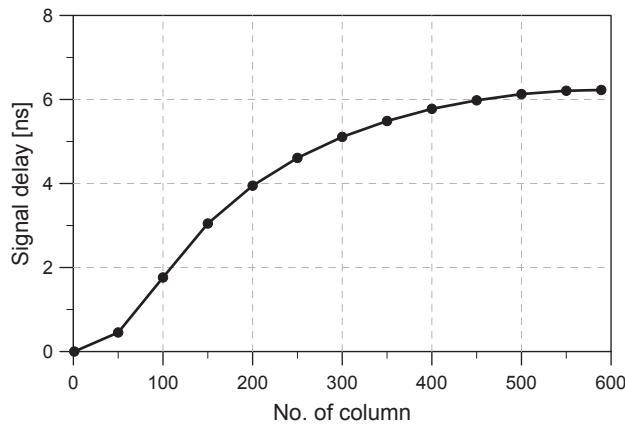
Figure 4.33: *Delay of a signal wire within a full scale sensor of 590 column.*

In the pixel sensor, the control signals are shared by a row of pixels. The parasitic resistance and capacitance of the wires introduce a delay that results in a different arriving time of signals for the various pixels. This delay possibly results in a deviation in the pixel response, translating into the FPN. The value of the delay can be calculated based on the parameters of the pixel layout. Assuming the metal wire with a unit length of pixel pitch can be simplified to a lumped model which includes a resistor R_0 and a capacitor C_0. In the MIMADC-SAR, the width of the control signals realized on M_4 is 0.35 μm. The resistance of a 0.35 μm width, 35 μm length metal wire on M_4 can be calculated to be ∼8 Ω, and the capacitance is ∼ 6 fF acquired by the parasitic extraction. The signal wire routed on a row of pixels can be modeled as a network that connects the above lumped model in series. By injecting a voltage pulse at the edge of this network, the transmission delay at each pixel can be measured. The simulation result of the signal delay in a full-scale sensor is shown in Fig. 4.33. the delay is larger than 6 ns between the pixels at the first and the last column. Since this simulation is based on the simplified lumped model, this transmission delay will be worse in the practical pixel matrix. The possible approaches to resolve this problem are:

- reducing the parasitic components in the layout by a cautious design;
- relaxing the requirements on the timing of the control signal to increase the robustness of the circuits;
- using large buffer to drive the control signal;
- implementing the distributed buffers within pixels to drive the signal, just like the clock

tree to drive the high-speed clock signal.

4.4.2 Power routing plan

The power plan, as an important step in the physical design of pixel sensor, aims to provide an uniform power distribution for the whole chip. In the circuit analysis, generally we assume that the power and ground signal lines are ideal, and hence the uniform voltages on them. In practice, all the metal lines exhibits a finite impedance which can be modeled with a RC equivalent circuit. The power/ground signals distributed in a chip can be seen as a network called power grid to connect the I/O pins at some points. The current drawing from the power pins flows through the power grid, and leads to a voltage fluctuation. The voltage drop on power rail is referred as *IR drop*, and the rise on ground is termed as *ground bounce*. Both of them are more serious in the advanced process due to the reduction of power supply and increase of current density. The analysis of power grid can be classified into two methods: static and dynamic [16]. For a simplification in calculation, only the static analysis is considered in this section.
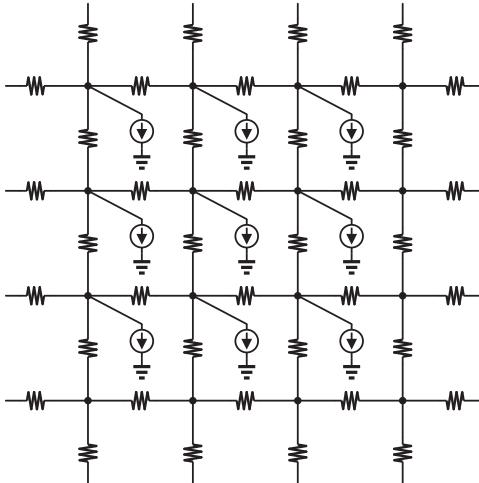
Figure 4.34: *DC equivalent model of the power grid for the static analysis.*

The equivalent model of the power grid is illustrated in Fig. 4.34, where the only the parasitic resistance are included in. The metal lines and vias are modeled as a resistance, whose value can be calculated from the resistance density of a given metal layer or extracted from the actual layout. In MIMADC-SAR, a very wide metal ring surrounding the pixel matrix. It is reasonable to assume that the edge of the matrix is powered by a constant voltage source. In the pixel sensor, each pixel cell draws the current from the power grid, which is modeled by an independent current source at each node of the power grid. As a result, the analysis of the power grid is summed up to a calculation of a linear resistance network.

In MIMADC-SAR, the independent power/ground network is designed for the analog

and digital parts in pixel respectively. Digital power "VDD" and the corresponding ground "VSS" are used only for the multiplexer DAC and the dynamic latch. The analog counterparts "vdda" and "gnd" power the sensing element, S/H amplifier and pre-amplifier.

We only consider the IR drop on the analog power "vdda". In TowerJazz 0.18 μm process, the resistance density of the metal is 80 mΩ/□ for M_1–M_5. The power "vdda" is implemented on metal layer M_2 with a width ~1.4 μm, which translates into a resistor of ~2 Ω on each edge of pixel with a length of 35 μm. The current drawing from "vdda" in pixel is set to 100 μA according to the circuit simulation. Based on the above calculated values, the IR drop of the power network can be simulated with an ideal model as shown in Fig. 4.34, where the resistors are 2 Ω and the ideal current sources are 100 μA.
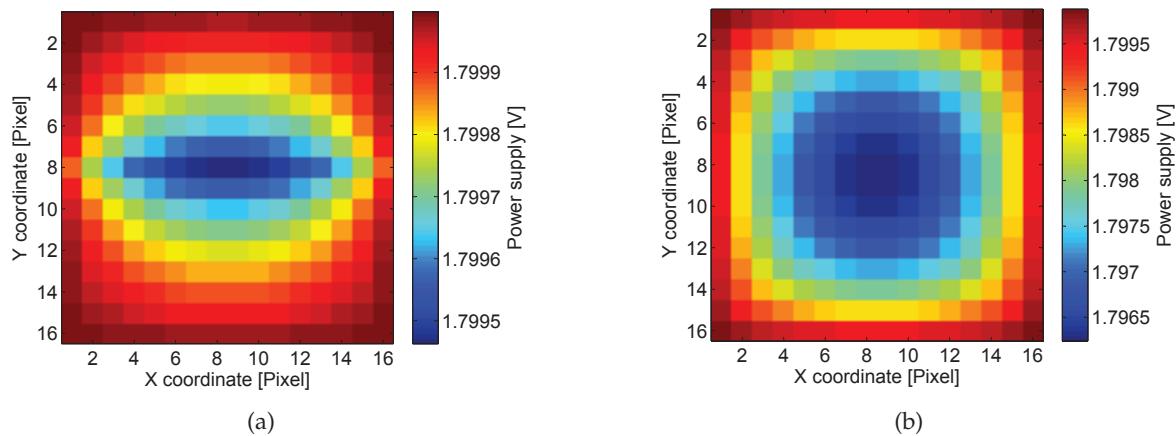
Figure 4.35: *Simulation result of IR drop in a 16×16 pixel matrix operated in (a) rolling shutter with row 8 being powered on, and (b) global shutter. The color bar is in the unit of Volt.*

Figure 4.35(a) is the distribution of the simulated IR drop in a 16×16 pixel matrix to imitate the case in MIMADC-SAR. Only one row of pixels is powered on, as with the operation of rolling shutter. The simulation result shows that in this small matrix, the IR drop can be ignored. As stated in Section 4.2.1, compared with the rolling shutter, the global shutter readout demonstrates a different performance on IR drop. As a comparison, a same simulation is performed on this model but all the pixels are powered on. The result in Fig. 4.35(a) indicates that because the great number of pixels operate simultaneously, a larger IR drop exists in the center of the matrix, but its value is acceptable.

The similar simulations are also applied to a full-scale matrix which matches the sensor on the outer layers of ILD-VTX. The required active area is ~2 cm×2 cm translated to a matrix size of 590 columns by 590 rows pixel cells. Figure 4.36(a) is the IR drop distribution for a full-scale sensor operated in rolling shutter mode. Benefiting from that only single-row is powered on, the IR drop still remains small even in the large matrix. As shown in Figure 4.36(a), operating in global shutter, most of the pixels in matrix suffer a large IR drop. Because of using the ideal model in the simulation, the power supply in the center of the matrix is reduced to the negative value. In a practical sensor, the power supply will drop to the
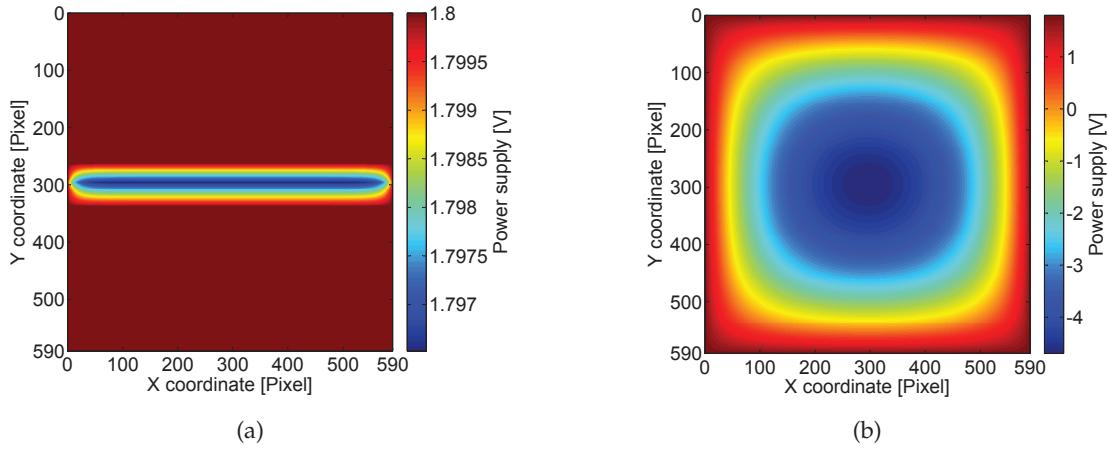
Figure 4.36: *Simulation result of the IR drop in a fully-scaled 590×590 pixel matrix operated in (a) rolling shutter and (b) global shutter. The color bar is in the unit of Volt.*

ground for the pixels with the negative simulation results shown in Fig.4.36(b). Consequently, if the power consumption of the pixel circuits is not reduced, the global shutter cannot be used to read out a large matrix. In conclusion, the rolling shutter readout can relax the design of power grid in the large-scale pixel sensor.

4.5 Conclusion

This chapter presents a CPS integrated pixel-level SAR ADCs dedicated to the ILD-VTX outer layers. Each pixel consists of a sensing element, a S/H amplifier, and a SAR ADC. The resolution of the ADC is 3-bit considering the trade-off between the spatial resolution and conversion speed. The LSB is equal to the floor noise of the sensing diode $\sim$20 e$^-$ that translated to $\sim$1 mV output voltage form the sensing element. For a purpose of maximum detection efficiency and least material budget, the constraints of low-noise and low-power are applied throughout in the circuit design. The major challenge in terms of pixel-level ADCs is how to implement the whole signal chain within a limited pixel area. Some special considerations are employed in the architecture selection, circuit design and the layout.

The MIMADC-SAR is a prototype to validate the concept to integrate SAR ADC within each pixel. The scale of the sensor is 16×16 square pixels with a pitch of 35 µm. The SAR ADC has a prominent merit in the conversion speed than the generally used slope-type ADC but at the cost of the large area in the DAC and SAR logic. An architecture including a multiplexer DAC and column-ended SAR logic is adopted to handle these problems. Driving by a clock frequency of 100 MHz, a conversion period of 160 ns is reached.

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5

Design of a CPS with pixel-level single-slope ADCs

In the previous chapter, we presented a pixel matrix integrated with pixel-level SAR ADCs. As an alternative, single-slope (SS) ADCs are also attractive for the in-pixel implementation. Compared with SAR ADCs, the SS architectures demonstrate a simpler topology. The SAR control logics and DACs in SAR ADCs are replaced by a ramp generation circuit, thereby reducing the occupied area and crosstalk, both of which are crucial for pixel-level ADCs. However, the exponential growth of conversion time as a function of resolution limits the use of SS ADCs in high-speed applications. Benefiting from a low resolution (3-bit) required in our design, the SS ADCs can achieve an acceptable conversion time.

In this chapter, we propose two pixel matrices integrated with pixel-level ADCs based on the SS architectures. The main difference between them is the arrangement of the memories used to save digitalized results: in the first matrix the memories are placed in column, in the same way as the SAR logics in the MIMADC-SAR; while in the other matrix, the memories are included in each pixel. Additionally, the different topologies also exist in the design of the S/H amplifiers. In this thesis, for convenience, the matrix with the column-ended memories is referred to as "MIMADC-SS1", and the other one is referred to as "MIMADC-SS2".

The application background of these two matrices is the same as of the MIMADC-SAR, i.e. the outer layers of the ILD-VTX. Therefore, the specifications are shared by all the three matrices: 35×35 μm^2 pixel size and 3 bits ADC resolution. The conversion time of SS ADCs is elongated to 180 ns for the compatibility of the testing system, and can be easily reduced to 160 ns in the future design. The rolling shutter readout is employed because of the low power consumption.

The detailed design of both matrices with pixel-level SS ADCs will be discussed in this chapter. Since some building blocks are identical to those in the MIMADC-SAR, the following discussion concerns only the different circuits.

5.1 Pixel-level SS ADC with column-ended memory

5.1.1 Architecture
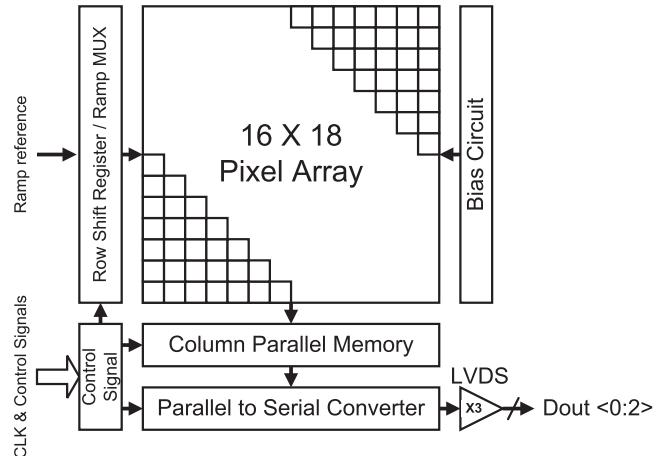
Figure 5.1: *Architecture of MIMADC-SS1 pixel matrix.*

The architecture of MIMADC-SS1 is shown in Fig. 5.1, where the topology is similar to that of MIMADC-SAR. The matrix scale is extended to 16 rows by 18 columns, and the column-ended SAR logics are replaced by the 3-bit digital memories. The ramp reference generated by the on-chip ramp generator is selected by the multiplexer and then transmitted to the activated row. A 3-bit digital counter offers the timing stamps shared by all the column-level memories. The ADC results are processed by a parallel-to-series converter and propagated out of chip by the LVDS drivers at a rate of 100 Mbps.

5.1.2 Circuit implementation

The block diagram of MIMADC-SS1 is depicted in Fig. 5.2. The pixel circuit is composed of a sensing element, an S/H amplifier, and a comparator, all of them are the same as those in the pixel of MIMADC-SAR. The detailed design of them can refer to the previous chapter, and therefore is not repeated again. The following discussion concentrates on the peripheral parts including ramp generator, buffer, and column-ended memory.

The principle of the SS ADCs can be derived by the timing sequence plotted in Fig. 5.3. Compared with the timing in MIMADC-SAR, the difference is only the procedure of the A/D conversion. The rise of the ramp reference triggers the counter to generate the timing stamps. As soon as input signal is equal to this ramp, the column-ended memories record the timing information at that instant as the ADC outputs.
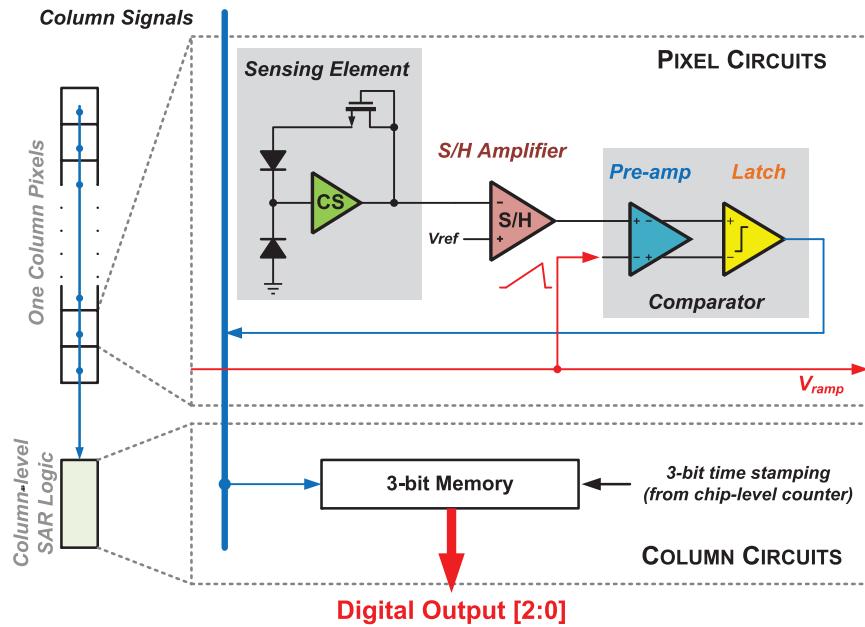
**Figure 5.2:** *Block diagram of MIMADC-SS1 circuits.*
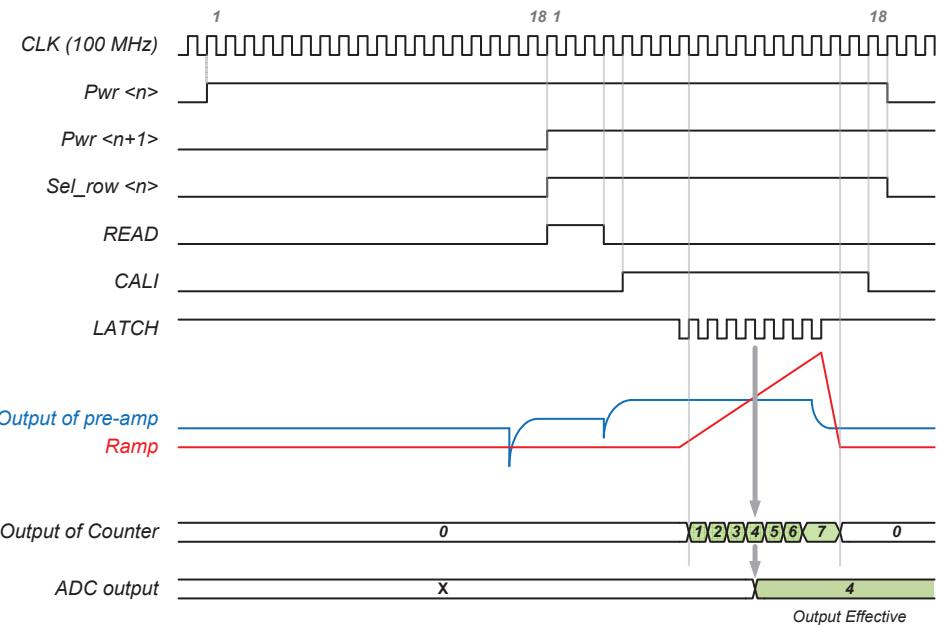
**Figure 5.3:** *Timing of the pixel in MIMADC-SS1.*

5.1.2.1 Adaptive ramp generator

In slope ADCs, the ramp reference acts as a ruler to measure the amplitude of the input signal. Any error existing in this reference is directly translated into an error of the ADCs. As a crucial building block, the ramp generator should conform to the following requirements:

- a high linearity of the ramp reference so as to reduce the DNL and INL errors in ADCS;

- a fast response speed to reach a desired rising time;

- a minimum noise with the ramp reference, which substantially degrades the SNR of pixel outputs;

- little sensitivity to process variation;

- good driving capability, excellent power supply rejection, etc.

Since the output of the ramp generator is shared by all pixels, the chip-level implementation allows a relaxation on power consumption and chip area.

The ramp generator can be realized by both analog and digital schemes. The principle of the analog scheme relies on a current integrator, while the digital one typically employs a DAC driven by a counter. Compared with the analog ramp generator, the DAC-based circuit not only features a large chip area and slow response speed, but also asks for some calibrations to ensure monolithic and output range. As a consequence, the analog generator scheme is chosen in our design.
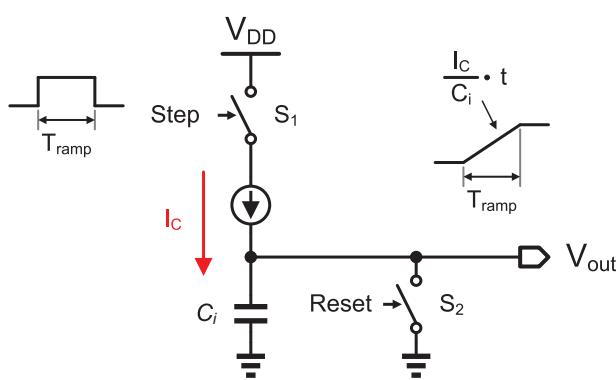
Figure 5.4:
Principle of a typical ramp generator. The capacitor C_i is charged by a constant current I_c. The voltage that integrated across C_i is in a form of ramp. The switch S_1 controls the current path to set the duration time of the ramp. Meanwhile, by closing the switch S_2, the ramp signal can be reset to the initial value.

A typical ramp generator operating in the analog domain is shown in Figure 5.4, where the current I_C integrating on the capacitor C_i results in a linear rising of ramp output. However, the linearity of output is generally degraded by the limited output impedance of the current source. Moreover, the parameters of the ramp reference, such as slope, max/min peak value, cannot be regulated easily.

To resolve the aforementioned drawbacks, an adaptive, high-accuracy ramp generator is employed. The word "adaptive" means the range of the generated ramp signal can converge to the pre-defined value automatically even with a large process variation. The block diagram of this architecture is illustrated in Fig. 5.5 [1], where the circuit consists of three parts described
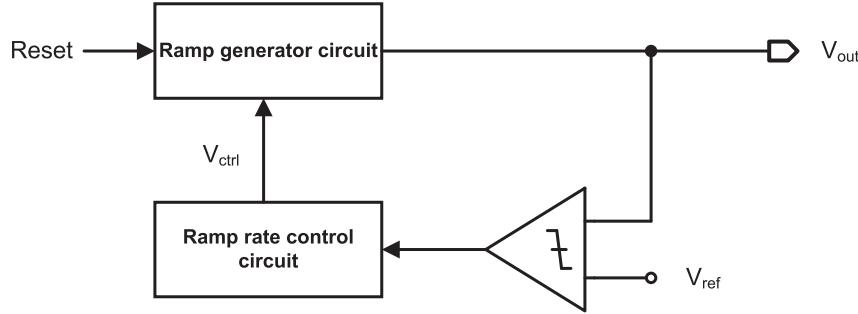
Figure 5.5: *Block diagram of the adaptive ramp generator.*

as follows:

- ramp generator core circuit composed of a voltage-controlled current source (VCCS) and an active integrator, generates the ramp signal;

- error amplifier compares this ramp signal with a pre-defined voltage. The error between both signals is extended to the power rails based on the polarity of the error value;

- ramp rate control circuit samples and shapes the output of the error amplifier, and then feed a correction voltage back to the VCCS within the ramp generator core.

The feedback loop comprised of the error amplifier and ramp rate control circuit adjusts the current source in the ramp generator core circuit continuously. Consequently, the ramp output will converge to a pre-determined shape within several correction periods.

Figure 5.6 is the schematic of the adaptive ramp generator. The integration capacitor, C_i, given in Fig. 5.4 is replaced with an active architecture, which is composed of an op-amp (A_0) and a capacitor (C_F). Transistors M_1–M_5 comprise the VCCS. The high-gain of A_0 and the cascode current mirror constituted of M_1–M_4 result in an approximately constant current output from the VCCS.

The output of the proposed ramp generator can be expressed as

$$V_{ramp}(t) = \frac{A_{v0}}{A_{v0}+1}\left(V_{low} + \frac{1}{C_F}\int_0^T I_c(t)\,\mathrm{d}t\right), \tag{5.1}$$

where A_{v0} is the open-loop gain of the op-amp A_0, T is the duration time of the ramp signal controlled by the "Reset" signal, and I_c is the current drawn by the cascode current mirror. When the adaptive scheme is operating, I_c varies with the time to approach the pre-determined value. As soon as the ramp output converges to the final value, the current I_c is almost constant, and hence the ramp signal is only a function of time to exhibit a linear rising.

The adaptive correction scheme including the error amplifier and ramp rate control circuits adjusts the peak value of the ramp signal to a given voltage, and then achieves a desired ramp slope. The errors of the ramp signal due to the process variation can be compensated by the
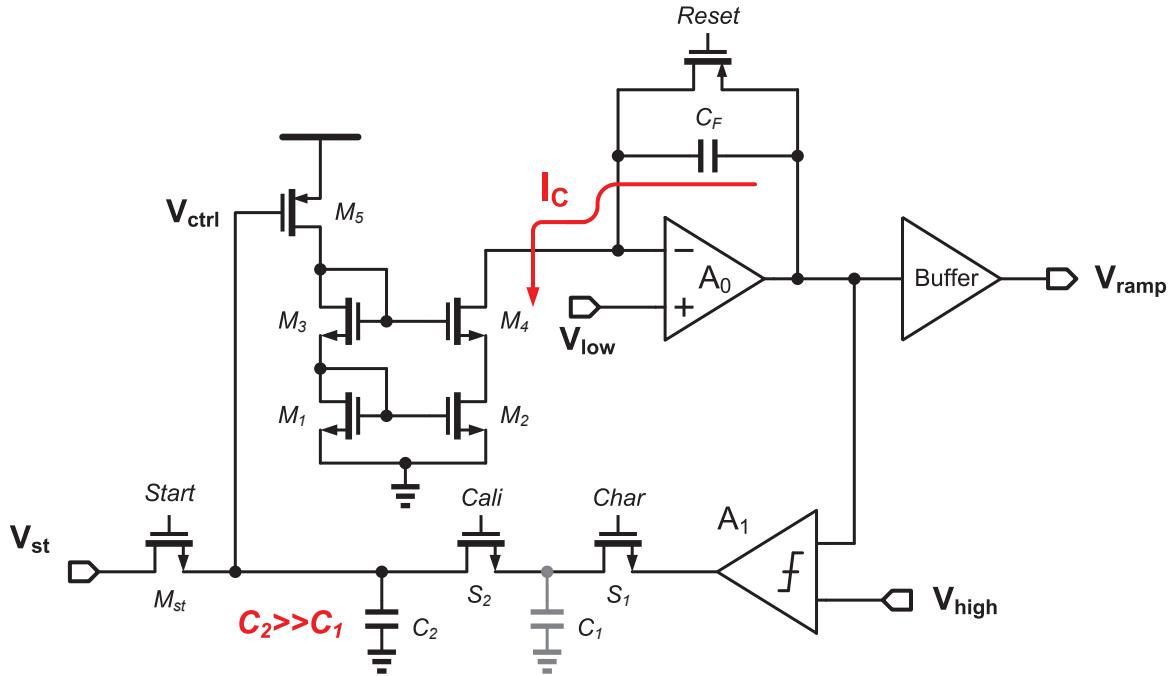
Figure 5.6: *Schematic of the adaptive ramp generator.*

feedback architecture. In consequence, a high-precision ramp output can be acquired. The principle of this adaptive correction is explained as follows.

The operation of the adaptive correction is controlled by 2-phase control signals "char" and "cali" shown in Fig. 5.7. In the "char" phase, the switch S_1 is on, and S_2 is off. The error amplifier A_1 compares the ramp output V_{ramp} with the voltage reference V_{high}. The difference of them is amplified and then charges the capacitor C_1. In the following "char" phase, S_1 is off, and S_2 is on. The output of A_1 is disconnected from C_1. The charge deposited on C_1 is equally redistributed to C_2. If V_{ramp} is lower than V_{high}, the charge redistribution leads to a reduction of the control signal V_{ctrl}, and then increases the output current. The maximum value of V_{ramp} will be reduced in the next operation period. This feedback mechanism adjusts the current drawn by the VCCS until the maximum value of V_{ramp} is equal to the pre-defined voltage V_{high}.

The input voltage of the VCCS, i.e. V_{ctrl}, can be obtained as follows

$$V_{ctrl}(i) = \frac{C_2}{C_1 + C_2} \cdot V_{ctrl}(i-1) + \frac{C_1}{C_1 + C_2}(V_{ramp} - V_{high}) \cdot A_{v1} , \tag{5.2}$$

where $V_{ctrl}(i)$ and $V_{ctrl}(i-1)$ are the control voltages during the current and the previous periods, respectively. A_{v1} donates the gain of the error amplifier A_1.

To achieve a high speed, A_1 is realized by a dynamic latch triggered by the signal "Char", thereby leading to an output with either positive or negative supply rail V_{dd}. Equation (5.2) can be rewritten as

$$V_{ctrl}(i) = V_{ctrl}(i-1) \pm \frac{C_1}{C_2} \cdot V_{dd} \, , \tag{5.3}$$

where the second item represents the correction voltage. If the $V_{ramp} > V_{high}$, the sign is negative, and if not, the sign is positive.

The voltage V_{ctrl} is connected to the gate of the M_5 to regulate the current I_c. The increment of V_{ctrl} results in a variation of the I_c at each iteration given by

$$\Delta I_c = g_{m5} \cdot \frac{C_1}{C_2} \cdot V_{dd} \, , \tag{5.4}$$

where ΔI_c is the variation value of I_c, and g_{m5} is the transconductance of the transistor M_5.

As soon as the correction procedure is finished, I_c will oscillate around a certain voltage in the following iterations. The step of this oscillation is still equal to ΔI_c that determines the precision of ramp. For a high precision of the ramp signal, a small ΔI_c is desired by reducing C_1/C_2.

To arrive at a low capacitance ratio and a minimum chip area, C_1 is implemented by two NMOS capacitors (W/L=34 µm/8 µm) connected in parallel. The equivalent capacitance value is ∼3.8 pF. C_2 utilizes the parasitic capacitance of the nearby switches S_1 and S_2 and the routing metal line to achieve a value less than 10 fF. When the ramp generator begins to power up, the cascode current mirror remains off, driving the active integrator out of operational region. So a power-up circuit is needed to provide an initial bias to activate the current mirror. Transistor M_{st} controlled by the "Start" signal compose this power-up circuit.
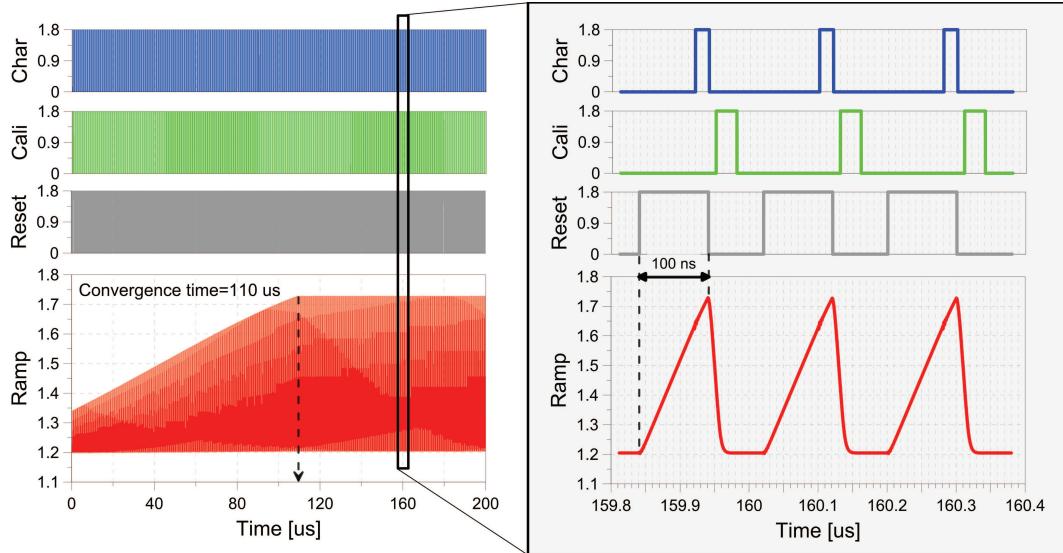
Figure 5.7: *Transient simulation results of adaptive ramp generator.*

The simulation of transient ramp output is illustrated in Fig. 5.7. The correction mechanism allows the ramp generator converging to the final value within less than 100 µs. The INL
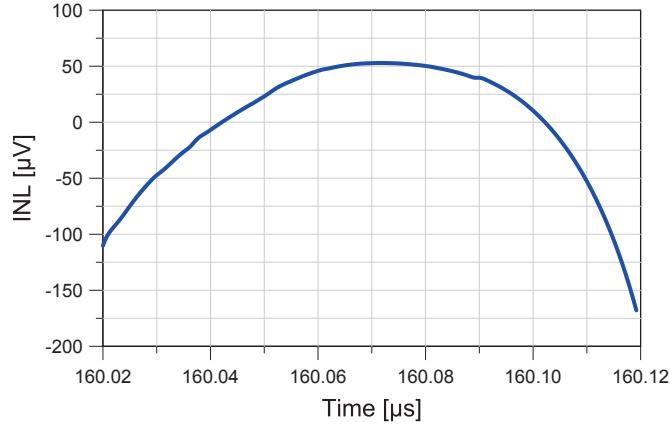
Figure 5.8: *Transient simulation results of INL for the adaptive ramp generator.*

of ramp signal is shown in Fig. 5.8. The linearity is more than 11-bit to meet the desired performance. The simulation results are summarized in Table 5.1.

Parameter	Value
INL [bit]	11.5
Ramp top voltage [V]	0.9–1.5
Ramp bottom voltage [V]	0.5–1.0
Slope variation [%]	2.35
Average power * [μW]	100

* Not include the power consumption of the buffer.

Table 5.1: *Summary of the simulation results of the adaptive ramp generator.*

5.1.2.2 Buffer

The ramp reference is shared by all pixels within the sensor. Although it is required to distribute this signal to each pixel, the rolling shutter readout allows for only one row of pixels are connected to this reference simultaneously. In MIMADC-SS1, an analog multiplexer gates the ramp signal to the selected row. With respect to a full-scaled sensor, the parasitic capacitance adhering to a row signal wire could be as high as 10 pF. In order to transmit the ramp signal with a small delay and distortion, a buffer following the ramp generator is required to drive the long signal wire.

The main specifications of the buffer focus on the bandwidth, noise and input/output range, while the chip-level integration relaxes the requirements on chip area and power consumption. The schematic of the op-amp used in the buffer is shown in Fig. 5.9.

The op-amp consists of a two-staged structure with a rail-to-rail AB-class output stage as
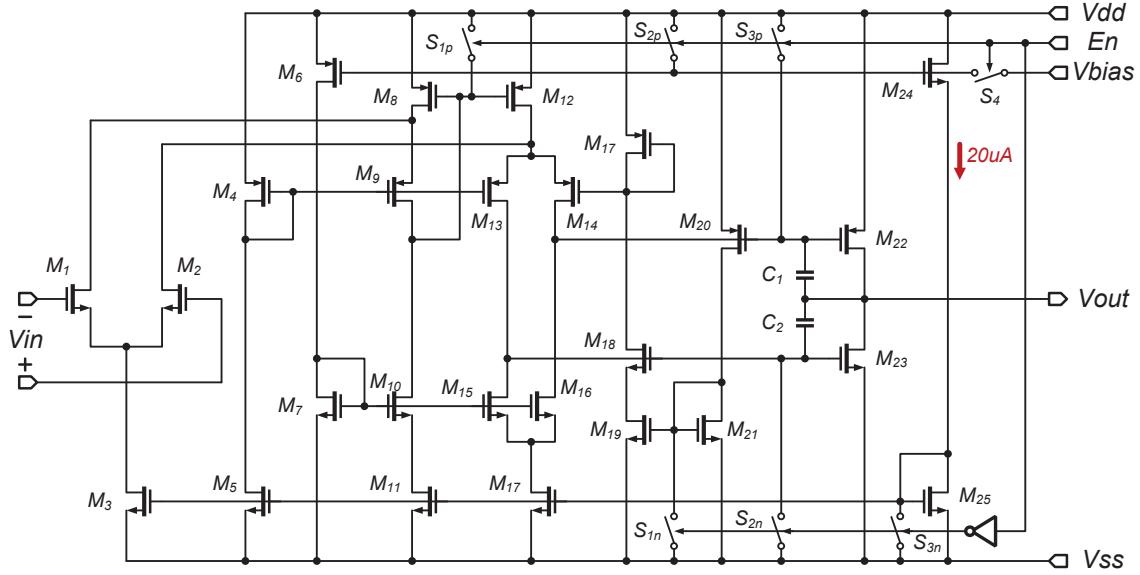
Figure 5.9: *Schematic of the op-amp with rail-to-rail AB-class output.*

given in [2]. The ramp reference has an amplitude larger than 1.2 V. To match the desired dynamic range, a NMOS input stage composed of M_1 and M_2 permits the common-mode input voltage up to the positive supply. Current mirror M_8 and M_{12} sum the opposite-phase input current signal generated from the differential input stage to drive the output stage. Folded mesh composed of M_{13}–M_{16} distributes the input current to drive the output transistor M_{22} and M_{23} as well as to provide a bias voltage. The circuit including M_{18}, M_{19}, and M_{21}, often referred as a minimum selector circuit, controls the quiescent current of the output transistors to keep them operating in the class-AB state. Furthermore, this circuit also determines the minimum current when one of the output transistors is driven hardly. The current in both output transistors M_{22} and M_{23} are measured by M_{20} and M_{18}, and then feed back to the minimum selector circuit. The output of the minimum selector circuit is represented by the gate voltage of M_{17}. The M_{13} and M_{14} form an amplifier to clamp the gate voltages of M_{17} and M_4 to a same value. Therefore, the biasing of M_{18} is set to the class-AB state by the feedback loop.

By setting the M_{19} working in the linear region, when the output voltage is equal to the common-mode output voltage that no current is drawn by the load, the corresponding quiescent current of the output stage can be calculated as

$$I_{Q22} = 2 \cdot \frac{W_{22}L_{20}}{W_{20}L_{22}} \cdot I_{M4} . \tag{5.5}$$

As soon as one of the output transistors is biased with a large current, the folded mesh combining with the minimum selector control the current in the other output transistor has a

non-zero minimum value to be half of the quiescent current $I_{Q22,23}$. Miller capacitors C_1 and C_2 are connected across output transistors to compensate the op-amp. The unit-gain frequency of the op-amp is given by

$$\omega_0 = \frac{g_{m1,2}}{C_1} \, , \tag{5.6}$$

where $g_{m1,2}$ is the transconductance of the input transistors M_1 and M_2. The first non-dominant pole is

$$\omega_1 = \frac{g_{m22}}{C_{GS22} + C_L + \dfrac{C_{GS22}}{C_1}C_L} \, , \tag{5.7}$$

where C_{GS22} is the gate-source capacitance of the output transistor and C_L is the load. For a phase margin of $\sim 60°$, the unit gain frequency ω_0 should be two times less than the ω_1.

The simulated performances of the op-amp are summarized in the Table 5.2.

Parameter	Value
Open-loop	
Gain@DC [dB]	103.2
Quiescent current [mA]	1.21
Offset voltage [mV]	1.27
Phase margin [degree]	83.15
0-dB Bandwidth [MHz]	131.5
Input noise@1–100 MHz [μV]	92.68
Common-mode input range [V]	0.5 – 1.7
Common-mode output range [V]	0.1 – 1.7
Closed-loop unit gain (Buffer)	
-3dB Bandwidth [MHz]	315.4
Input noise@1–100 MHz [μV]	92.92
Input/Output range [V]	0.5 – 1.7

Table 5.2: *Summary of the simulation results in terms of the op-amp connected in unit-gain. (10 pF capacitance load).*

5.1.2.3 Column-ended memory

Referring to the concept of column-level SAR logics in MIMADC-SAR, the memories in this matrix are also moved to the end of column, and shared by the pixels within the corresponding column. This architecture relaxes the demand on the silicon area and allows implementing the memories by the flip-flop gates provided in the standard cell library.

The column-ended memory is composed of three D-type flip-flops. Their data inputs are connected to the 3-bit timing stamps generated by the on-chip binary counter, and the clock inputs are tied together to the output of the comparator. As soon as a change appearing at the comparator output, the flip-flops saves the timing stamps, and then are waiting for the parallel-to-series converter to read out these codes.

If the 3-bit ADC output is "000", the output of the comparator will not charge to trigger the flip-flops. Therefore, the flip-flops should be reset periodically at the beginning of each conversion.

5.1.3 Layout

5.1.3.1 Pixel matrix
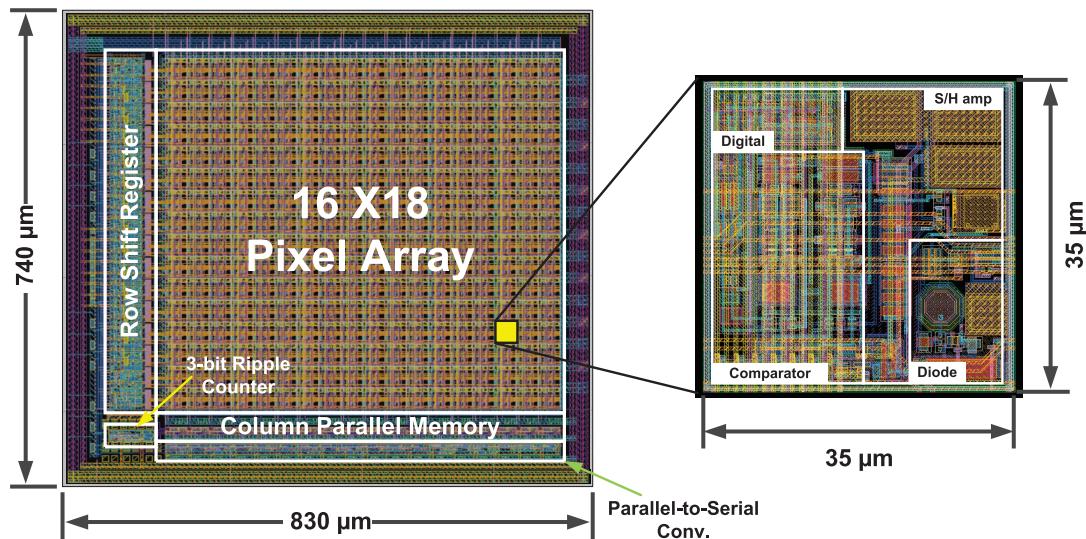
Figure 5.10: Layout of the MIMADC-SS1 pixel matrix combining with a zoomed view of the pixel.

The layout of the MIMADC-SS1 is shown in Fig. 5.10, where the matrix is composed of 16×18 pixels with the pitch of 35 µm. Total 18 column-ended digital memories are placed at the end of matrix. The shift registers at the left of the matrix make up the rolling shutter control circuits. The control signals and the ramp signal are input to this part and then allocated to the activated row. The column-level 3-bit memories only contribute a negligible insensitive area for the sensor.

As illustrated in Fig. 5.10, the floorplan of the pixel in MIMADC-SS1 is almost same as the SAR one except that the DAC is removed. So more pixel area can be spared for the comparator, the additional guard ring, and substrate contacts. In contrast to the pixel of MIMADC-SAR, the 7 reference signals are replaced by a ramp signal. At the same time, no feedback loop exists between the pixel and column circuits , which simplifies the signal links. In consequence, the difficulty of the signal routing is greatly relaxed in this matrix, and less crosstalk exists among the various signal wires.

5.1.3.2 Peripheral

The layouts of the ramp generator and the following buffer are depicted in Fig. 5.11, where the size of the ramp generator and the buffer are 200×80 µm^2 and 130×80 µm^2, respectively. In order to reserve sufficient metal layers for the global signal routing, only metal layers M_1–M_3 are used in the layout.
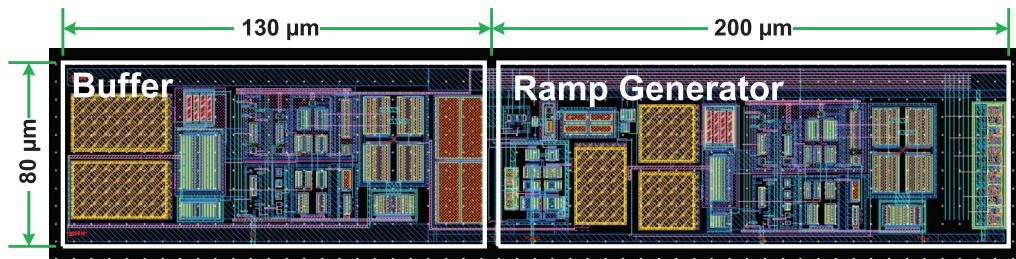

Figure 5.11: *Layout of the ramp generator and buffer.*

## 5.2 Pixel-level SS ADC with in-pixel memory

The previous two pixel matrices (MIMADC-SAR, MIMADC-SS1) shift a part of ADC circuits from pixel to the column, maximizing the circuit sharing and utilization. This concept is effective to implement complicated circuits within a limited pixel area. However, the maximum achievable frame rate of this architecture is severely limited. As stated before, in a typical row-by-row rolling shutter, the frame time is equal to the product of row number and readout time of each pixel. The row number is determined by the pixel pitch and sensor size, both of them cannot be changed arbitrarily for a given application. The readout time of the pixel depends on the pixel circuits. Without an improvement in circuit architectures, it is difficult to improve the readout speed further.

Double-sided readout is an intuitive method to halve the frame time but at the cost of an additional insensitive zone. The multi-row parallel readout can further enhance the speed. Even though the acceleration of the frame rate is generally at the cost of more power consumption, in some application such as inner layer of VTX, the design concentrates more on the speed and an increase of power is essential. Thus to conceive a proper sensor architecture is meaningful. The existence of the column-ended circuits shared by column of pixels is prevented from the multi-row readout, since more than one pixel operate at the same instant. To overcome this drawback, moving the column-ended circuits into the pixel is the direct choice. In this section, we present a matrix called MIMADC-SS2, where the pixel is integrated with a complete signal chain covering particle sensing, amplification, A/D conversion, and data storage. Compared with the architecture of MIMADC-SS1, the in-pixel data storage allows employing the various readout methods, ranging from single-row to multi-row rolling shut-

ter, and even global shutter. Therefore, this architecture can reach a faster frame rate than others.

5.2.1 Architecture
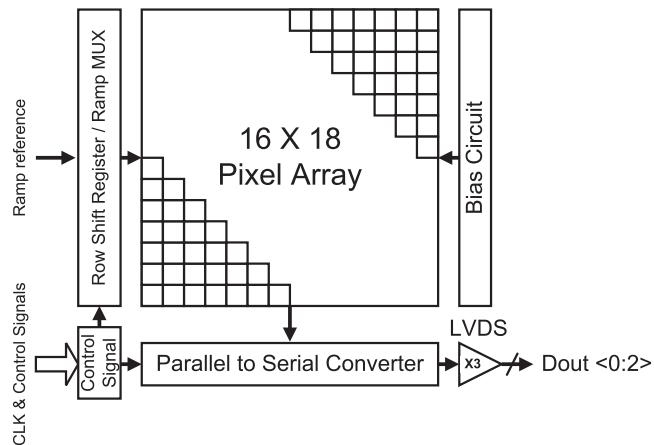
Figure 5.12: Architecture of MIMADC-SS2 pixel matrix.

As shown in Fig. 5.12, the architecture of MIMADC-SS2 is similar to the MIMADC-SS1. The prominent difference is no column-ended memories at the bottom of the matrix. The timing stamps generated by the on-chip binary counter is distributed to each pixel, the same as ramp reference. For the purpose of simplifying the design and to be compatible with the existing testing system, the single-row rolling shutter readout method is still used in this sensor. While it should be noted that this pixel architecture is capable to arrive at a high level parallel readout i.e. multi-row rolling shutter and global shutter. Other blocks including ramp generator, parallel-to-series converter, and LVDS are reused as those in the MIMADC-SS1.

5.2.2 Circuit implementation

The pixel schematic of the MIMADC-SS2 is depicted in Fig. 5.13, where a pixel includes sensing element, S/H amplifier, comparator, and memories. The fundamental blocks are identical to the previous sensors, while for the implementation of in-pixel integration, some improvements are performed on the circuits design. These improvements are studied in detailed as follows.

5.2.2.1 Open-loop S/H amplifier

In the previous two matrices, the S/H amplifier is operated in a closed-loop scheme with a capacitance feedback. This structure features a high linearity and is insensitive to process variations, whereas at the cost of the larger pixel area occupied by the feedback capacitors. In order to reserve sufficient pixel area for incorporating the memories, the large passive
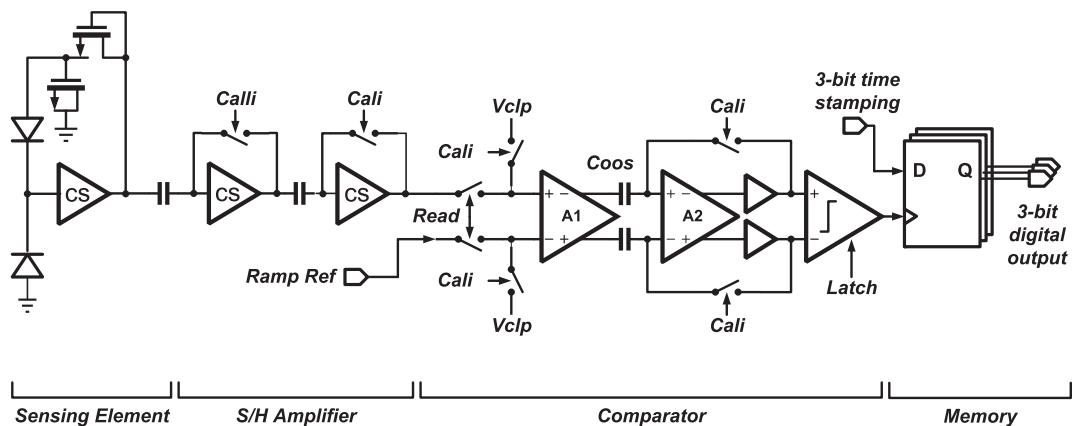
Figure 5.13: *Schematic of the pixel in MIMADC-SS2.*

components cannot be used in the pixel circuits. As a consequence, the open-loop amplifier is a potential choice.
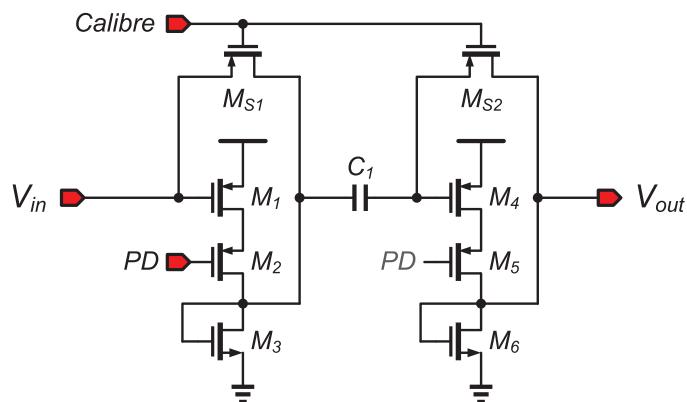
Figure 5.14: *Schematic of the open-loop S/H amplifier.*

Figure 5.14 is the schematic of the open-loop S/H amplifier. A two-staged CS amplifier ensures a sufficient gain for S/H amplifier. The offset suppression technique is employed to remove the offset. As stated in Section 4.3.3.2, both IOS and OOS are the possible choices. Despite a good performance in the offset cancellation, two drawbacks prevent the use of OOS. First, with respect to OOS, because of the uncertainty of the clamping turn-off time, the mismatch of channel charge injection between the clamping switches introduces an offset. This issue can be resolved by delaying all clamping switches with in a certain sequence. However, this special timing complicates the generation of the controls signals. Second, the clamping voltages acting as the input bias for the amplifiers used in OOS are set by the fixed voltages. The change of the operating points due to process variations is capable to drive the amplifier out of the high gain region. In contrast, the input bias of IOS is set by the feedback. This self-biased structure makes the amplifiers insensitive to the process variation. Because of these reasons, the IOS scheme is used in this S/H amplifier.

The operation of the S/H amplifier is controlled by the calibration signal "calibre". During "calibre" is low, the offsets of the CS amplifiers are stored in the inter-stage capacitors. In the next "read" phase, the clamping switches are open, and then both CS amplifiers are operating in an open-loop mode to amplify the input signal.

The main issues with the open-loop amplifier are linearity and performance dispersion. In contrast to the closed-loop amplifier whose gain is only related to the ratio of passive components, that of open-loop amplifier strongly depends on the operating points and transistor parameters. The change in the operating points directly results in a variation of the gain, thereby translating into a poor linearity within the input range. Since the process variation generally is random in the spatial distribution, the uncertainty of pixel output responses for a given input introduces a FPN. Therefore, an analysis is necessary to provide more insight into the behavior of CS amplifier.

The CS amplifier is composed of two transistors that one is the input and the other acts as the load. The input transistor is formed by a PMOS due to its superior feature in low $1/f$ noise. The load can be implemented by either NMOS or PMOS. The reason to select which type transistor as the load depends on the requirements on the linearity and process variation sensitivity.

Region	M_1	M_2
❶	lin.	sat.
❷	sat.	sat.
❸	off	off

(a)   (b)   (c)
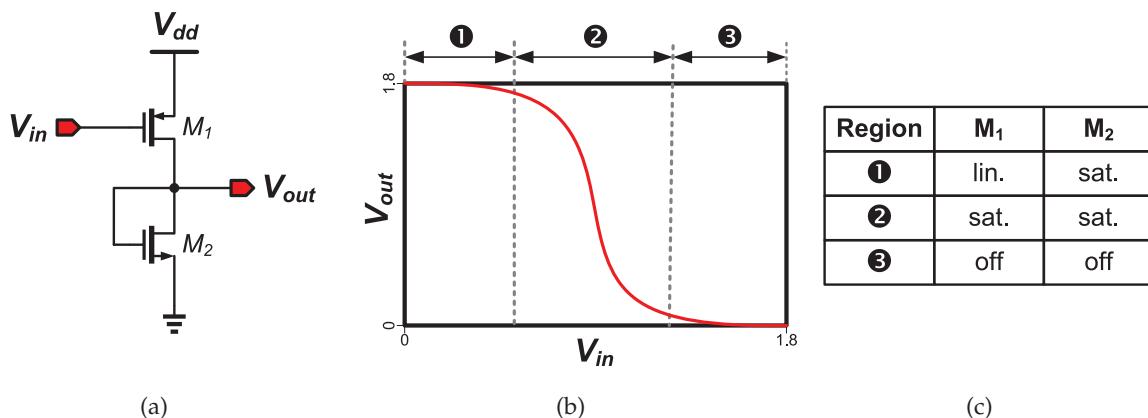
Figure 5.15: Input/output transfer characteristic of a CS amplifier: (a) the schematic of the CS amplifier, (b) the transfer curve, and (c) a summary of operation status of the transistors, where "lin.", "sat.", and "off" represent linear, saturation, and cutoff regions respectively.

Considering a CS amplifier shown in Fig. 5.15(a), the input/output response can be depicted in Fig. 5.15(b), where the transfer curve can be divided into three parts, i.e. regions 1–3. The operations of the CS amplifier within these regions are discussed next.

- **Region 1** : In this region, the input, V_{in}, begins to increase from zero. Since V_{in} is small enough, a large current drawn by M_1 pulls the output V_{out} to high, and thereby M_2 in saturation region. When $V_{in} - V_{out} < V_{th1}$ is established, where V_{th1} is the threshold voltage of M_1, transistor M_1 operates in linear region. As the increase of V_{in}, the current is reduced. In the linear region, the current of M_1 is not only related to the V_{in}, but also

to V_{out}. The decrement of current due to the increase of V_{in} is partially compensated by the rising of V_{out}. Therefore, the amplifier operating in this region exhibits a small gain.

- **Region 2** : With the increase of V_{in}, the current is great reduced. As soon as $V_{in} - V_{out} > V_{th1}$, M_1 turns into the saturation region. The decrement of current in M_1 is completely contributed to the output, thus a high gain can be achieved. Based on the current equation of the saturated transistor, and the case that an identical current flows in both M_1 and M_2, the output voltage V_{out} can be obtained as

$$V_{out} = -\alpha \cdot V_{in} + \alpha \cdot (V_{dd} - |V_{th1}|) + |V_{th2}| , \qquad (5.8)$$

where V_{dd} is the power supply, V_{th1} and V_{th2} are the threshold voltages of M_1 and M_2 respectively. The coefficient α is the square root of quotient between the aspect ratios of M_1 and M_2 aspect ratios, given as

$$\alpha = \sqrt{\frac{\mu_p W_1/L_1}{\mu_n W_2/L_2}} . \qquad (5.9)$$

where μ_p and μ_n are the hole-carrier effective mobility and electron-carrier effective mobility, respectively. Deriving both side of Eq. (5.8), the gain A_v can be calculated as

$$A_v = -\alpha . \qquad (5.10)$$

Equation (5.10) indicates that the gain only depends on the property of silicon and the aspect ratio of transistors. For a given circuit, this value is constant. It should be noted that the current equations used in Eq. (5.8) is derived from an approximate model without considering some second- or high-order effects. Thus the deviation exists between the calculated gain and actual one.

- **Region 3** : The input V_{in} is large enough that $V_{in} - V_{dd} > V_{th1}$. Both M_1 and M_2 turn off and no current flows in the transistors. The output voltage is pushed to low. The gain in this operating region is close to zero.

In conclusion, the region that both transistors are in saturated, demonstrates a gain with a maximum value and less sensitivity to the variation of process and bias. As a consequence, the behavior of the amplifier in this region is crucial for circuit design, thereby deserving a detail analysis.

Besides gain, input range is also important for the open-loop amplifier. However, the limited power supply impose a trade-off between the requirements between both input range and gain. As illustrated in Fig. 5.16, for a given power supply, a high gain always results in a narrow input range.

For the reason of the linearity requirement in our design, we desires the amplifier features a flat gain within an as large as possible input range. Figure 5.17 shows the gain and input
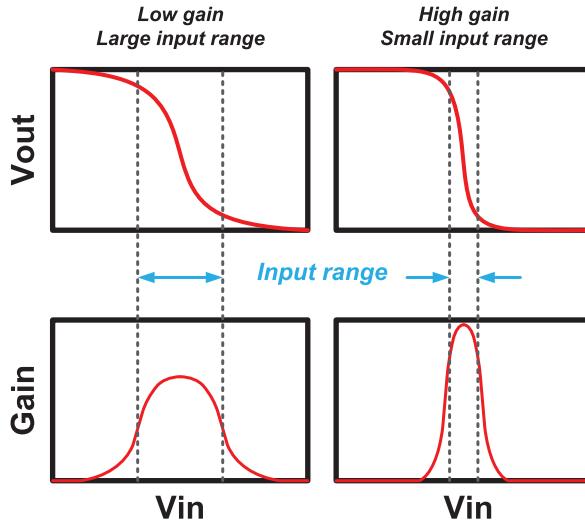
Figure 5.16: *The relation of input range and gain in an open-loop amplifier. Here, the input range is defined by the voltage at which the gain drops 3 dB below peak. In the left two figures, the transfer curve is flatter, leading to a low peak of gain but a wide input range. The case in the right figures, in contrast, exhibits a high gain peak and a narrow input range.*

range of a CS amplifier at the different aspect ratios for both transistors, where the input range is defined as the voltage range that the corresponding gain value is higher than $1/\sqrt{2} \approx 0.707$ of its maximum value, i.e. the -3dB gain rolling off range. It is obvious there is an inverse proportion between gain and input range. The peak value of gain is ~ 11.5, but the input range is only 61 mV. As the gain is fallen to ~ 2.6, the input range is enlarged to 386 mV.

(a)

(b)
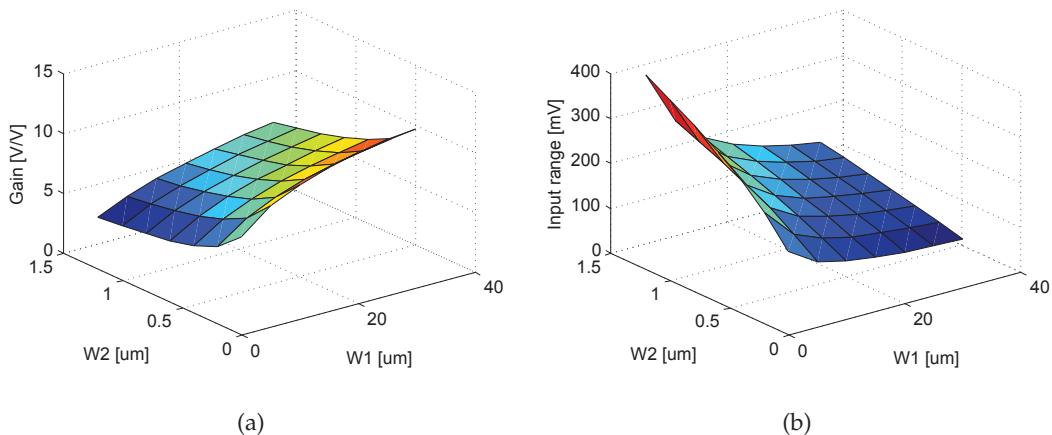
Figure 5.17: *(a) Gain, and (b) input range of a CS amplifier with various transistor aspect ratios. These results are acquired by assuming that the length of both transistors are 1 μm.*

In our design, we select the CS amplifier featuring a relative wide input range but at the cost of low gain. The insufficient gain can be compensated by cascading two CS amplifiers. Compared with the PMOS load, the NMOS one provides less output resistance to meet the low gain requirement. The schematic of the CS amplifier with the transistor aspect ratio and

operational points are presented in Fig. 5.18(a), and the simulated transfer curve is depicted in Fig. 5.18(b). The simulated peak gain is ∼4.95 dB at the input voltage of ∼1.2 V, which corresponds a -3 dB input range of ∼148 mV. Since the operating point at the amplifier input is set by the unit-gain feedback in IOS, the simulated input voltage is indicated in Fig. 5.18(b) and the corresponding gain is ∼4.93 dB, very closed to the peak value.

<div align="center">(a)</div>

<div align="center">(b)</div>
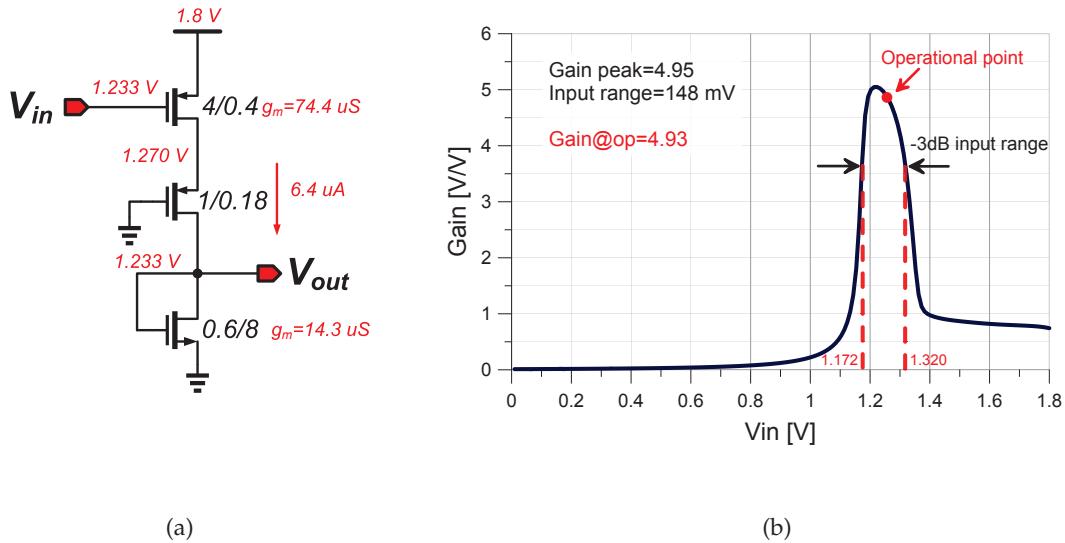
Figure 5.18: *(a) Schematic of the CS amplifier with the transistor aspect ratio and operational point, and (b) the simulated transfer curve.*

The previous simulation results are dedicated to the single CS amplifier. Next, the performances of the S/H amplifier, which is composed of two CS amplifiers operating in IOS scheme. A simulation of 1000 times Monte-carlo has been performed at a sweep of the input voltage. The transfer curve and gain of S/H amplifier at the various inputs are plotted in Fig. 5.19(a). The deviation of output voltage and gain due to process variations and component mismatch are also provided in the same figure.

The temporal noise of the S/H amplifier is ∼0.18 mV calculated by 1000 times TNS. Compared with the temporal noise of the closed-loop amplifier mentioned in the previous sections, the noise of open-loop one is slightly less. The possible reason is the open-loop architecture features a simpler topology, thereby resulting in less noise contributor in the circuit.

5.2.2.2 Comparator

In the pixels of the MIMADC-SAR and MIMADC-SS1, the positive input of the comparator is connected to the CDS capacitor at the output of the S/H amplifier. The output impedance of the S/H amplifier exhibits a very high value, which results in an input feedthrough from the DAC or ramp reference. Therefore, a pair of buffers are inserted before the comparator
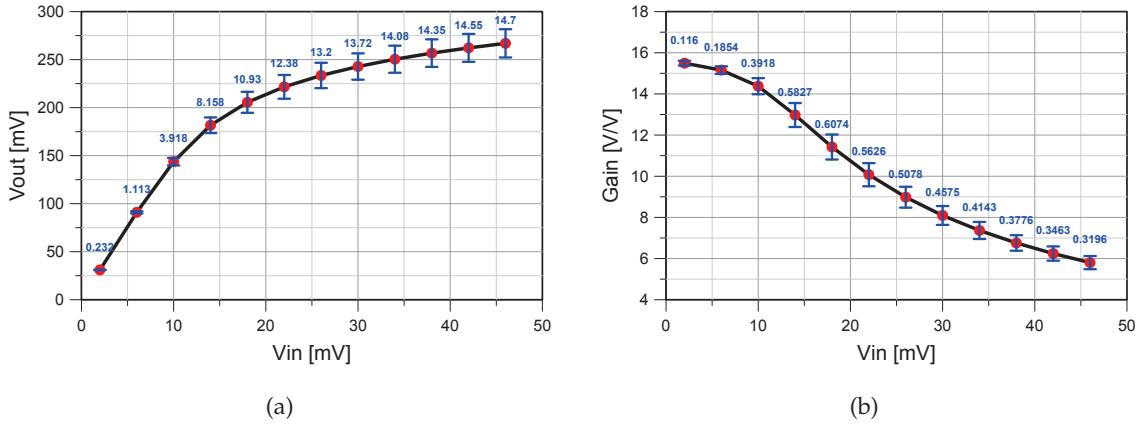
Figure 5.19: *Simulation results of the S/H amplifier: (a) input/output transfer function and (b) the corresponding voltage gain. The values used to plot the curve are the mean value of the simulated results. The error bars are used to represent the standard deviation of results due to the process variation and component mismatch. The unit of the values on the error bars is millivolt. In the simulation, the input voltage is inject into the amplifier via a coupling capacitor. Thus, both "Vin" and "Vout" in this figure are the relative values to represent the net input and output voltages.*

inputs to handle this problem. In the MIMADC-SS2, no capacitor exists at the output of the S/H amplifier, and this node is directly connected to the input of comparator. Compared with the closed-loop amplifier, the CS amplifier generally features a lower impendence. As a result, the effect of the input feedthrough is greatly attenuated, and thus the corresponding buffers in the previous architecture are not necessary.

The rest of circuits in comparator including both pre-amplifier and latch are identical to those in MIMADC-SS1. The designs and simulation results of them can refer to the previous sections.

5.2.2.3 In-pixel memory

The in-pixel data storage provides the sensor a flexible readout strategy. In MIMADC-SS2, each pixel integrates an independent memory to record the 3-bit digital results generated by the ADC.

As illustrated in Fig. 5.20, the memory cell is implemented by three D-type flip-flops. Compared with other memory structures, the D flip-flop memory can eliminate the sensing amplifier, and then reaches a very high readout rate. Additionally, improved radiation hardness is also possible because of no sensing amplifier. The only disadvantage is the larger size. In this prototype, we select the D flip-flop directly from the digital standard cell library. A customized design can further reduce this size.
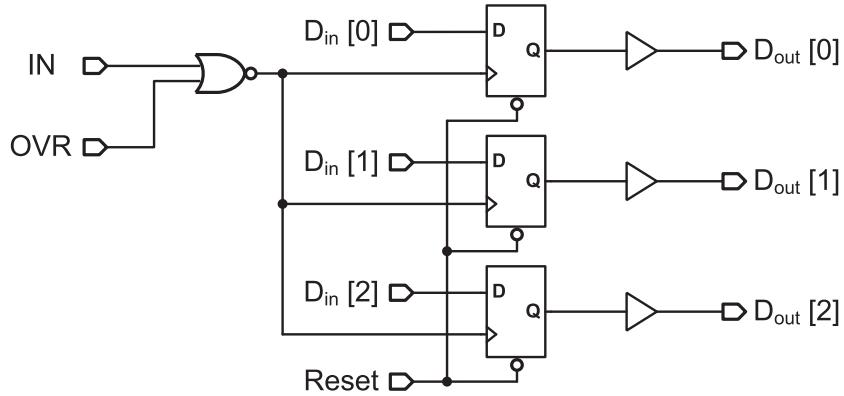
Figure 5.20: *Schematic of the in-pixel memory used in MIMADC-SS2.*

5.2.3 Layout

As shown in Fig. 5.21, the layout of the MIMADC-SS2 consists of 16×18 pixels. The pixel pitch is 35 μm that is same as other two matrices. The one-row rolling shutter readout is performed by a shift register control circuits at the left of the matrix. Benefiting from the use of the in-pixel memory, no column-ended circuit is demanded. The digital results stored in the pixel is read out in sequence, then formatted by a parallel-to-serial converter, and finally transmitted by 4 LVDS links.
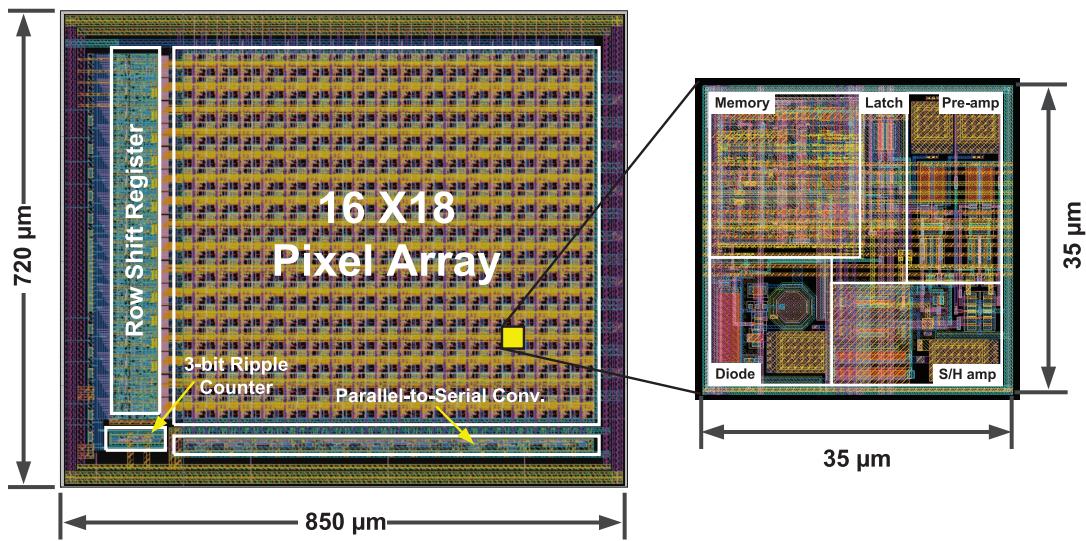

Figure 5.21: *Layout of the MIMADC-SS2 pixel matrix combining with a zoomed view of the pixel.*

Figure 5.21 is the layout of a pixel. The size of the sensing element and S/H amplifier is reduced compared with the pixel in other matrices. More pixel area therefore is spared for the in-pixel memory. The memory including three D flip-flops occupies approximate 1/3 pixel area. In order to reduce the pixel size further, more advanced process can be used to reach a small size for the digital cell. Moreover, the customized memory can be utilized.

5.3 Conclusion

Two pixel matrices are presented in this chapter. Both of them are aiming to implement SS ADCs within an area-limited pixel. The SS ADC features a merit in the simple structure which is helpful to reach a compact layout. In the MIMADC-SS1 matrix, the memory circuits are placed at the end of column. The closed-loop S/H amplifier is used in the pixel of MIMADC-SS1 targeting a good linearity. In the matrix MIMADC-SS2, a two-staged CS amplifier operated in an open-loop mode is used. The area saved by the S/H amplifier is used to place the in-pixel memory. No column-ended circuits exist in this sensor structure. The cost is the poor linearity and process sensitivity. Some techniques are used in the design to alleviate these effects.

In order to generate a ramp reference for the slope ADCs in both matrices, an on-chip ramp generator has been designed. To be different from the conventional ramp generator which operates based on charging a capacitor with a constant current, our design uses an adaptive architecture. The main parameters of the ramp output (e.g., rise time) can be regulated on board. The feedback structure in this circuit also ensures that the output voltage has a high linearity and a good tolerance to process variations.

The scales of both matrices are identical to be 16×18 matrix with a 35×35 μm^2 pixel size. The resolution of the pixel-level ADC is 3 bits. The conversion time is $\sim$ 180 ns driven by a clock of 100 MHz.

Bibliography

[1] F. Azais, S. Bernard, Y. Bertrand, X. Michel, and M. Renovell, "A low-cost adaptive ramp generator for analog BIST applications," in *VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001*, 2001, pp. 266–271.

[2] K.-J. de Langen and J. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 10, pp. 1482–1496, Oct 1998.

Characterization of MIMADC chip

The prototype MIMADC described in the previous chapters has been fabricated in the TowerJazz 0.18 μm CIS process. These matrices are implemented in the chip aiming to verify the concept of pixel-level ADCs with a variety of architectures. Figure 6.1 shows the microphotograph of the MIMADC chip with a chip size of $1.7{\times}3.7$ mm^2. The serial ADC outputs are transmitted by four pairs of LVDS drivers which are multiplexed by three matrices. The chip clock signal is input by a pair of LVDS receiver. Two ramp generators are integrated on the chip: one generates the ramp reference shared by the two matrices with single-slope type ADCs; the other one has an independent output pad allowing us to test the performance of the ramp reference. Besides, the input of the ramp reference can also be switched to an external reference. By configuring manually the switches on the test board, each pixel matrix can be tested separately.
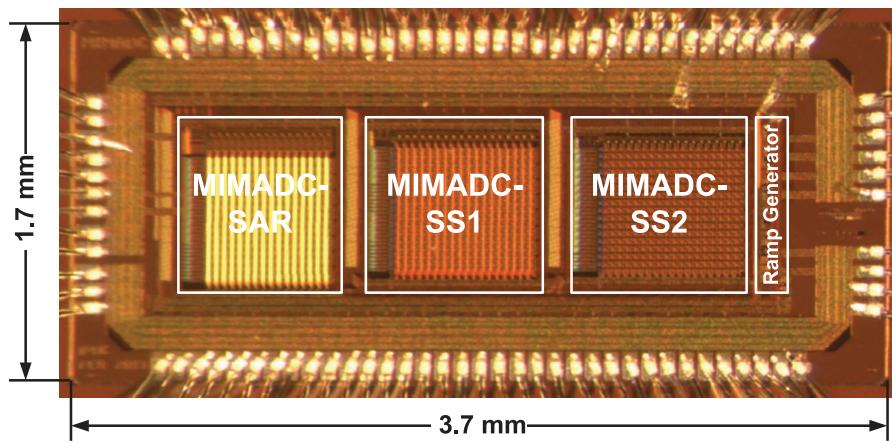

Figure 6.1: *Microphotograph of the MIMADC chip: the left one is the 16×16 pixel matrix with SAR ADCs (MIMADC-SAR); the middle one is the 16×18 pixel matrix with SS ADCs and column-level memories (MIMADC-SS1); the right one is the 16×18 pixel matrix with SS ADCs together with the in-pixel memories (MIMADC-SS2).*

This chapter will start with an introduction of the measurement setup. Then the measured results in terms of the three pixel matrices will be presented. Finally, the measurement results

are summarized.

6.1 Measurement system
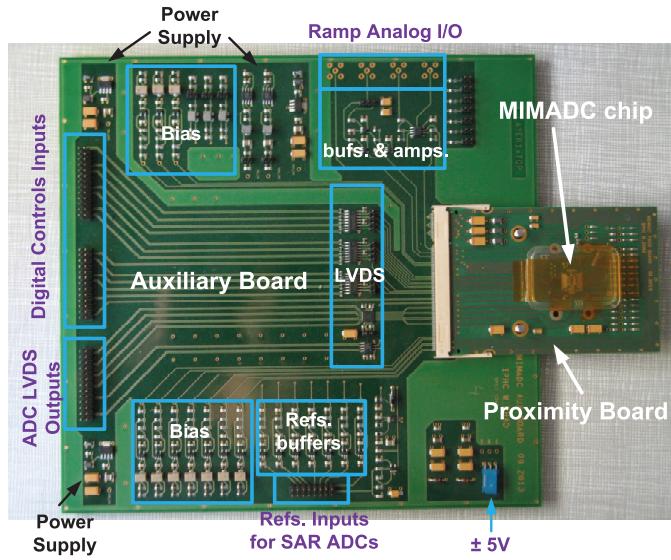
Figure 6.2: *Photo of the test boards. A proximity board is inserted into the auxiliary board via a SO-DIMM connector. The MIMADC chip is wire bonded on the proximity board, and the polarization signals, I/O buffers and power supplies are provided by the auxiliary board.*

Two test boards have been designed and manufactured in this thesis. As shown in Fig. 6.2, the MIMADC chip is wire bonded on the proximity board that contains a SO-DIMM (200 pins, small outline, dual in-line memory module). The proximity board can be plugged into the auxiliary board which carries the functionalities including the bias signal generators, LVDS, DAC and power supplies. This approach provides enough flexibility in changing the different DUTs (device under tests), resulting in a reduction of the cost in preparing the additional test boards.

The proximity board provides mechanical support for the MIMADC chip, capacitors as noise filters and resistors for impedance matching. The ADC LVDS output signals of the chip are acquired by the LVDS buffers on the auxiliary board to achieve a far-distance, high-speed data transmission between the test board and the instruments. The auxiliary board contains seven LVDS drivers for the external digital control signals, and seven voltage buffers for the voltage references of the SAR ADCs. In order to measure the ramp generator and the buffer integrated in the MIMADC, four analog ports are equipped on the auxiliary board. Both the proximity and auxiliary boards are implemented in a 6-layer process, and the proximity board is thinned down to ∼1 mm to match the SO-DIMM standard.

Figure 6.3 illustrates the diagram of the acquisition system for the data analysis of the
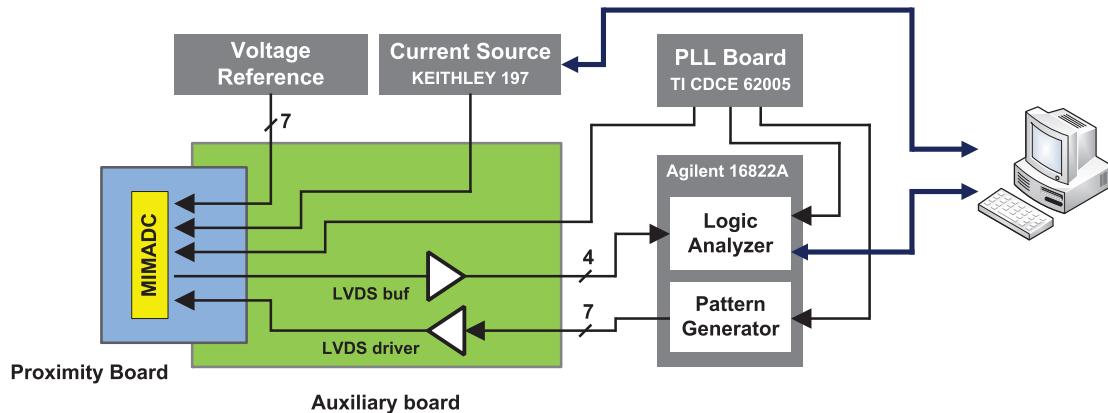
Figure 6.3: *Diagram of the acquisition system.*

MIMADC chip. A PLL clock generator board[1] supplies the system clock to the chip, and sends the trigger signals to the logic analyzer. This arrangement can reduce the signal jitter and assures the synchronous operation among the chip, control signals as well as the output data sampling. The ADC outputs on the auxiliary board are captured by the logic analyzer (Agilent 16822A) with a PC interface. The built-in pattern generator in the logic analyzer produces the control signals to the chip. To test the SAR ADCs, seven references are produced by a voltage generator including a resistor ladder. The injected test input signal is generated by a current source instrument (KEITHLEY 237) that can offer a high precision current signal in the order of microampere. This current is transferred to a voltage by a 100 Ω resistor. During the measurement, the current generator programmed by a PC injects a desired input signal to the chip, and the corresponding serial ADC outputs are recorded by the logic analyzer. Sweeping the input current linearly within a desired range, the transfer function of the ADCs is obtained. Additionally, the tests can be performed at various clock frequencies by configuring the PLL board to exploit the frequency-dependent performance of the ADCs.

6.2 Test results of SAR-ADC matrix

As the analog input voltage is increased, the "ideal" ADC (noise-free ADC) maintains a constant output code until the transition region is reached, at which point the output code instantly jumps to the next value. An "ideal" ADC has zero "code transition" noise, and a transition region width equal to zero. A practical ADC has some amount of "code transition" noise, and thus a transition region width larger than zero. Today, *code transition noise* is commonly referred to as *input-referred noise* [1]. The input-referred noise is most often characterized by examining the histogram of a large number of output samples when the input to the ADC is a dc value. Since the noise is approximately Gaussian, the standard deviation of the histogram corresponds to the input-referred rms noise . This approach concerns only

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1. Designed by K. Jaaskelainen

the input-referred noise, but without the noise due to quantization error and distortion which only occur when an ADC is processing an ac signal (which is not the case in our application). To distinguish from static noise such as FPN (Fix Pattern Noise), we refer the input-referred noise as temporal noise (TN) in the following content.

6.2.1 Noise performance

To test the SAR-ADCs in the chip, we sweep the input voltage from zero to the full scale. The corresponding output starts from the minimum code "000" and finally reaches the maximum code "111". A large number of frames are recorded repeatedly for each input value. By accumulating the probability of the output codes, a transfer curve can be drawn. Near the transition position, the temporal noise leading to a shift of output between the two neighbouring codes. The resulting transfer curve is broadened to a "S" shape. The width of the transition region corresponds to the peak-peak value of temporal noise. The midpoint of the transfer function approximates the transition point in a noise-free case. Due to the process dispersion, the transition points of different ADCs present a dispersion which is approximately Gaussian, and the associated standard deviation is referred as FPN.


(a)   (b)
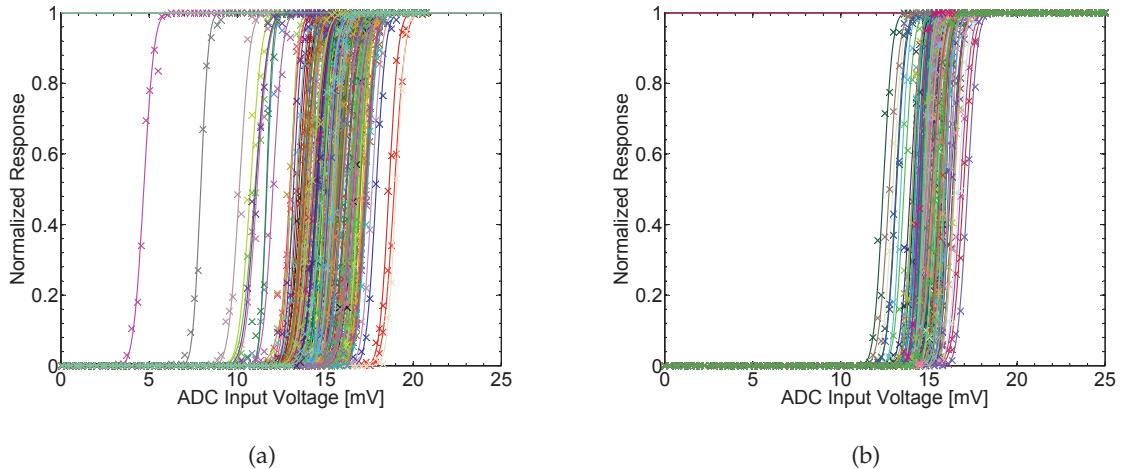
Figure 6.4: *Normalized response of the 256 pixel-level SAR ADCs at a clock frequency of (a) 100 MHz, and (b) 50 MHz, respectively. The cross symbols represent the measured data, and the solid curves are the fit results by error functions.*

Figure 6.4(a) shows the S-curves of all the 256 pixels in the SAR-ADC matrix, measured at the first transition step corresponding to the output code from "000" to "001". The operational frequency reaches the goal of design, a clock frequency of 100 MHz. Most of the curves are centered around a transition position of ∼15 mV, but still some individuals are located far from them. This case cannot be explained by the devices mismatch because it does not comply with the Gaussian distribution. A test under the same circumstance was performed but at a half clock frequency of 50 MHz. The measured result is shown in Fig. 6.4(b). The dispersed

curves existing in the case of 100 MHz disappear, presenting a good concentration of all curves. This comparison indicates that a high operational frequency will degenerate the FPN. The possible reason is the crosstalk from the digital circuits as discussed later on.


(a) (b)
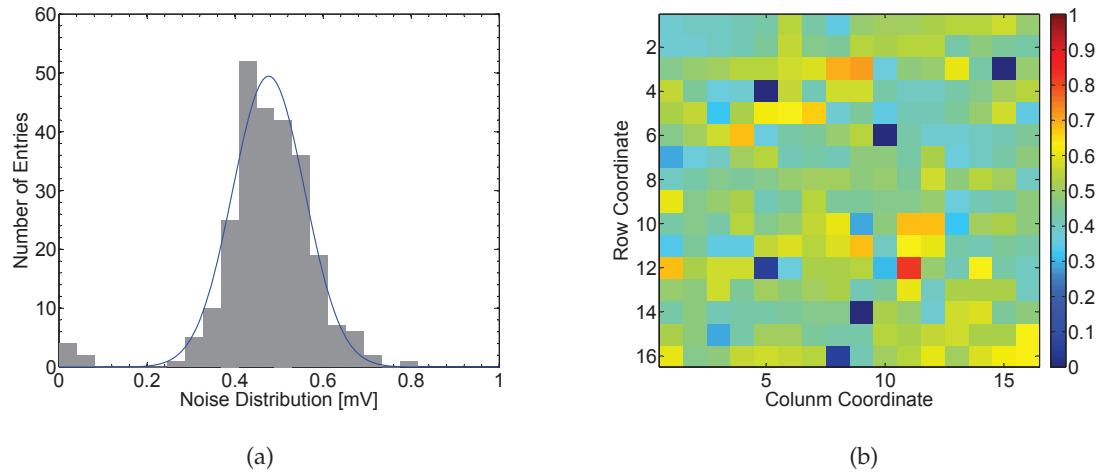
Figure 6.5: *Temporal noise distribution of the 256 pixel-level SAR ADCs. (a) Histogram of the TN. The mean value is 0.476 mV, and the standard deviation is 0.116 mV. The mean value is the average rms noise of all the ADCs. (b) Spatial distribution of the TN within the whole matrix. The unit of color-bar is mV. There are 6 dead pixels in this matrix. They exhibit the very small TN values.*

The temporal noise can be calculated by fitting the transfer curve with an error function (erf); its derivative gives a gaussian (normal) distribution. The statistical result of the temporal noise obtained on the 256 ADCs at a 100 MHz clock is plotted in Fig. 6.5(a). From Fig. 6.5(a), the extracted mean TN is 0.48 mV. The spatial distribution of the noise on the 16×16 SAR-ADCs is given in Fig. 6.5(b). We can observe that except several hot pixels that displays a significant higher noise than other pixels, noise of the rest pixels is uniform and has no certain spatial pattern.

The distribution of the transition points of all ADCs is presented in Fig. 6.6(a). The FPN is computed to be 1.10 mV. At each transition step, the extracted FPN is shown in Fig. 6.6(b). At the last two transition regions (code transfer from "101" to "110" and "110" to "111"), the FPN is significant larger than the preceding ones. The most likely explanation of the frequency dependent FPN is the presence of the crosstalk among the different circuits. Reviewing the layout of the pixel shows that the row buses for the reference voltages REF<5> and REF<6> are very closed to the output of latch which has a high activity as well as a rail-to-rail swing range. The crosstalk between them will introduce the noise to the reference voltages.

The above results are measured at the desired clock frequency of 100 MHz. Generally, temporal noise originates from resistor noise and "KT/C" noise, while FPN mainly arises from mismatch in the individual pixel. Both TN and FPN are independent of operational frequency. In practice, the crosstalk among the transmission lines and devices as well as the substrate also

(a)   (b)
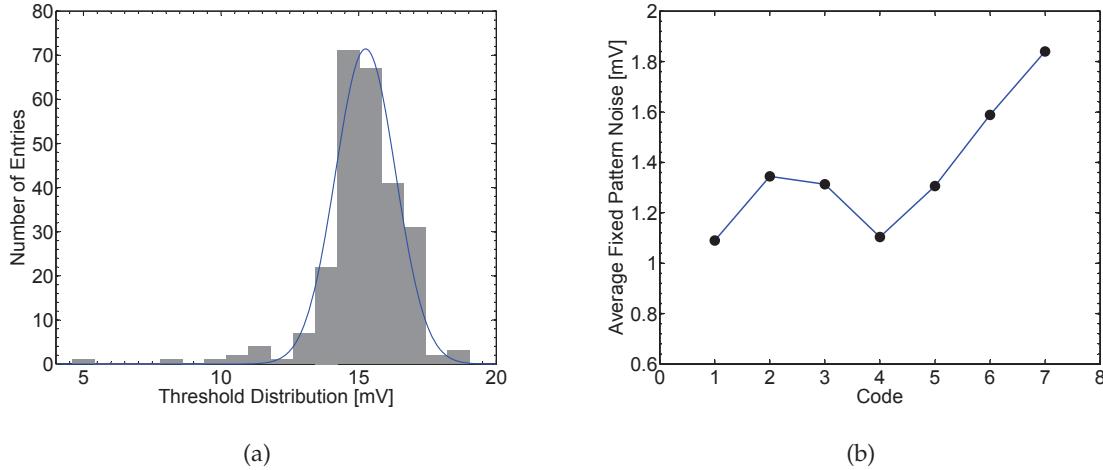
Figure 6.6: *Distribution of the fixed pattern noise (FPN) of 256 pixel-level SAR ADCs. (a) Histogram of the FPN as well as the fitting result by a Gaussian function. The standard deviation, i.e. average FPN, is 1.10 mV. (b) Average FPN measured at each transition step.*

introduces additional temporal noise and FPN. In order to exploit whether the temporal noise and FPN are affected by the operational frequency, both parameters are measured at various clock frequencies. The results are presented in Fig. 6.7. Both the temporal noise and the FPN of the SAR-ADCs matrix degrade with the operational frequency. The pixels in the MIMADC-SAR and the MIMADC-SS1 share the same S/H amplifier and comparator. Since the test result of the SS1 matrix (will be stated in the next section) shows no frequency-depended performances, it implies that the performance degradation with frequency in the SAR matrix is caused by the crosstalk on the transmission lines of the 7 reference voltages.
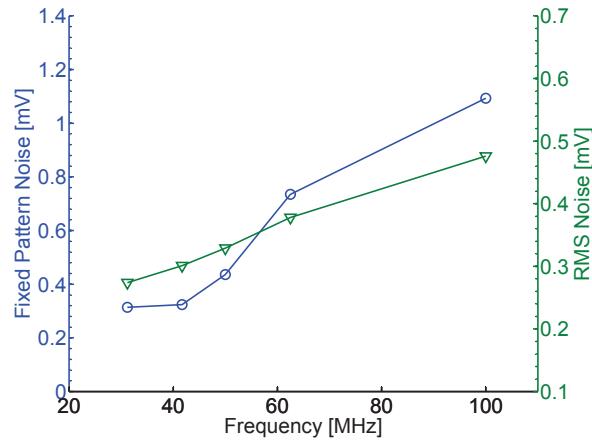

Figure 6.7: *Average FPN and rms TN of the SAR ADCs measured at the clock frequency of 100 MHz, 62.5 MHz, 50 MHz, 41.7 MHz and 31.2 MHz.*

6.2.2 Linearity measurement

In our design, the dynamic errors of ADCs are described by the temporal noise. Meanwhile, the static errors can be obtained by differential nonlinearity (DNL) and integral nonlinearity (INL). The histogram (code density) test with a linear ramp input is universally accepted and ideally suited for the measurement of ADCs [2]. The test is driven by a linear ramp input with a sufficient slow slope to assure no ac-related errors affecting the output. A large number of results are collected, and the number of occurrences for each code are tallied. In an ADC with no DNL and INL errors, the probabilities of occurrence for all codes are same. Hence, the same number of events is presented in each code bin. In a real ADC, the non-linear ADC response results in a dispersion of the number of events in each bin. The DNL of a particle code n, can be calculated by

$$DNL(n) = \frac{H_{actual}(n)}{H_{ideal}(n)} - 1 \,, \tag{6.1}$$

where $H_{actual}(n)$ is the number of measured events in the bin corresponding to code n, and $H_{ideal}(n)$ represents the number of events of code n with an ideal ADC featuring no linear error.
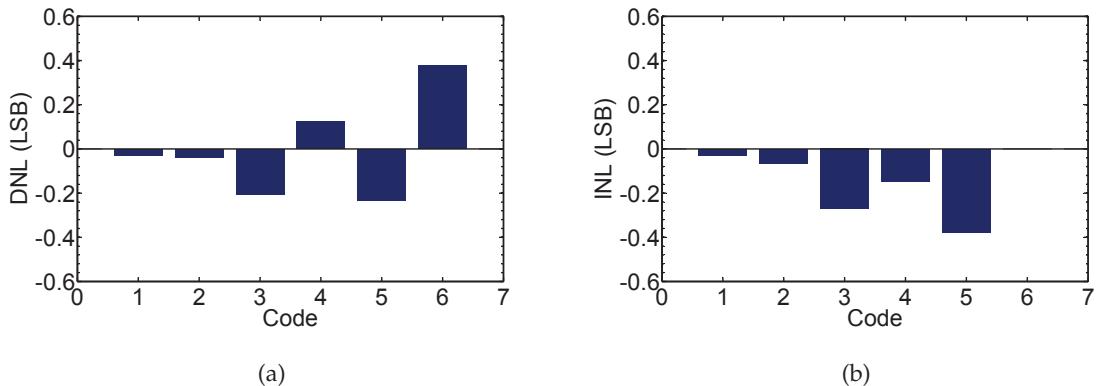
Figure 6.8: *Average value of (a) DNL and (b) INL, calculated over the 256 SAR ADCs.*

To test the DNL and INL in our ADCs, the LSB is set to ~1 mV by regulating the references. Then a linear sweep of the input voltage is performed. For each input voltage, up to 800 events are collected to eliminate the effect of the temporal noise. One can obtain the DNL by categorizing the output codes for 8 bins. The INL can be achieved by accumulating the DNL. Figure 6.8 gives the average DNL and INL of all the 256 ADCs. The response of ADCs is monotonic, and no code loss exhibited. In order to further study the spatial distribution of the DNL and INL for each pixel, the associated maximum and minimum values are illustrated in Fig. 6.9.

(a)

(b)

(c)

(d)
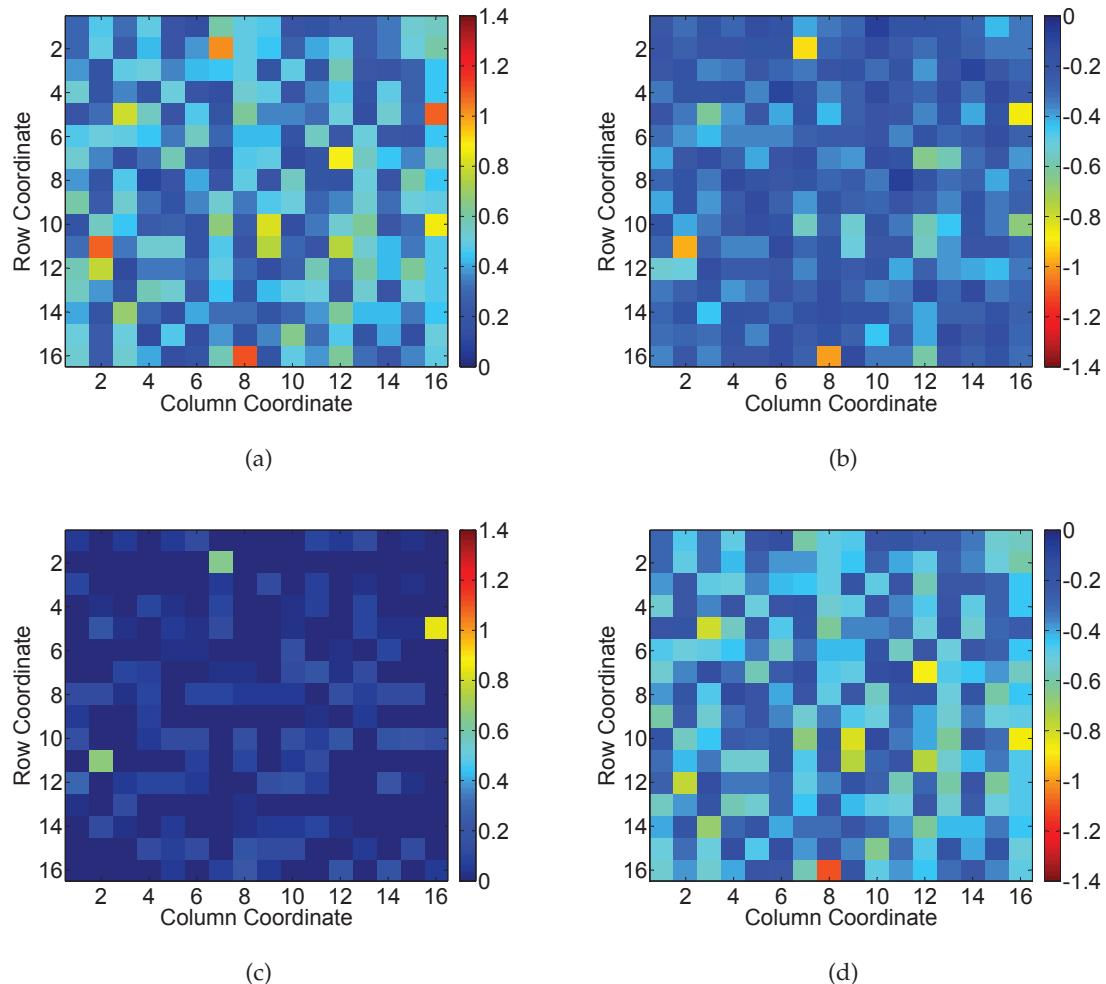
Figure 6.9: *Spatial distribution of the measured DNL and INL peak values in MIMADC-SAR matrix. (a) and (b) are the maximum and minimum values of DNL. (c) and (d) are the maximum and minimum values of INL. The unit of the colorbar is mV.*

6.2.3 Power consumption measurement

Power consumption is crucial for the outer layers of ILD-VTX. In MIMADC, the power is mainly consumed by the analog and digital parts in matrix, the on-chip ramp generator and buffer, as well as the I/O pads. The analog part is comprised of a sensing element, a S/H amplifier, and a pre-amplifier in the comparator. The digital part includes a latch, a memory, a SAR logic (for SAR ADC), a counter (for SS ADC) and peripheral control circuits. The power dissipated by each part is depicted in Fig. 6.10(a) for various clock frequencies. We can notice that the analog part consumes almost constant power with different frequencies. The contribution of the digital part strongly depends on the operational frequency. Based on the simulation, the latch is the dominant power source in the digital part. Summing up the power of the analog and the digital parts, and then dividing it with the number of power-on pixels, one can calculate the power consumption of a single pixel, as shown in Fig. 6.10(b). The power consumed by an individual pixel is ~200 µW at 100 MHz, in which the dynamic power due to the digital part exceeds our estimation.

(a)   (b)
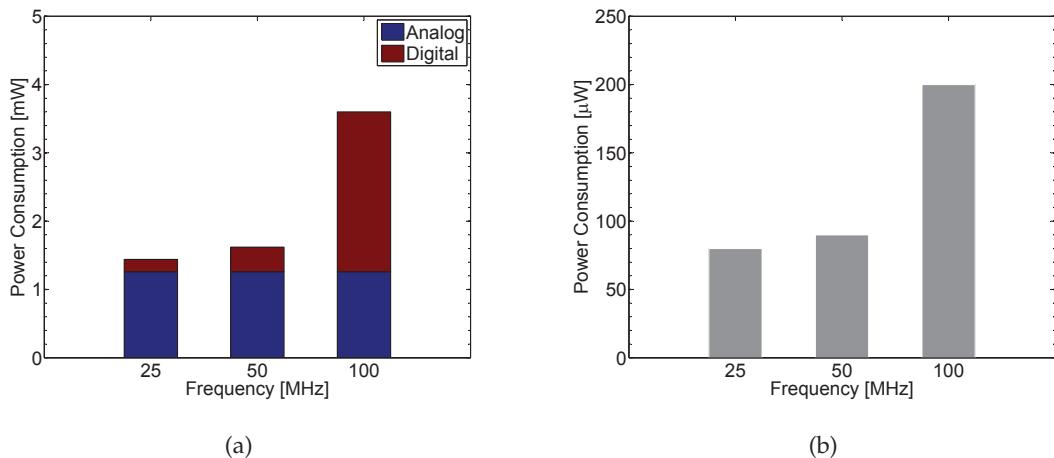
Figure 6.10: *Power consumption of the MIMADC-SAR matrix. (a) Power consumed by the whole matrix, (b) Power of an individual pixel.*

6.3 Test results of SS-ADC matrix with column memories

With respect to the SS ADCs, the performance strongly relies on the ramp reference. Its errors in linearity and noise are directly translated to the errors in ADCs. In MIMADC, two ramp generator circuits are integrated, one for the matrix and the other is connected to an analog output which can be monitored by an external instrument. Figure 6.11 shows the screenshots of the ramp output captured by the oscilloscope at the frequency of 100 MHz and 50 MHz. It indicates that the rise time of the ramp can be controlled by the power-on time of the "RG_rst" signal. The test has also validated that the bottom and peak value can be set

by the external voltages. The ramp can be swung in the range of 0.2–1.6 V, which is sufficient for the ADC's operation. Meanwhile, this results also demonstrates that the buffer following the ramp generator works well. However, comparing Fig. 6.11(a) with 6.11(b), one can observe that the falling edge in the case of 100 MHz is slow, thus the ramp signal can not reset to the baseline at the power-off of "RG_rst". The reason may be the limitation of the swing rate of the buffer or the integrator in the ramp generator. Although the speed of the ramp generator is slight slower than expected, the ramp signal still remains a good linearity in the several clock cycles after the rise edge of "RG_rst".


(a)   (b)
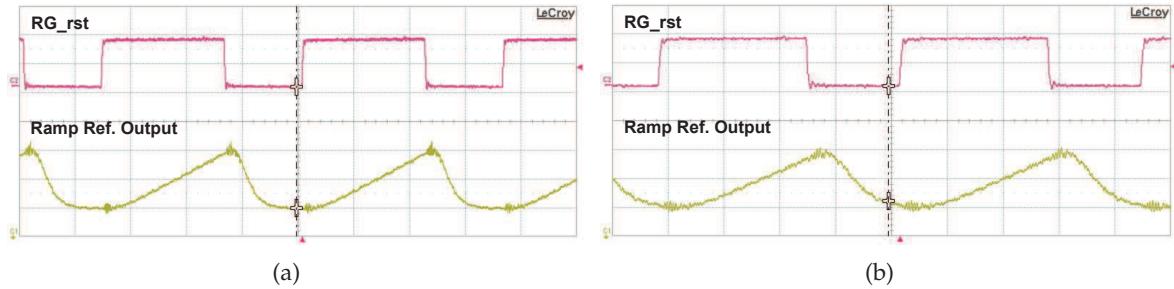
Figure 6.11: *Measured ramp reference at the clock frequency of (a) 50 MHz and (b) 100 MHz.*

6.3.1 Noise performance

Figure 6.12 depicts the responses of 288 pixel-level SS ADCs in the MIMADC-SS1 matrix. They are measured by sweeping the input signal near the first transition position at the clock frequency of 100 MHz. Fitting the curves with error functions, one can compute the distributions of the temporal noise and the transition position.
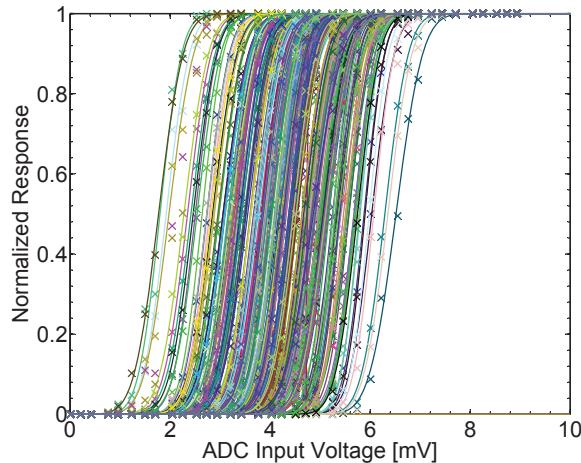
Figure 6.12: *Response of the 288 SS ADCs in the MIMADC-SS1 matrix. The average of 400 events have been calculated for each input voltage. The cross symbols represent the measured data, and the solid curve is the fitting result by an error function.*

(a)   (b)
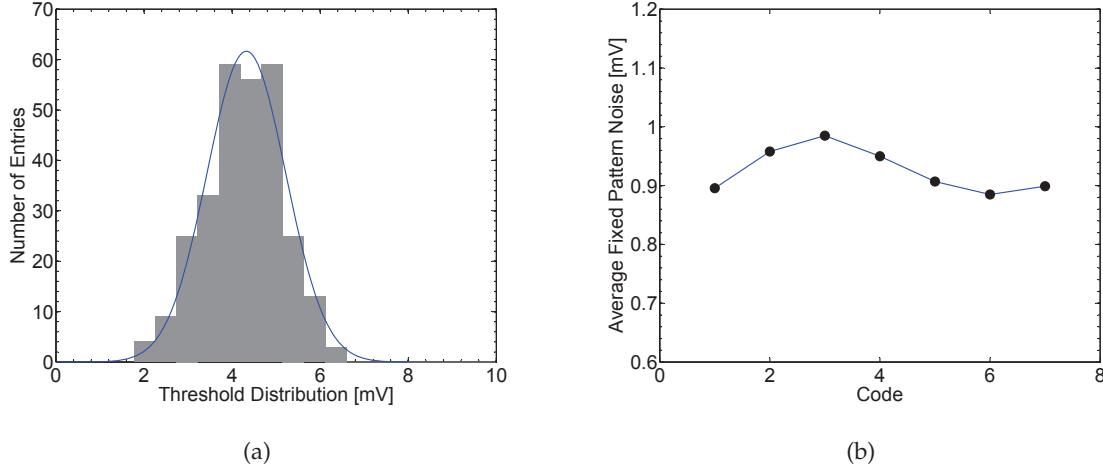
Figure 6.13: *Distribution of the fixed pattern noise (FPN) of 288 SS ADCs in the MIMADC-SS1 matrix. (a) Histogram of the FPN as well as the fitting result by a Gaussian function. The standard deviation, i.e. average FPN, is 0.896 mV. (b) Average FPN measured at each transition step.*

Figure 6.13(a) shows the histogram of the offset distribution for all ADCs in the MIMADC-SS1 matrix. As a Gaussian distribution, its standard deviation, i.e. FPN, is ∼0.896 mV. The FPN values at each code are calculated as shown in Fig. 6.13(b). In contrast to the case in the MIMADC-SAR, the values of FPN at various codes have less difference and are always below 1 mV at all codes. This may be explained by the fact that much less transmission lines are used in SS-ADCs matrices: a single ramp signal in the MIMADC-SS1 and MIMADC-SS2 rather than seven reference voltages in the MIMASDC-SAR. The simplified layout reduces the possibility of crosstalk.

The distribution of the temporal noise is given in Fig. 6.14(a). The rms temporal noise is ∼0.37 mV. The spatial distribution of the rms noise in the matrix is provided in Fig. 6.14(b).

The FPN and temporal noise in the MIMADC-SS1 matrix are also tested in various operational frequencies. As illustrated in Fig. 6.15, the FPN is always in the range of 0.85 mV to 1 mV, and has no obvious change with frequency. The temporal noise shows the same trend as the FPN. This results prove that the ADCs in this matrix suffer less crosstalk than in the case of MIMADC-SAR matrix.

6.3.2 Linearity measurement

The average DNL calculated on all the 288 pixels is shown in Fig.6.16(a). A good DNL, less than 0.1 LSB is achieved at the code of 2–6. But a much larger value exists in the first code, which is due to the nonlinearity of the ramp generator. In the single-slope type ADC, the linearity greatly depends on the performance of the ramp reference. The linearity error in this reference is directly translated into a DNL error of the ADC. In practice, the ramp reference cannot remain an excellent linearity over the full-scale of input. An actual ramp

(a)   (b)
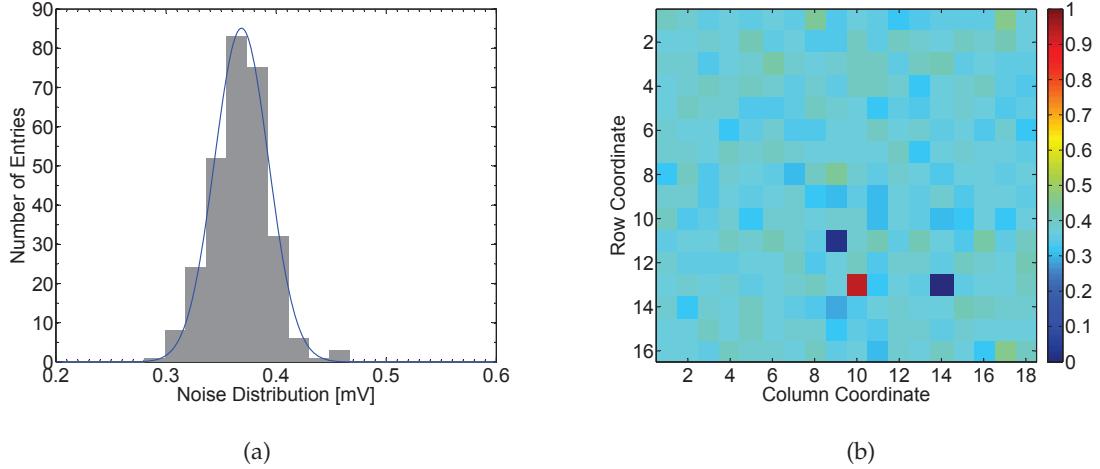
Figure 6.14: *Distribution of the temporal noise (TN) of the 256 SS ADCs in the MIMADC-SS1 matrix. (a) Histogram of the TN as well as the fitting result by a Gaussian function. The mean value is 0.368 mV, and standard deviation is 0.034 mV. The mean value is the average rms noise of all ADCs. (b) Spatial distribution of the TN within the whole matrix. The color-bar is in an unit of mV.*
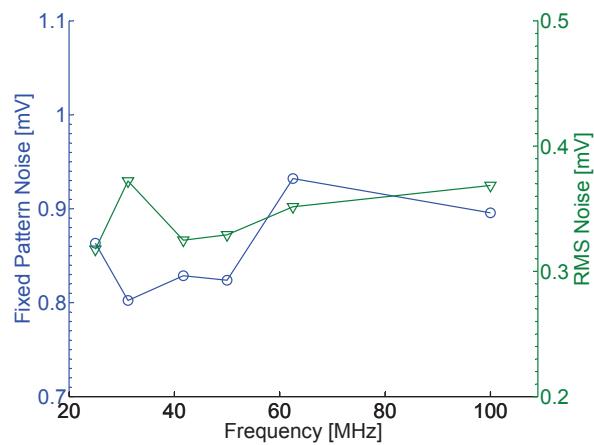
Figure 6.15: *Average FPN and rms TN of the SS ADCs in the MIMADC-SS1 matrix measured at the clock frequency of 100 MHz, 62.5 MHz, 50 MHz, 41.7 MHz and 31.2 MHz.*
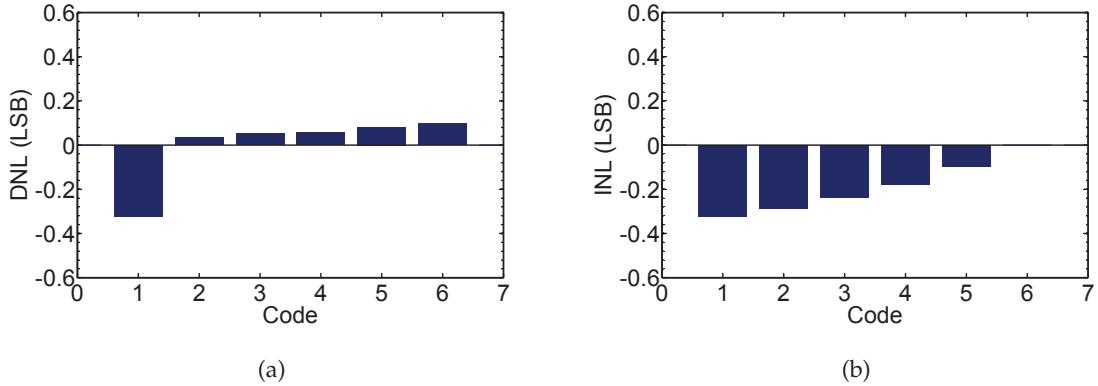
Figure 6.16: Average of (a) DNL and (b) INL, calculated over the 288 SS ADCs in MIMADC-SS1.

signal is illustrated in Fig. 6.17(a). At the beginning of conversion, the control signal "RG_rst" (cf. Fig. 6.11) initiates the ramp reference to rise. Because of the bandwidth limitation of the ramp generator, this voltage can not rise instantly, and therefore, a reduced slope appears at the beginning, leading to a lower ramp reference than expected. For a given number of ADC inputs, less events trigger the latch to save the first code "001", translating into a larger DNL, as shown in Fig. 6.16(a). A measured ramp signal at a clock frequency of 100 MHz is presented in Fig. 6.17(b). One can observe an obvious slow rising at the beginning of the ramp. One of the possible method to solve this problem is to shift the initialization of "RG_rst" to an earlier clock cycle, resulting in a sufficient set-up time for the ramp to reach the normal state. Consequently, as soon as the start of the comparison, the ramp reference achieve a good linearity. This approach is effective for low clock frequencies. But for the desired clock of 100 MHz, less time is reserved for the ramp generator to recover to the baseline level. Hence, a ramp generator with a large bandwidth and a fast reset is required.

The peak values of the DNL and INL of each pixel in the MIMADC-SS1 are shown in Fig. 6.18. Uniform distributions of the max/min value are obtained for the DNL and INL. We observe that the maximum value of INL is zero at the last ADC code, since the end-point fitting is used for calculating the INL.

6.3.3 Power consumption measurement

The power consumption of each part in the MIMADC-SS1 matrix is drawn in Fig. 6.19(a). Most of the power is consumed by the two on-chip ramp generators with ∼2 mW for each one. In a full-scale chip, this power will be averaged by all pixels. For each pixel, the power contributed by the ramp generator can be ignored. The digital power is greatly reduced with frequency, while the analog power remains constant. The pixel power consumption that only taking into account of the digital and the analog part is illustrated in Fig. 6.19(b). Less than 200 μW/pixel is achieved. The measured result is larger than the simulation result because the
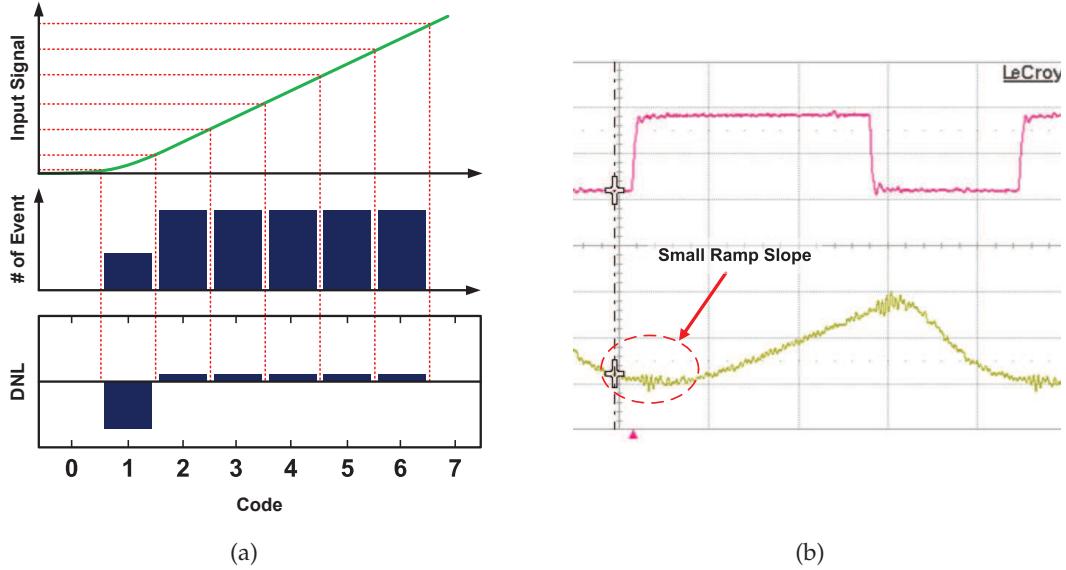
Figure 6.17: *Influence of the nonlinearity of ramp signal on DNL of ADCs. (a) Principle of the DNL error introduced by the nonlinearity of ramp single at the first code. (b) Measured ramp signal in the MIMADC-SS1 at 100 MHz clock frequency.*

digital power exceeds the estimation. The dynamic power of the latch may be the dominant reason. This problem has not been found during the post-simulation because of the incomplete extraction of parasitic components from the layout. This issue can be corrected in the future design.

6.4 Test results of SS-ADC matrix with in-pixel memories

6.4.1 Noise performance

Similar tests as for the previous two matrices are performed for the MIMADC-SS2 matrix. Figure 6.20 shows the transfer function curves obtained on the 288 SS ADCs of the MIMADC-SS2. The distribution of extracted threshold is depicted in Fig. 6.21(a). The extracted FPN for the first ADC code is ∼0.70 mV. No significant change of the FPN at different ADC transition steps, as shown in Fig. 6.21(b).

The statistical result of the rms temporal noise is plotted in Fig. 6.22(a). The measured average rms temporal noise of all the 288 pixels is ∼0.32 mV. The spatial distribution of the noise is presented in Fig. 6.22(b). A random distribution can be observed, and no special pattern exists.

Both of the FPN and TN are measured at various clock frequencies (Fig. 6.23), and have no obvious variation. It indicates that the crosstalk does not affect the noise performance.
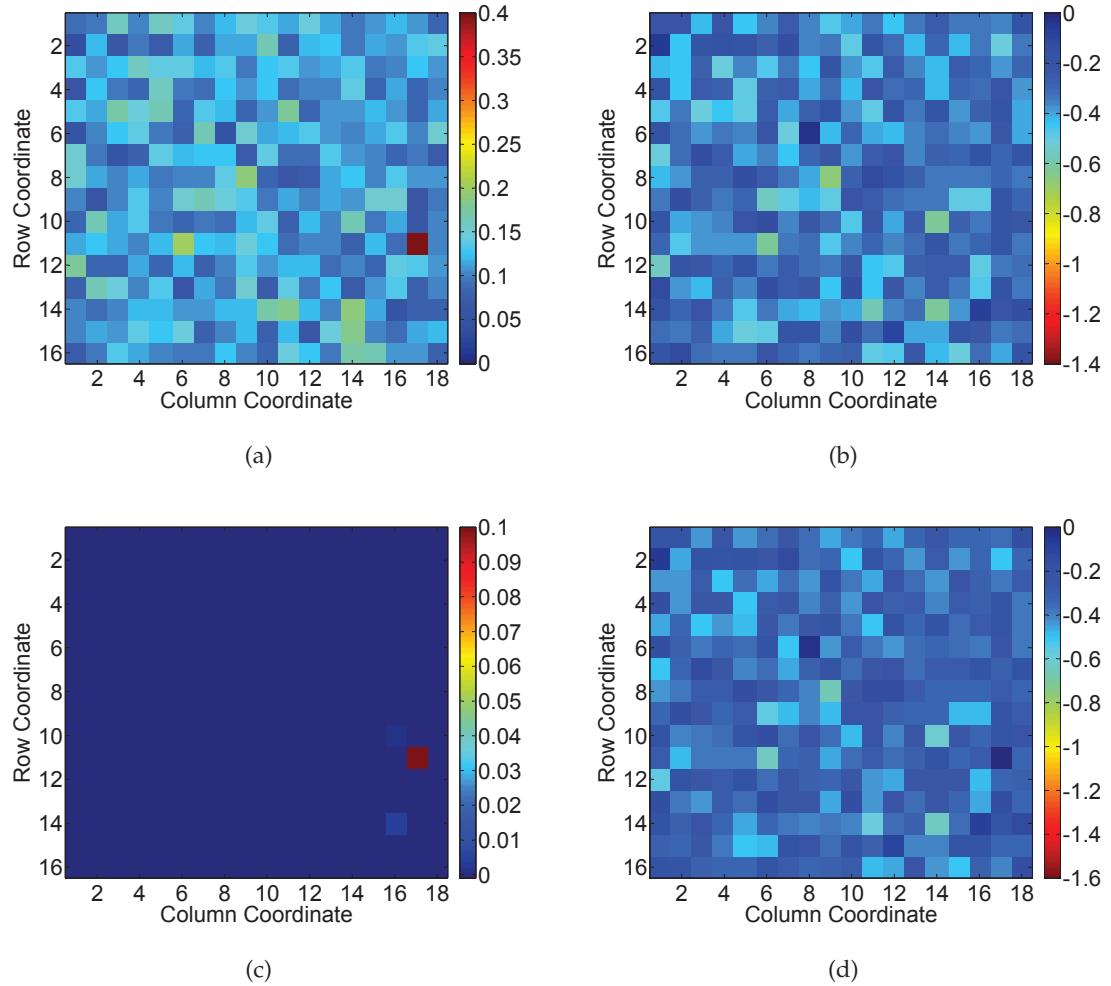
Figure 6.18: *Spatial distribution of the measured DNL and INL peak values in the MIMADC-SS1 matrix. (a) and (b) are the maximum and minimum values of the DNL, respectively. (c) and (d) are the maximum and minimum values of the INL, respectively. The color-bar is in an unit of mV.*
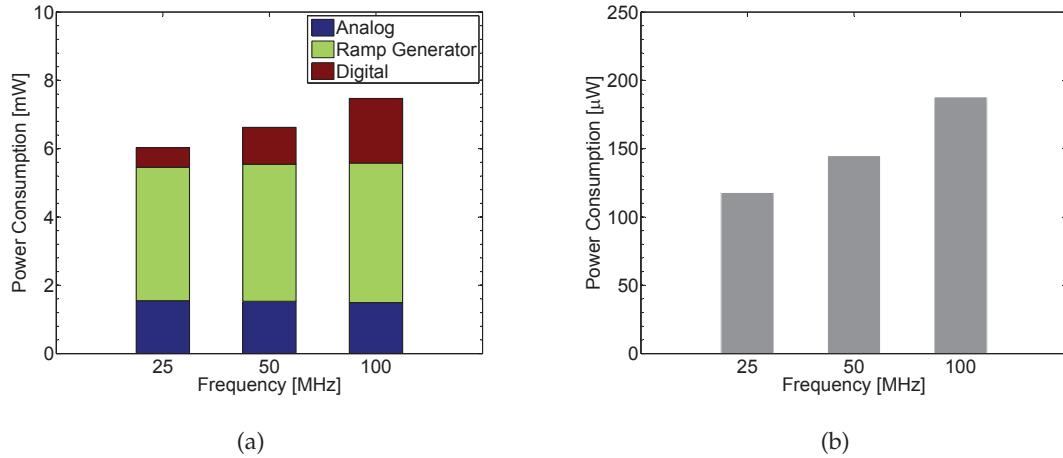
Figure 6.19: *Power consumption of the MIMADC-SS1 matrix. (a) Power consumed by the whole matrix, (b) Power consumption of an individual pixel.*
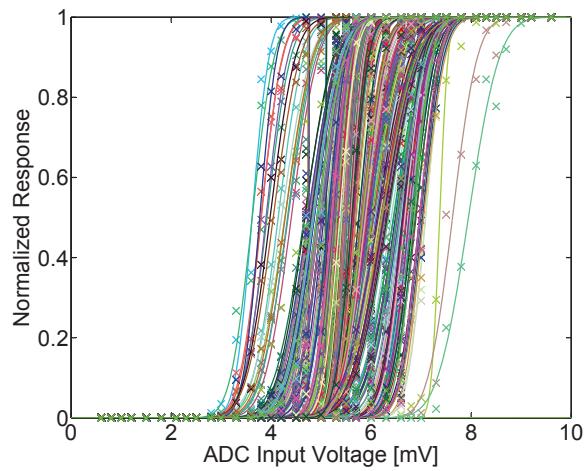
Figure 6.20: *Response of the 288 pixel-level SS ADCs in the MIMADC-SS2 matrix. The average value of 400 events has been calculated for each input voltage. The cross symbols are the data points recorded, and the solid curve is the fit result by an error function.*

(a)　　　　　　　　　　　　　　(b)
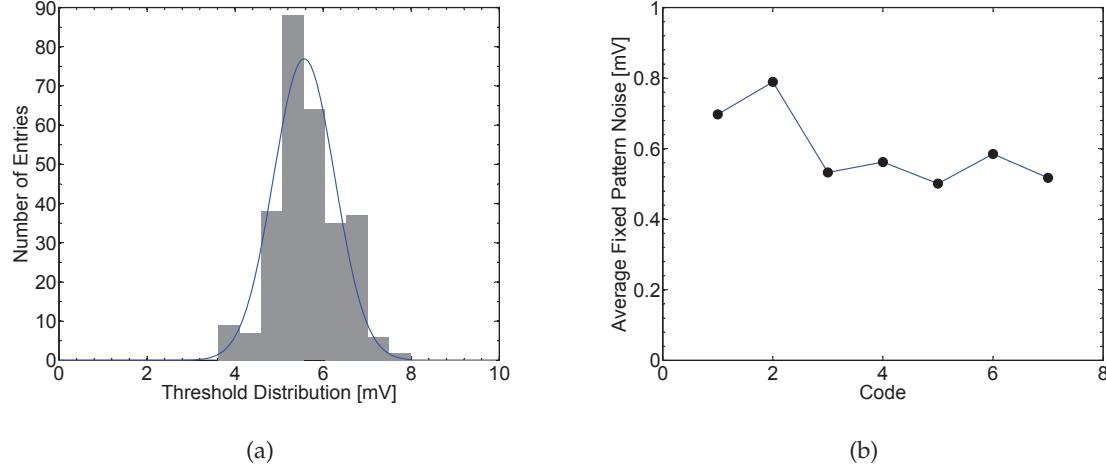
Figure 6.21: *Distribution of the fixed pattern noise (FPN) of the 288 pixel-level SS ADCs in the MIMADC-SS2. (a) Histogram of the FPN as well as the fitting result by a Gaussian function. The standard deviation, i.e. average FPN, is 0.697 mV. (b) Average FPN measured at each transition step.*


(a)　　　　　　　　　　　　　　(b)
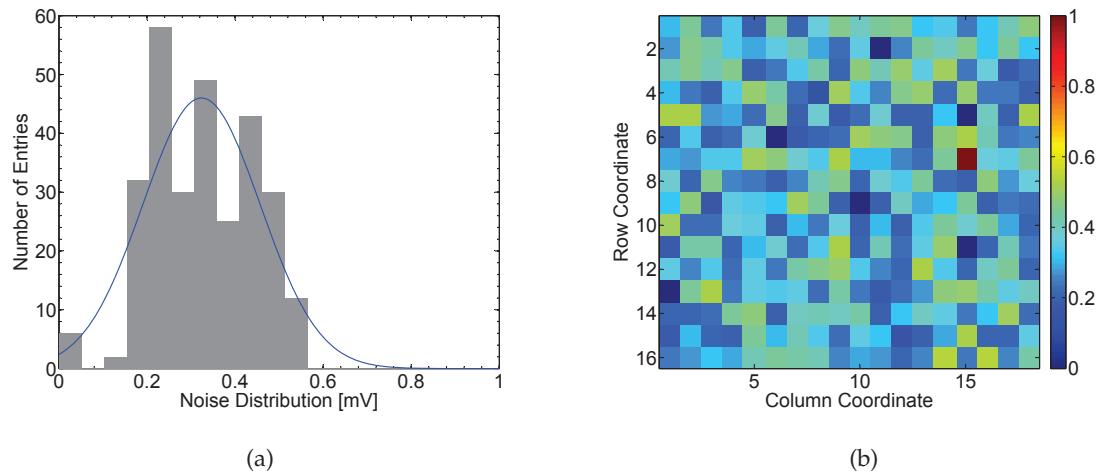
Figure 6.22: *The distribution of the temporal noise (TN) of the 256 pixel-level SS ADCs in the MIMADC-SS2 matrix. (a) Histogram of the TN as well as the fitting result by a Gaussian function. The mean value is 0.324 mV, and standard deviation is 0.188 mV. The color-bar is in an unit of mV.*
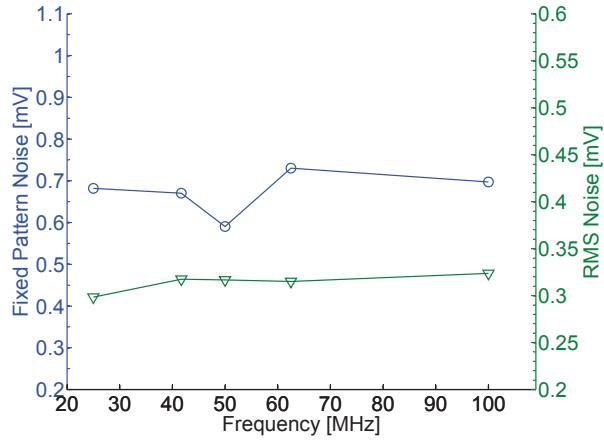
Figure 6.23: *Average FPN and rms TN of the SS ADCs in the MIMADC-SS2 matrix measured at the clock frequency of 100 MHz, 62.5 MHz, 50 MHz, 41.7 MHz and 31.2 MHz.*

6.4.2 Linearity measurement

The average values of the DNL and INL of all the ADCs in the MIMADC-SS2 are shown in Fig. 6.24. Due to the same reason as in the case of MIMADC-SS1, the DNL at the first code is larger than others. The linearity is degraded comparing to the previous SS ADCs. As stated in Chapter 4.3.2.2, the linearity of cascaded CS amplifier is poorer than closed-loop amplifier. The max/min values of the DNL and INL are shown in Fig. 6.25.

(a)   (b)
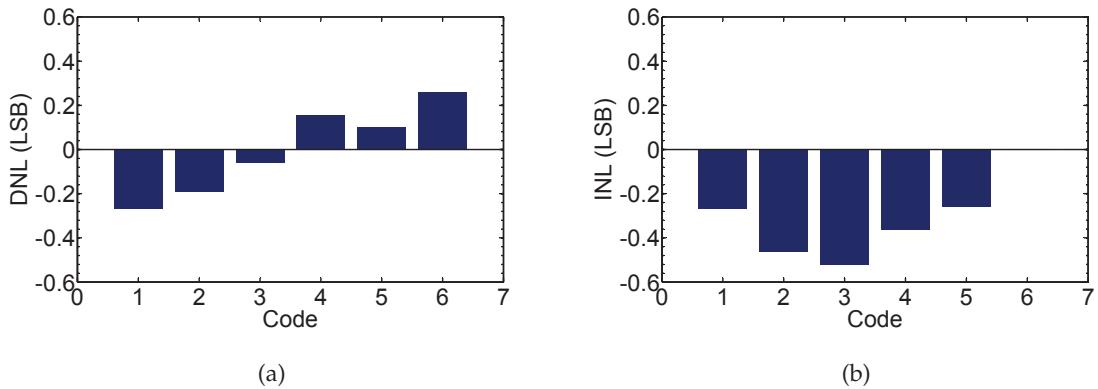
Figure 6.24: *Measured average values of the (a) DNL and (b) INL, over the 288 SS ADCs in the MIMADC-SS2 matrix.*

6.4.3 Power consumption measurement

The power of the whole matrix as well as of individual pixel is illustrated in Fig. 6.26. The power consumption is similar to the previous matrices.
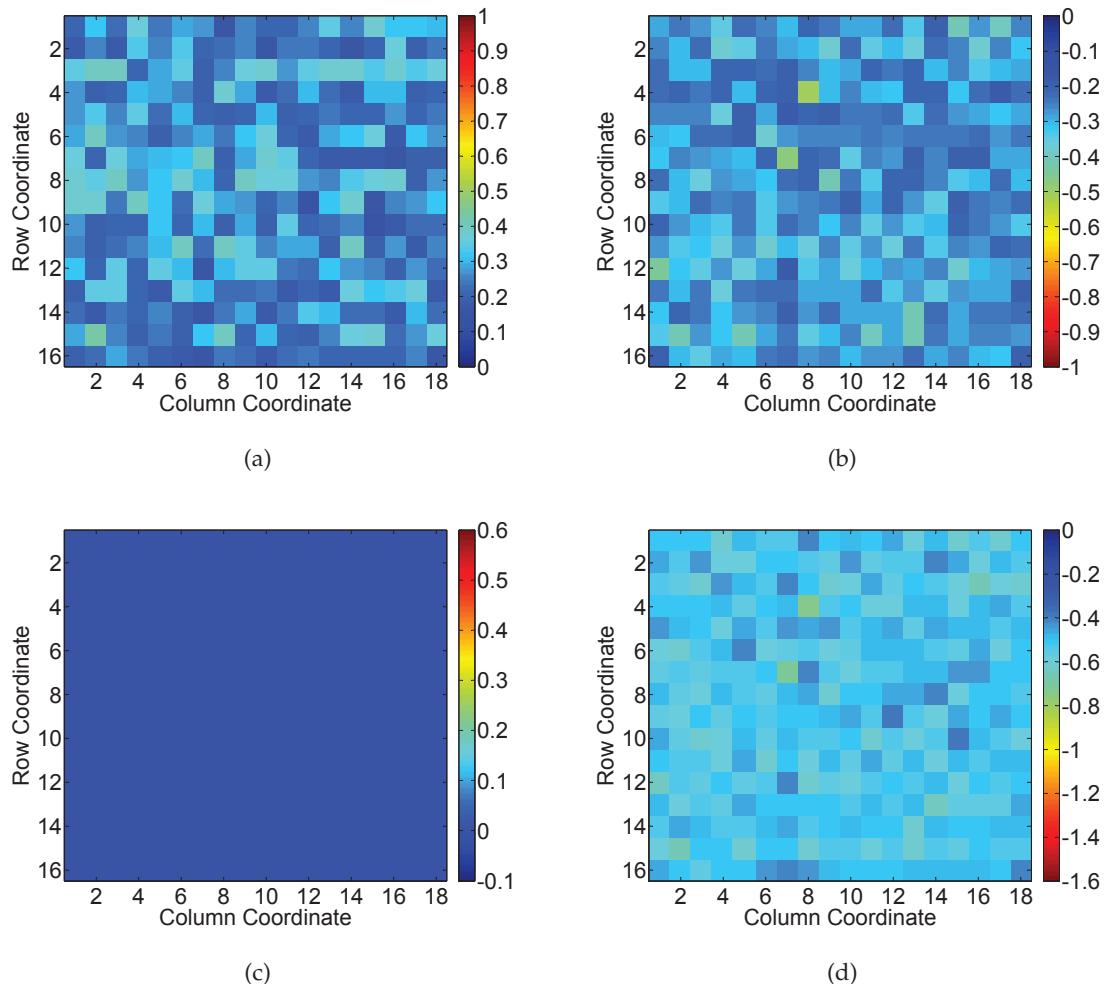
Figure 6.25: *Spatial distributions of the measured DNL and INL peak values in the MIMADC-SS2 matrix. (a) and (b) are the maximum and minimum values of the DNL, respectively. (c) and (d) are the maximum and minimum values of the INL, respectively. The unit of the color-bar is mV.*

(a)   (b)
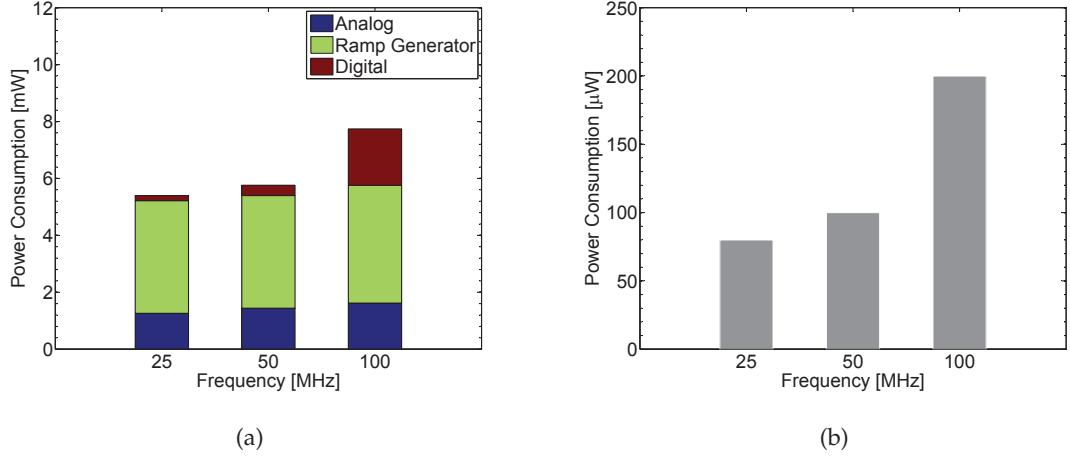
**Figure 6.26:** *Power consumption of the MIMADC-SS2 matrix. (a) Power consumed by the whole matrix, (b) Power consumption of an individual pixel.*

6.5 Conclusion

In this chapter, the electrical tests are performed for the three matrices fabricated in the MIMADC prototype. Considering the application of the pixel-level ADC for the CPS on vertex detector, the tests focus on the temporal noise, FPN and the static performance including the DNL and INL. The test results have validated the concept of integrating an independent ADC within an area-limited pixel. The high sampling rate can meet the requirements of the ILD-VTX outer layers. Moreover, the power consumption achieves the design specification benefiting from both the advanced process and the reasonable circuit architectures.

The performances of the three types ADCs are summarized in Table 6.1. The preliminary results indicate that all of them can meet the requirements of the outer layers. The sampling rate of the SAR-ADCs is slightly higher than the single-slope ones, however, the latter type has the potentiality for enhancing the conversion speed thanks to its relaxed timing control. Compared with the SAR-ADCs, the single-slope ADCs have simpler structure and layout, leading to less crosstalk and thus smaller temporal noise and FPN. The measurements imply that the inter-pixel crosstalk is the main constraint on the performance of the pixel-level ADC. Therefore, optimizing the pixel layout and minimizing the crosstalk are the major tasks in the further development. All the three type in-pixel ADCs have a power consumption of around 200 μW. Although this measured result is larger than the simulation, the power consumption of 200 μW/ADC can still meet the requirement of the outer layer (< 500 μW/ADC). It is reasonable to expect that the power consumption can be reduced further by correcting the design.

In group of PICSEL/IPHC, several designs have been proposed to realize the multi-bit quantization of CPS for the ILD vertex detector. But all the previous architectures are imple-

Item	SAR	SS-1	SS-2
Process	Tower 0.18 µm CIS		
Sampling Rate	6.25 MS/s	5.55 MS/s	
Conversion Time	160 ns	180 ns	
Worst Average DNL	0.38 LSB	0.32 LSB	0.27 LSB
Worst Average INL	0.38 LSB	0.32 LSB	0.46 LSB
Temporal Noise (rms)	0.48 mV	0.37 mV	0.32 mV
Column FPN (rms)	1.10 mV	0.90 mV	0.70 mV
Active Area	35×35 µm^2		
Power Consumption	200 µW	188 µW	200 µW

Table 6.1: Performance summary of the MIMADC prototype

mented in column-level. A comparison of our chip with them is concluded in Table 6.2. It is obvious that the pixel-level ADCs architecture exhibits significant merits in terms of power consumption and active area. The pipeline ADCs in [3] and [4] provide a twice high sampling rate but at the expense of power dissipation. The single-slope ADC in [5] has much slower speed and larger LSB than the single-slope ADCs in this work. The ADCs in [6] achieve comparable performance with our designs. The former employs a non-linear quantization mode, resulting in a maximum 4-bit resolution with the same number of quantization levels of 8 as for the SAR ADCs in this work. Our SAR ADCs perform a linear quantization relying on the external references, and therefore, it is easy to change to the non-linear quantization. Compared with [6], the big advantage of our SAR ADCs is that the analog signal is propagated over a short distance, reducing the crosstalk along the column bus and the capacitive load on the line drivers. We conclude that the CPS with pixel-level ADCs can offer promising performance for the outer layers of the ILD VTX.

Specifications	[3]	[4]	[5]	[7]	[6]	MIMADC-SAR	MIMADC-SS1	MIMADC-SS2
Architecture	Pipeline in-column	Pipeline in-column	Ramp in-column	SAR in-column	SAR in-column	SAR in-pixel	Ramp in-pixel	Ramp in-pixel
Technology (µm)	0.35	0.35	0.35	0.35	0.35	0.18	0.18	0.18
Supply Voltage (V)	3.3/2.5	2.95(analog) 2(digital)	3.3	3.3	3	1.8	1.8	1.8
Sampling Rate (MS/s)	12.5	12.5	1	9	6.25	6.25	5.55	5.55
Resolution (bit)	5	5	4	4/3/2	4/3/2	3	3	3
LSB (mV)	1	1	7.8	15	1	1	1	1
Active Power (mW)	0.85/0.644	1.71	0.744	0.27 (static)	0.714	0.20	0.19	0.20
Inactive Power (mW)	–	–	–	–	0.486	–	–	–
Active Area (µm^2)	21.5×1430	20×1400	25×900	25×1275	35×545	35×35	35×35	35×35

Table 6.2: Comparison of the column-level ADCs and with the pixel-level ADCs in this work.

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Conclusions and perspectives

General conclusions

As one of the two detectors installed in the next generation large linear accelerator — ILC, the ILD is demanding in unprecedented precision of tracking. The ILD vertex detector, targeting on the reconstruction of decay vertices of short lived particles, motivates the development of very granular and thin pixel sensors. CMOS pixel sensors, proposed and extensively studied by the PICSEL group in IPHC, is a promising technology employed in particle tracking. Their outstanding performances have been demonstrated by a number of MIMOSA prototypes. One scheme based on the CPS technique and the double-sided ladder concept have been conceived to match the requirements of the ILD vertex detector. The proposed layout of the vertex detector features a 3-layer, concentric barrel geometry. Driven by the hit rate and the surface area in terms of different layers, dedicated sensors are needed to be optimized for the trade-offs between spatial resolution, readout speed, and power consumption. In contrast to the sensors on the innermost layer, those on the outer layers are prior to the power efficiency to be compatible with the low-mass cooling system such as air flow. A spatial resolution better than $\sim$4 µm combining with a readout time of $\sim$100 µs are expected to be sufficient for the outer layers of the vertex detector operated at a 500 GeV collision energy.

This thesis concerns the design of ADCs embedded in CMOS pixel sensors adapted to the outer layers of the ILD vertex detector. The CPS equipped with on-chip ADCs permits a large pixel size aiming for low power consumption, while no loss of spatial resolution. Several prototypes dedicated to the outer layers of the ILD vertex detector have been fabricated, where various ADC technologies were exploited. A latest prototype, called MIMOSA-31, constitutes a 48×64 pixel matrix with column-level SAR ADCs to match the specifications indicated above. The FPN of the column-ended ADCs is quite small, i.e. 0.40 mV, thanks to the large available peripheral area at the end of columns. However, the analog outputs of pixels are sensitive to the noise along the column bus, resulting in a large temporal noise ($\sim$1 mV). In addition, a large area occupied by the ADCs (> 500 µm in column direction) contributes more insensitive zone for the sensor.

To minimize power consumption and insensitive area, we proposed a concept of CPS integrated with pixel-level ADCs. Compared with column-level ADCs, pixel-level ones generally

demonstrate the following advantages. First, the pixel output signals are exclusively in digital format, preventing the crosstalk during the pixel readout. In a typical CPS, the analog pixel output is sensitive to the noise coupling during the signal transmitted from pixel to peripheral circuits. The digital outputs from pixel-level ADCs have good noise tolerance, therefore it is reasonable to expect a better SNR. Second, a relaxation on driving ability in terms of matrix line is helpful to promote the power efficiency. Considering an analog readout pixel matrix with a large scale, strong buffers are demanded to drive the heavy capacitive load on the matrix lines, leading to a large power dissipation. In the sensor integrated with pixel-level ADCs, only the energy-saving digital buffers are necessary, favoured by the low-power applications. Additionally, the in-pixel integration is advantageous to the reduction of insensitive area. The above features can be achieved at the expense of great challenges during the circuit design. To implement an ADC combining with the sensing element within a limited pixel area asks for a comprehensive study of each building block. A reasonable architecture, a robust circuit, together with an ingenious layout are essential, allowing the pixel circuits to be operated under a targeted speed and meantime to suffer less crosstalk.

Driven by the specifications of the outer layers of the ILD vertex detector, a prototype, called MIMADC, is developed to exploit the feasibility of the pixel-level ADCs utilized in CPS. The previous studies show that a pixel size of 35×35 μm^2 coupled with a 3-bit quantization is capable to reach the spatial resolution of 3–4 μm which is adequate for the ILD baseline requirement. Considering the balance between the power consumption and the readout speed, the row-by-row rolling shutter mode is employed. To well reconstruct the position of the traversing particles, a small LSB ($\sim$1 mV) calculated from the noise floor of the sensing element is set initially.

Aiming to extensively study the potential architectures that can be used to implement the pixel-level ADCs, three matrices featuring a variety of ADC architectures are designed in this prototype: one matrix, called MIMADC-SAR, is integrated with SAR ADCs; the others with single-slope ADCs are called MIMADC-SS1 and -SS2 respectively. Conceptually, SAR and single-slope ADCs are attractive for the in-pixel integration, thanks to the simpleness in architecture and the potential in low power consumption.

The SAR ADC is generally considered as a relatively fast architecture, but the large area required by the DAC and the SAR logic circuit prevent it from the very granular sensor. To reach a more compact architecture, we optimize the design of the DAC. The conventional charge-redistributed DAC can be replaced by a modified one, which includes a group of voltage references and a multiplexer. The operation of this DAC relies on the behavior that the input digital codes drive the multiplexer to select one of the references as the corresponding analog output. Since these references can be shared by all pixels, only a multiplexer is demanded in the pixel, which can be easily implemented by several MOS switches. With respect to the SAR logic circuits, they are placed at the ended of column and shared by the associated pixels. Although the column-ended circuits exist, the merit provided by pixel-level

ADCs, i.e. all-digital pixel output, still remains. This architecture allows us to integrate SAR ADCs within a limited pixel size. To validate this SAR-ADC architecture, the pixel matrix MIMADC-SAR featuring 16×16 pixels has been implemented. A sampling rate of 6.25 MS/s is reached at a clock frequency of 100 MHz. The measurement results have well verified the proposed concept: the temporal noise is ∼0.48 mV; the FPN is ∼1 mV; both worst DNL and INL are less than 0.4 LSB.

Single-slope ADCs, well-known by its simplest architecture, is a suitable choice for pixel-level ADCs. The matrix MIMADC-SS1 inherits the architecture from MIMADC-SAR, while the column-ended logic circuits are replaced by the memories to record the ADC outputs. An adaptive ramp generator has been employed on chip. The generated ramp reference is adjustable and insensitive to process variation. The sampling rate is ∼5.6 MS/s, which is slightly slower than the SAR ADCs. The measured temporal noise and FPN are ∼0.37 mV and 0.9 mV respectively. The DNL and INL are no more than ∼0.32 LSB. In MIMADC-SS2, the S/H amplifier has been re-designed with a cascaded open-loop architecture. Benefiting from the fact that less capacitor is required in the S/H amplifier, more pixel area allows us to carry out in-pixel memories. The measurement results show that the temporal noise is ∼0.32 mV and the FPN is 0.7 mV. The linearity is better than 0.5 LSB.

According to the specifications of the ILD vertex detector outer layers, a power consumption of 500 µW for each pixel is allowable. Because of the low power supply together with the reasonable design, the power consumption of pixels in the three matrices is less than 200 µW, much less than that of MIMOSA-31 and the requirement as well.

The prototype MIMADC, dedicated for the sensors equipping the outer layers of the ILD vertex detector, has demonstrated the feasibility of developing CMOS pixel sensors with pixel-level ADCs. Both of the SAR and the single-slope types ADCs have been confirmed to be suitable for the in-pixel integration. A large scale sensor with in-pixel ADCs optimized in terms of noise, cross talk and read-out speed is foreseen to match the full requirements of the outer layers.

Perspectives

This work has studied three architectures of in-pixel ADCs, adapted to the CMOS pixel sensors for the outer layers of the ILD vertex detector. The first prototype fabricated in a 0.18 µm CMOS image sensor process has validated that all the three architectures show promising results on the balance between the noise performance, the conversion time, and the power consumption. According to the test results of MIMADC, several improvements are expected in the next prototype.

A complete measurement for both the sensing elements and the ADCs is necessary to evaluate the performances on the multi-bit quantization for the incident particles. In addition,

the scale of the matrices in MIMADC is limited, which hides some problems only shown up in a large-scale sensor. The issue on the delay of the control signals for various pixels deserves an attention as well. The sensor with pixel-level ADCs requires a complicated timing control. The latency on timing control will result in the performance error, and even the faults during the pixel operation. To ensure an acceptable latency within the whole matrix is a great challenge.

With respect to the ADC design, some improvements can be carried out with a guide of testing results. An optimization of the layout is a primary task. In MIMADC, the interference of the different blocks degrades the FPN and temporal noise. Moreover, reducing the number of control signals is beneficial to reduce such noise. Since the speed of the on-chip ramp generator is not sufficient for high-speed operation, an improved design featuring a large bandwidth is preferred for promoting the linearity of the ADCs.

Furthermore, the sensor integrated with the pixel-level ADCs can be easily migrated to the 3D integration technology. The sensing element and the ADC can be separated to the different tiers. An improvement of both noise and FPN is foreseeable in the 3D process. Meanwhile, this approach can also resolve the issues on the crosstalk and signal coupling. Even in standard CMOS fabrication processes, migrating the process from the present 0.18 μm to a smaller feature size can provide a higher circuit density, as well as a reduction of power consumption.

A

Schematics of the test boards for MIMADC chip
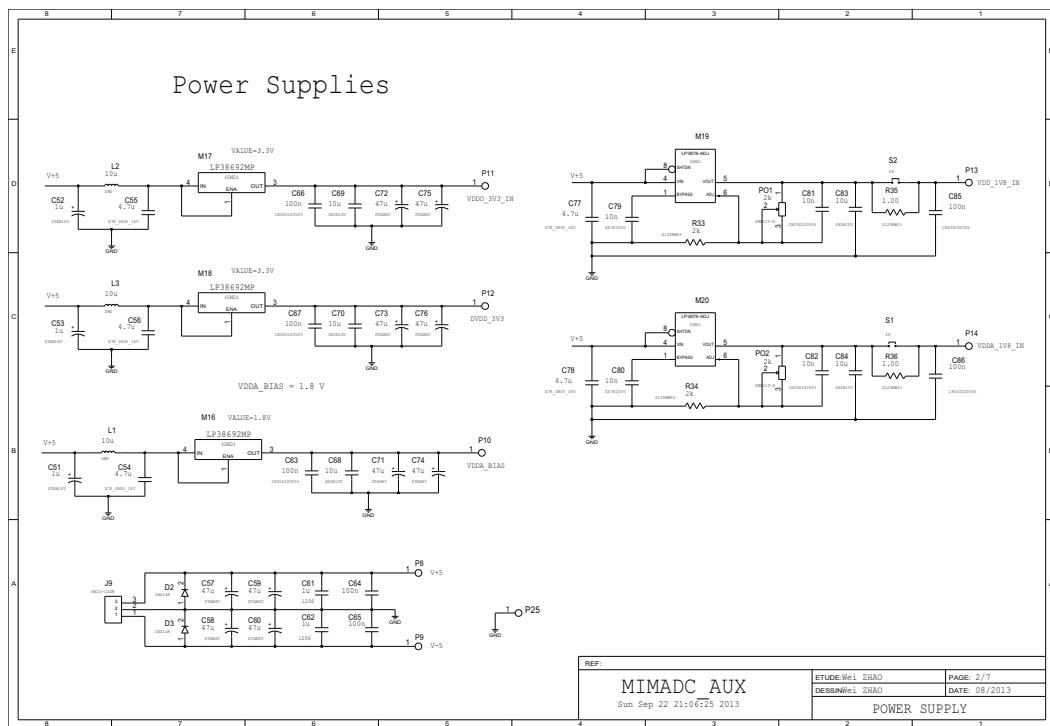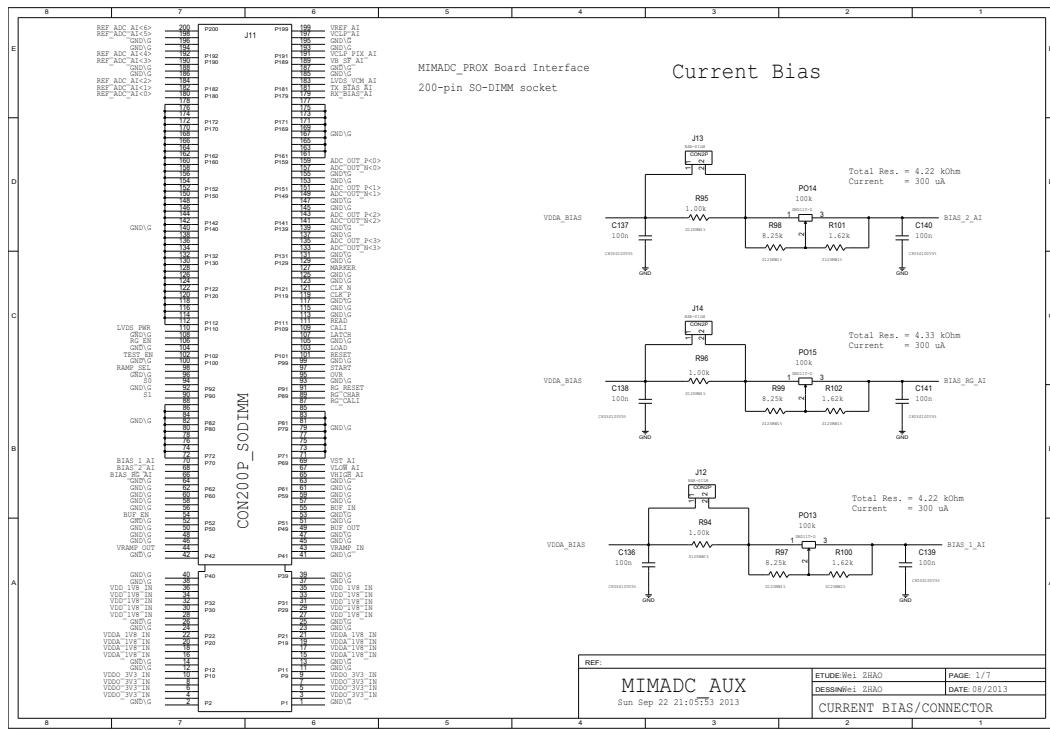
Figure A.1: *First and second page of the schematic of the MIMADC auxiliary test board.*
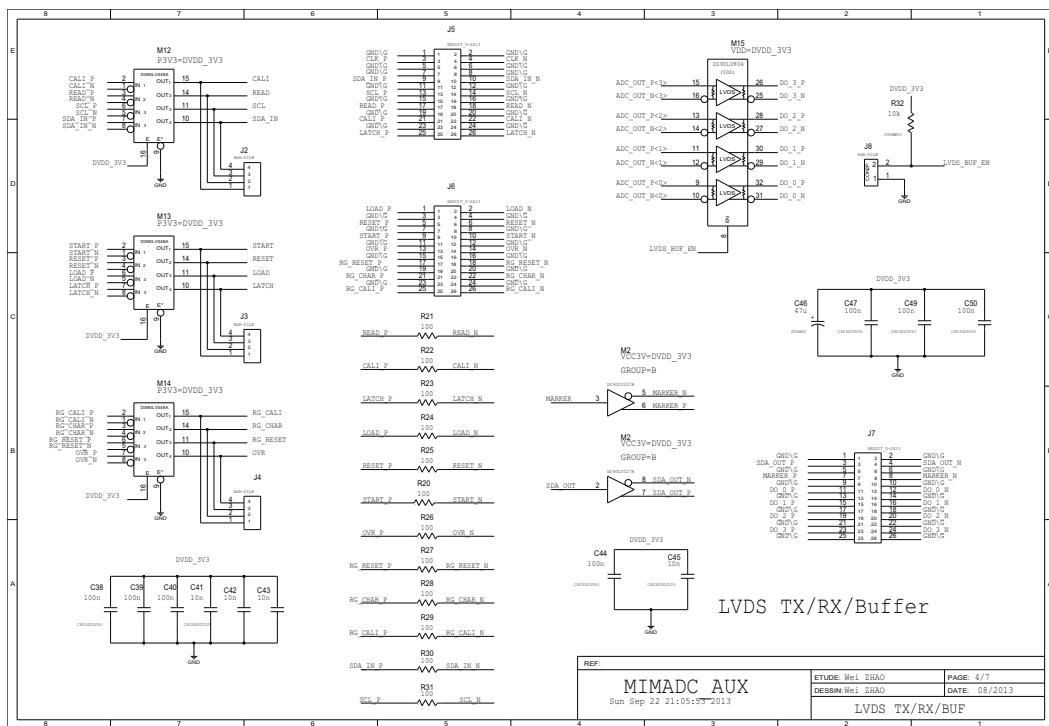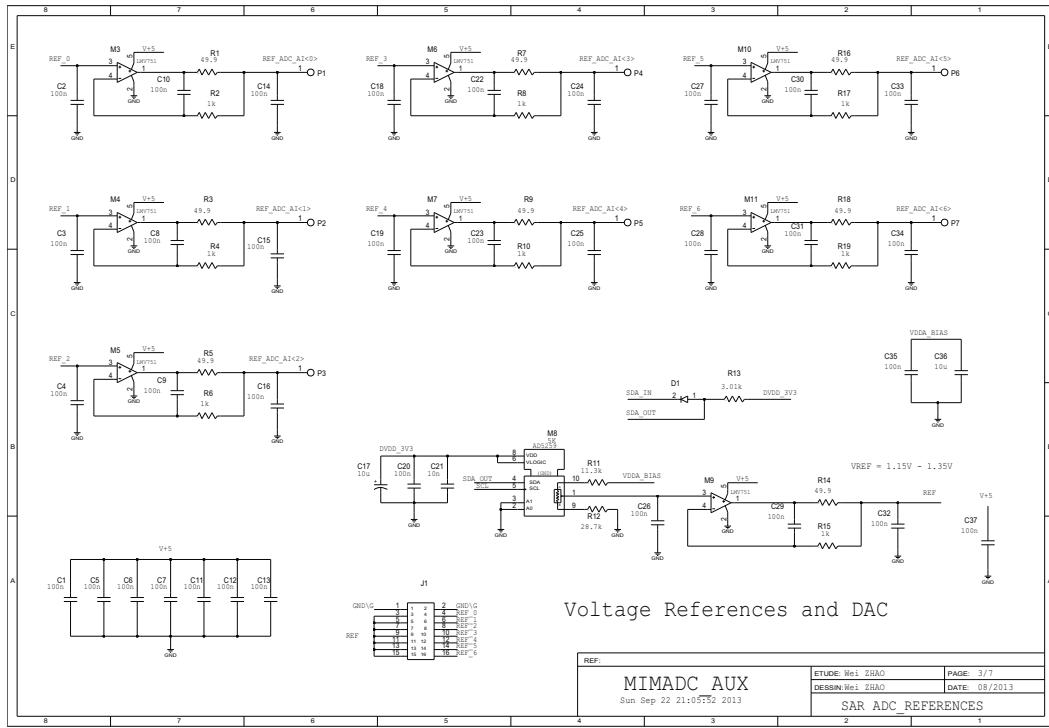
Figure A.2: *Third and fourth page of the schematic of the MIMADC auxiliary test board.*

Voltage References

MIMADC AUX
Sun Sep 22 21:05:53 2013

VOLTAGE BIAS

Analog Buffer & Static Select Signal

MIMADC AUX
Sun Sep 22 21:05:53 2013

ANALOG/CONTROL SWITCH
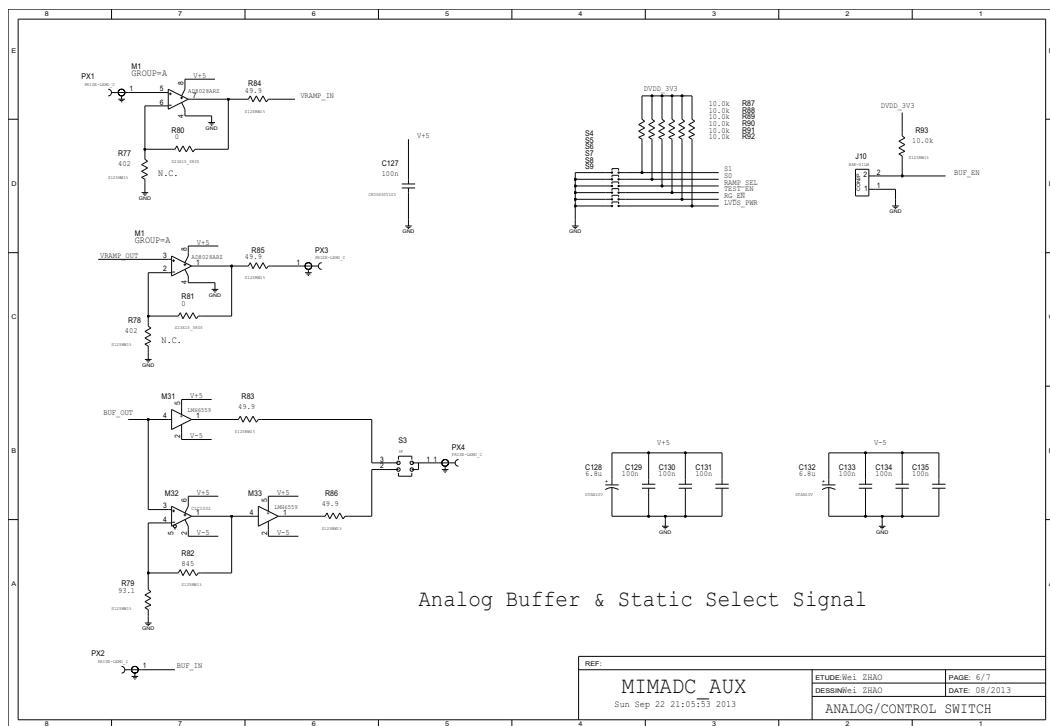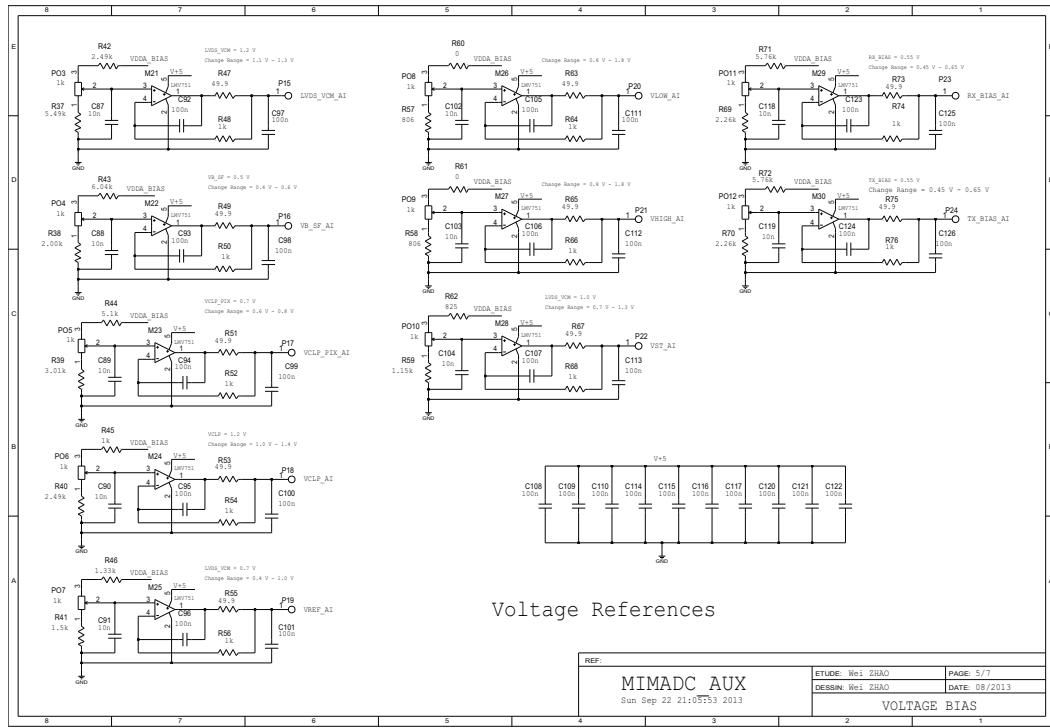
Figure A.3: *Fifth and sixth page of the schematic of the MIMADC auxiliary test board.*
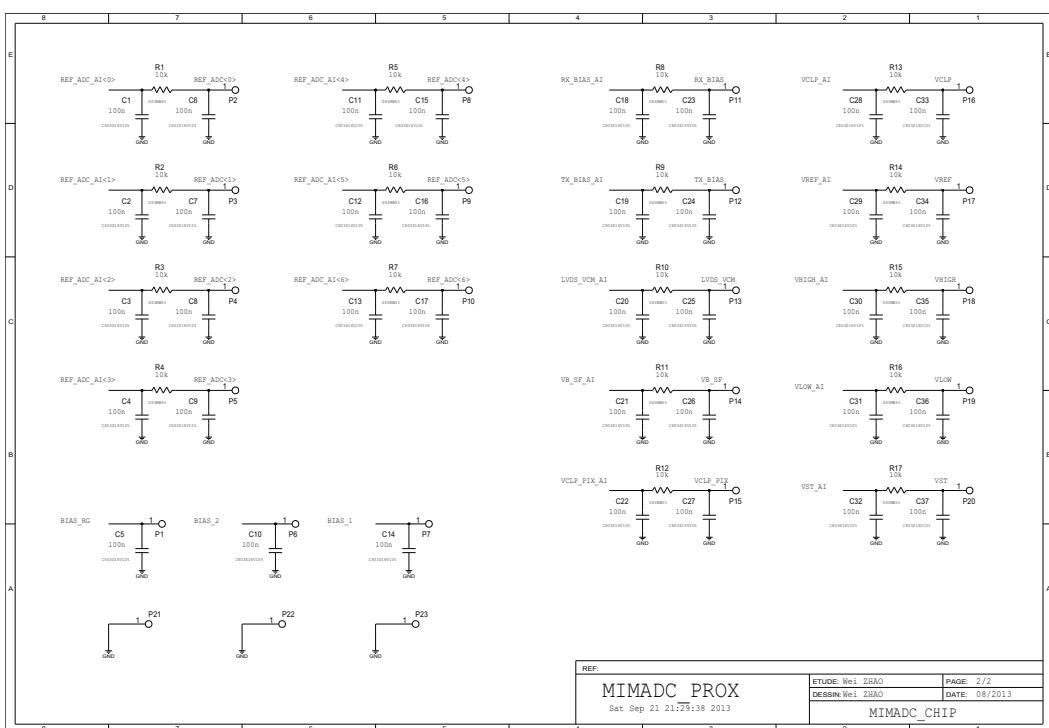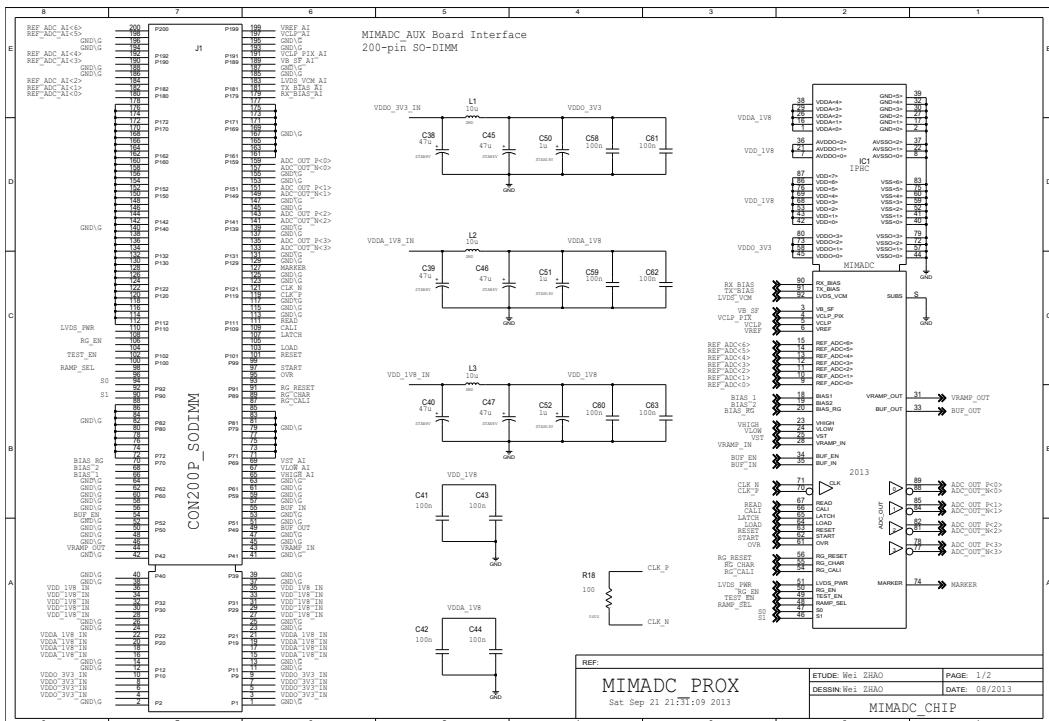
Figure A.4: *First and second page of the schematic of the MIMADC proximity test board.*

B

Calculation of offset in pre-amplifier
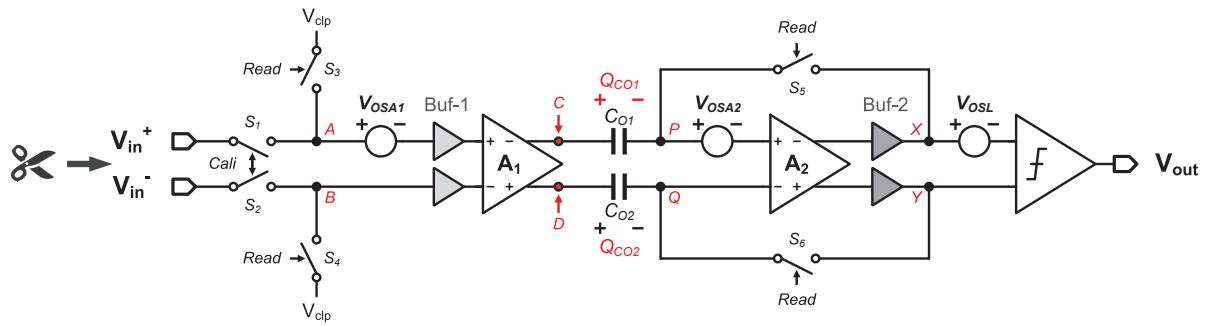
Figure B.1: *Architecture of the pre-amplifier including the input offset sources.*

To arrive at the input offset of the pre-amplifier shown in Fig. 4.19, we firstly consider an equivalent circuit as shown in Fig. B.1, where the voltage sources V_{OSA1}, V_{OSA2}, and V_{OSL} are the input offset of amplifiers A_1, A_2, and the latch, respectively. This pre-amplifier features a fully differential architecture. For simplicity of calculation, a half circuit of the pre-amplifier can be achieved by cutting the pre-amplifier from the center. By this method, the half circuit which represents the upper part of the pre-amplifier is shown in Fig. B.1, where the offset sources are preserved in this circuit. The negative input of the A_1 and A_2 are replaced with the reference voltages V_{CM1} and V_{CM2} respectively, both of which are the common-input voltage of amplifiers. We also assume that both coupling capacitors C_{O1} and C_{O2} have the same value, equal to C_O. For simplicity, the gains of four buffers are considered to be one, and their offsets are incorporated into both offset voltage sources V_{OSA1} and V_{OSA2}.

As discussed in Sec. 4.3.3.2, the operation of the pre-amplifier controlled by the signals "Read" and "Cali" can be subdivided into two phase: calibration phase and amplification phase. Therefore, the calculation of the offset is based on the charge redistribution principle and carries out in each phase as follows.

1. **Calibration phase** :

    During this phase, signal "Read" turns on the switches S_3 and S_5, and meantime the input voltage is disconnected from the pre-amplifier. According to the input/output
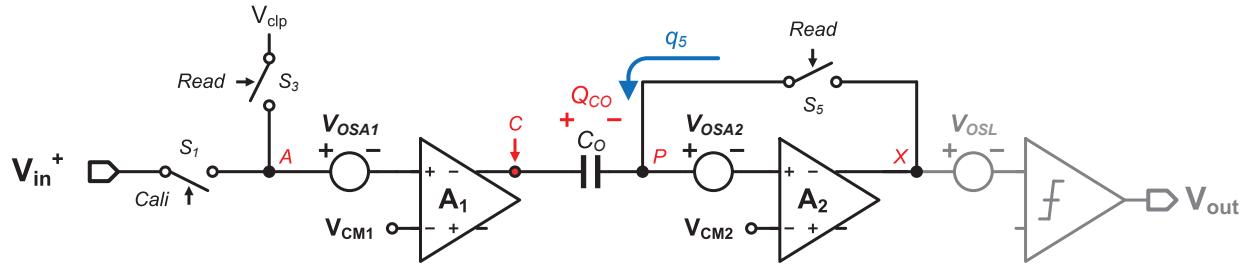
Figure B.2: *Half circuit of Fig. B.1.*

relation of both A_1 and A_2, the following equations can be obtained as

$$V_C = (V_{clp} + V_{OSA1} - V_{CM1})(-A_{v1}) \tag{B.1}$$

and

$$V_P = (V_P + V_{OSA2} - V_{CM2})(-A_{v2}) , \tag{B.2}$$

where A_{v1} and A_{v2} are the absolute value of gain of A_1 and A_2, respectively. It should be noted that both gains are the negative values. The voltage on nodes "C" and "P" are V_C and V_P respectively. V_P can be calculated from Eq. (B.2), as

$$V_P = (V_{CM2} - V_{OSA2})\frac{A_{v2}}{A_{v2} + 1} . \tag{B.3}$$

The charge deposited on the coupling capacitor C_O is Q_{CO}, given as

$$\begin{aligned} Q_{CO} &= (V_C - V_P)C_O \\ &= \left[(V_{clp} + V_{OSA1} - V_{CM1})(-A_{v1}) - (V_{CM2} - V_{OSA2})\frac{A_{v2}}{A_{v2} + 1}\right]C_O . \end{aligned} \tag{B.4}$$

2. **Calibration phase $\rightarrow$ Amplification phase** :

   As soon as "Read" turns off the switches S_3 and S_5, S_5 inject a part of channel charges, q_5, on the negative plate of C_O. The charge stored on C_O then increases to

$$Q_{CO} = \left[(V_{clp} + V_{OSA1} - V_{CM1})(-A_{v1}) - (V_{CM2} - V_{OSA2})\frac{A_{v2}}{A_{v2} + 1}\right]C_O + q_5 . \tag{B.5}$$

Note that, the injected charge due to S_1 and S_3 contributes no offset for the circuit.

3. **Amplification phase** :

   In this phase, the charge on C_O maintains a same value as that in calibration phase. Therefore, this relation is established as

$$Q_{CO} = (V_C' - V_P')C_O , \tag{B.6}$$

where V_C' and V_P' are the voltages on nodes "C" and "P" during the amplification phase. V_C' can be calculated as

$$V_C' = (V_{in}^+ + V_{OSA1})(-A_{v1}) . \tag{B.7}$$

From Eqs. (B.5), (B.6), and (B.7), the voltage V_P' is obtained as

$$V_P' = (-A_{v1})(V_{in}^+ - V_{clp} - V_{CM1}) + (V_{CM2} - V_{OSA2}\frac{A_{v2}}{A_{v2}+1}) - \frac{q_5}{C_O} . \tag{B.8}$$

V_P' is amplified by A_2, and then generates the voltage V_X' on node "X", which is the output of the pre-amplifier. V_X' is obtained as

$$V_X' = (-A_{v2})(V_P' + V_{OSA2}) . \tag{B.9}$$

From both Eqs. (B.8) and (B.9), we can achieve the value of V_X' as a function of input voltage V_{in}^+:

$$\begin{aligned}
V_X' &= A_{v1}A_{v2} \cdot V_{in}^+ - A_{v1}A_{v2}(V_{clp} - V_{CM1}) - A_{v2}(V_{CM2} - V_{OSA2})\frac{A_{v2}}{A_{v2}+1} \\
&+ A_{v2}\frac{q_5}{C_O} - A_{v2}V_{OSA2} .
\end{aligned} \tag{B.10}$$

A similar calculation can be applied to the lower half circuit shown in Fig. B.1 to reach the voltage on the negative output of pre-amplifier, "Y", as well. The voltage V_Y' has an identical format as Eq. (B.10), but the offset voltages do not exist. V_Y' can be calculated as

$$\begin{aligned}
V_Y' &= A_{v1}A_{v2} \cdot V_{in}^- - A_{v1}A_{v2}(V_{clp} - V_{CM1}) - A_{v2}V_{CM2}\frac{A_{v2}}{A_{v2}+1} \\
&+ A_{v2}\frac{q_6}{C_O} ,
\end{aligned} \tag{B.11}$$

where q_6 is the charge injection due to the switch S_6, and V_{in}^- is the input voltage connected to the negative input node of pre-amplifier.

From Eqs. (B.10) and (B.11), the differential output of the pre-amplifier at the end of the amplification phase can be obtained as

$$V_{XY}' = A_{v1}A_{v2} \cdot (V_{in}^+ - V_{in}^-) + A_{v2}V_{OSA2}\frac{A_{v2}}{A_{v2}+1} + A_{v2}\frac{\Delta q_{5,6}}{C_O} - A_{v2}V_{OSA2} , \tag{B.12}$$

where $\Delta q_{5,6}$ is the mismatch of charge injection from switches S_5 and S_6, i.e. $\Delta q_{5,6} = q_5 - q_6$.

In Eq. (B.12), the first item is the differential input amplified by the cascaded amplifier A_1 and A_2, and the rest items are contributed by offset of pre-amplifier. Dividing the V_{XY}' by the total gain of pre-amplifier, i.e. $A_{v1}A_{v2}$, the equivalent input offset can be

calculated, as given in Eq. (B.13), where the offset of latch is considered as well.

$$V_{OS,in} = -\frac{V_{OSA2}}{A_{v1}(A_{v2}+1)} + \frac{\Delta q_{5,6}}{A_{v1}C_O} + \frac{V_{OSL}}{A_{v1}A_{v2}} \, , \qquad (B.13)$$

C

Histogram measurement of ADC linearity

The measurement based on the histogram testing is widely used to determine the linearity of ADC. As a kind of code density test, this approach is quite simple and easy to apply. The ramp histogram and sine histogram can be used. With respects to ramp histogram testing, a linear ramp is applied to the ADC. The rising rate of ramp is much slower than ADC sampling rate and the range of ramp is slightly exceeds both ends of the dynamic range of the ADC. A large number of samples are collected, and the number of occurrences in terms of each code are tallied. The DNL and INL of the ADC can be extracted from the code density of the measurement.

Assuming the resolution of ADC under the test is n bits, the steps of calculating the DNL and INL from the results of histogram testing is given as following [1, 2]:

- Applying the input of ramp for ADC, and the occurrences of the ADC output with respect to each code are counted. Total M_T samples are recorded for the code "1" to "$2^n - 2$". Meanwhile, the counts falling in the bin "0" and "$2^n - 1$" are not included in the M_T;

- Counting the number of occurrences in terms of each code: $H(n)$, where n is the bin number;

- The average number of occurrences for each bin is:

$$H_{aver} = \frac{M_T}{2^n - 2} = \frac{\sum\limits_{n=1}^{2^n-2} H(n)}{2^n - 2}; \tag{C.1}$$

- Calculating DNL(n) for each code from $n = 1$ to $n = 2^n - 2$:

$$DNL(n) = \frac{H(n)}{H_{aver}} - 1. \tag{C.2}$$

The $DNL(0)$ and $DNL(2^n - 1)$ are set to zero;

- Accumulating the $DNL(n)$ to calculate the $INL(n)$.

The INL for last code $2^n - 2$ can be calculated as

$$INL(2^n - 2) = \sum_{n=1}^{2^n-2} DNL(n)$$

$$= \sum_{n=1}^{2^n-2} \left[\frac{H(n)}{H_{aver}} - 1 \right] = \frac{\sum_{n=1}^{2^n-2} H(n)}{H_{aver}} - (2^n - 2). \tag{C.3}$$

Substituting Eq. (C.2) into this gives

$$INL(2^n - 2) = \frac{M_T}{H_{aver}} - (2^n - 2) = 0. \tag{C.4}$$

The reason of the $INL(2^n - 2) = 0$ is the calculation of DNL and INL employs the end-point fit method. The straight line representing the ideal ADC transfer curve passes the endpoint, i.e. the code $(2^n - 2)$, resulting in a zero INL value.

Bibliography

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[2] H. Okawara, "Histogram method in ADC linearity test," Verigy, Ltd, Tech. Rep., 2009.

Abstract

This thesis presents the development of CMOS pixel sensors (CPS) integrated with pixel-level ADCs for the outer layers of the ILD (International Large Detector) vertex detector. Driven by physics in the ILC (International Linear Collider), an unprecedented precision is required for the detectors. The priority of the sensors mounted on the outer layers is low power consumption due to the large coverage ratio of the sensitive area ($\sim$90%) in the vertex detector. The CPS integrated with ADCs is a promising candidate for this application. The architecture of column-level ADCs, exists but do not provide an optimized performance in terms of noise and power consumption. The concept of pixel-level ADCs has been proposed. Benefiting from the all-digital pixel outputs, pixel-level ADCs exhibit the obvious merits on noise, speed, insensitive area, and power consumption. In this thesis, a prototype sensor, called MIMADC, has been implemented by a 0.18 μm CIS (CMOS Image Sensor) process. The target of this sensor is to verify the feasibility of the CPS integrated with pixel-level ADCs. Three matrices are included in this prototype but with two different types of pixel-level ADCs: one with successive approximation register (SAR) ADCs, and the other two with single-slope (SS) ADCs. All of them feature a same pixel size of 35$\times$35 μm^2 and a resolution of 3-bit. In this thesis, the prototype is presented for both theoretical analyses and circuit designs. The test results of the prototype are also presented.

Keywords: Charge particle detection, CPS (CMOS Pixel Sensors), Pixel-level ADCs (Analog-to-Digital Converters), ASIC (Application Specific Integrated Circuit), ILC (International Linear Collider), ILD (International Large Detector), VTX (Vertex Detector), DPS (Digital Pixel Sensors).

Résumé

La thèse présente le développement de CPS (CMOS Pixel Sensors) intégré avec CAN au niveau du pixel pour les couches externes du détecteur de vertex de l'ILD (International Large Detector). Motivé par la physique dans l'ILC (International Linear Collider), une précision élevée est nécessaire pour les détecteurs. La priorité des capteurs qui montre sur les couches externes est une faible consommation d'énergie en raison du rapport de couverture de la surface sensible (~90%) dans le détecteur de vertex. Le CPS intégré avec CAN est un choix approprié pour cette application. L'architecture de CAN de niveau colonne ne fournit pas une performance optimisée en termes de bruit et consommation d'énergie. La conception de CAN au niveau du pixel a été proposée. Bénéficiant des sorties de pixels tout-numérique, CAN au niveau des pixels présentent les mérites évidents sur le bruit, la vitesse, la zone sensible et la consommation d'énergie. Dans cette thèse, un prototype de capteur, appelé MIMADC, a été implémenté par un processus de 0.18 μm CIS (CMOS Image Sensor). L'objectif de ce capteur est de vérifier la faisabilité du CPS intégré avec les CAN au niveau des pixels. Trois matrices sont incluses dans ce prototype, mais avec deux types différents de CAN au niveau de pixel: une avec des CAN à registre à approximations successives (SAR), et les deux autres avec des CAN à une seule pente (Single-Slope, SS) CAN. Toutes les trois possédant les pixels de la même taille de 35×35 μm^2 et une résolution de 3-bit. Dans ce texte, des analyses théoriques et le prototype sont présentés, ainsi que la conception détaille des circuits.

Mots-clés: Détection de particules de charge, CPS (CMOS Pixel Sensors), CAN (Convertisseur Analogique-Numérique) au niveau du pixel, ASIC (Application Specific Integrated Circuit), ILC (International Linear Collider), ILD (International Large Detector), VTX (Vertex Detector), DPS (Digital Pixel Sensors).