UNIVERSITÀ DI PISA
Scuola di Dottorato in Ingegneria "Leonardo da Vinci"
UNIVERSITÈ BORDEAUX 1
Ecole Doctorale des Sciences Physiques et de l'Ingeniéur

Corso di Dottorato di Ricerca in Ingegneria dell'Informazione
Cours de Doctorat en Électronique
Tesi di Dottorato di Ricerca - Thèse de Doctorat - Doctoral Thesis

Deep Sub-micron RF-CMOS Design and Applications of Modern UWB and Millimeter-wave Wireless Transceivers

Autore - Auteur - Author

Domenico PEPE _____

Relatori - Directeurs de Thèse - Supervisors
Dr. Domenico ZITO (Università di Pisa) _____
Dr. Thierry TARIS (Universitè Bordeaux 1) _____
Prof. Bruno NERI (Università di Pisa) _____
Prof. Jean-Baptiste BEGUERET (Universitè Bordeaux 1) _____

Pisa, Italy, 2009

Examining Commission

Prof. Carmine Ciofi
Dipartimento di Fisica della Materia e Ingegneria Elettronica, Università di Messina

Prof. Guido Masera
Dipartimento di Elettronica, Politecnico di Torino

Prof. Massimo Macucci
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa

Dr. Domenico Zito
Tyndall National Institute, University College Cork

Prof. Bruno Neri
Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa

Dr. Thierry Taris
Laboratoire IMS, Universitè Bordeaux 1

Prof. Jean-Baptiste Begueret
Laboratoire IMS, Universitè Bordeaux 1

Final Examination

25th June, 2009, Pisa

To my parents

Acknowledgements

First of all I am grateful to my Family, for fully supporting me in all these years.

I am grateful to my supervisors, Dr. Domenico Zito, Dr. Thierry Taris, Prof. Bruno Neri and Prof. Jean-Baptiste Begueret, for their precious support and assistance. A special thanks to Domenico Zito, who made this research work possible and that in these years has been a teacher and a friend.

I am grateful to all my colleagues and people that have been worked at RFLab (Pisa), from my MSc thesis mates, to PhD mates, and to all the people that made here their thesis, whose work has been very important for this research.

I am grateful to all my collegues and professors of the IMS Laboratory (Bordeaux), in particular Thierry Taris for his precious support and availability.

Moreover, I am grateful to Prof. De Rossi and collegues of "Centro Piaggio" for their support.

Sommario

L'attività di ricerca scientifica effettuata nell'ambito del corso di dottorato di ricerca si è svolta nel settore della progettazione di circuiti integrati a radio-frequenza, per sistemi ultra-wideband (UWB) e alle onde millimetriche, e si è articolata nei seguenti temi: (i) circuiti integrati a radio-frequenza per ricetrasmettitori a basso consumo di potenza potenza per reti locali wireless; (ii) radar UWB completamente integrato per il monitoraggio cardio-polmonare in tecnologia 90nm CMOS; (iii) amplificatori a basso rumore (LNA) a 60 GHz in tecnologia standard 65nm CMOS.

Nel Capitolo 1 una valutazione teorica della massima distanza operativa dei Radio Frequency Identification Device (RFID) passivi e il progetto di un ricetrasmettitore a bassa potenza per applicazioni ZigBee (IEEE 802.15.4) a 2.4 GHz in tecnologia 0.35µm Bi-CMOS di Austriamicrosystems sono riportati. Inoltre, viene presentato il progetto di un oscillatore controllato in tensione (VCO) a 5-6 GHz in tecnologia 0.35µm di Austriamicrosystems. In particolare, gli induttori sono stati realizzati mediante una nuova versione dell'induttore attivo chiamato "Boot-Strapped Inductor" (BSI). Infine, viene presentato un nuovo circuito equivalente a larga banda, a componenti discreti indipendenti dalla frequenza, per descrivere in termini di equivalenti elettrici a parametri concentrati il comportamento di induttori a spirale integrati su silicio.

Nel Capitolo 2 viene presentata l'attività di ricerca riguardante la realizzazione di un sistema radar UWB indossabile per il monitoraggio cardio-polmonare completamente integrato in tecnologia 90nm CMOS. In dettaglio, sono riportati lo studio di fattibilità, l'analisi di sistema e i risultati delle simulazioni di sistema. Inoltre, viene riportato il progetto dei principali blocchi del sensore radar UWB (l'amplificatore a basso rumore (LNA), il generatore di impulsi e il generatore di ritardo) in tecnologia 90nm CMOS di ST-Microelectronics. I test-chip sono stati realizzati e caratterizzati sperimentalmente. Sono riportati i risultati delle misure, che si sono dimostrati in eccellente accordo con i risultati delle simulazioni post-layout.

Nel Capitolo 3, infine, il progetto di un amplificatore a basso rumore (LNA) a 60 GHz in tecnologia 65nm CMOS di ST-Microelectronics è riportato. Il LNA sfrutta una nuova topologia per ottenere l'adattamento di impedenza in ingresso basata sull'uso di un trasformatore integrato, che permette la realizzazione dell'adattamento di impedenza senza l'applicazione di una degenerazione sul source, che causa un abbassamento del guadagno dell'amplificatore, cosa indesiderata specialmente alle onde millimetriche.

Riassunto

L'attività di ricerca scientifica effettuata nell'ambito del corso di dottorato di ricerca si è svolta nel settore della progettazione di circuiti integrati a radio-frequenza, per sistemi ultra-wide-band (UWB) e alle onde millimetriche, e si è articolata nei seguenti temi: (i) circuiti integrati a radio-frequenza per ricetrasmettitori a basso consumo di potenza per reti locali wireless; (ii) radar UWB per il monitoraggio cardio-polmonare in tecnologia 90nm CMOS; (iii) amplificatori a basso rumore (LNA) a 60 GHz in tecnologia standard 65nm CMOS.

Questa tesi di dottorato è organizzata in tre Capitoli, ognuno dei quali tratta uno di questi temi sopra elencati affrontati durante la ricerca di dottorato.

Capitolo 1: Circuiti Integrati a Radio-frequenza per Ricetrasmettitori a Bassa Potenza per Reti Locali Wireless

Negli ultimi anni l'interesse in applicazioni a basso data-rate, come i Radio-Frequency Identification Device (RFID), e le reti di sensori wireless, è rapidamente cresciuto. Con esso è cresciuta notevolmente anche la richiesta di ricetrasmettitori a basso costo e basso consumo di potenza. I sistemi RFID possono essere classificati in passivi e attivi. I dispositivi passivi possono essere fabbricati a bassissimo costo, tuttavia hanno dei range di funzionamento di qualche metro, che dipende sostanzialmente dalla potenza richiesta dai tag per funzionare. È stata effettuata una valutazione teorica della massima distanza operativa dei RFID passivi [OP1]. Estendere il range di funzionamento dei dispositivi RFID a distanze superiori a una decina di metri è possibile utilizzando tag attivi.

Un ricetrasmettitore a bassa potenza per applicazioni ZigBee (IEEE 802.15.4) a 2.4 GHz è stato progettato in tecnologia 0.35µm Bi-CMOS di Austriamicrosystems e presentato in [OP1, OP4]. Il ricevitore, che consiste in un LNA e un mixer I/Q, presenta una cifra di rumore (NF) di 8.7 dB, un guadagno in tensione di 26 dB un punto di intercetta del del terzo ordine riferito all'ingresso (iIP3) di -13 dBm, con un consumo di potenza di 8.6 mW. Il trasmettitore consiste in un amplificatore di potenza a due stadi (un preamplificatore in classe A seguito da un amplificatore in classe C) e due mixer doppiamente bilanciati a cella di Gilbert. Fornisce una potenza di uscita fino a 6 dBm con un consumo di potenza di 16 mW.

Anche l'interesse per canali radio ad elevato data-rate, come nel caso delle Wireless Local Area Network (WLAN), è notevolmente cresciuto negli ultimi anni. Un oscillatore controllato in tensione (VCO) (che tipicamente rappresenta il sottocircuito più critico dell'intero ricetrasmettitore) a 5-6 GHz, è stato progettato in tecnologia 0.35 µm di Austriamicrosystems, e presentato in [OP3, OP7]. Per

ovviare ai limiti nelle prestazioni degli induttori a spirale su silicio, è stata sviluppata anche una nuova versione CMOS dell'induttore attivo ad alto fattore di merito "Boot-Strapped Inductor" (BSI) [OP6]. Questa nuova versione di CMOS BSI è stata opportunamente modificata per essere impiegata al posto degli induttori del filtro risonante del VCO. Un modello per piccolo segnale del nuovo BSI è stato implementato con MATLAB™, in modo da poter efficacemente dimensionare ed ottimizzare l'induttore attivo.

Infine, un nuovo circuito equivalente a larga banda, a componenti discreti indipendenti dalla frequenza, è stato sviluppato per descrivere in termini di equivalenti elettrici a parametri concentrati il comportamento di induttori a spirale integrati su silicio e presentato in [OP5]. Questo nuovo modello è in grado di modellizzare efficacemente il comportamento di un induttore integrato in presenza o meno di uno schermo elettromagnetico sottostante (PGS). Gli elementi RLC del circuito sono stati ricavati direttamente dai parametri S dell'induttore. Sono state sviluppate due diverse procedure di "fitting" che offrono diversi livelli di accuratezza.

Capitolo 2: Radar UWB per il Monitoraggio Cardio-polmonare in Tecnologia 90nm CMOS

Nel 2002 la Federal Communication Commission (FCC) ha approvato l'immissione sul mercato di dispositivi che sfruttano un nuovo standard di comunicazione che impiega segnali ultra-wideband (UWB). Per i sistemi UWB è stata allocata la porzione di spettro radio 3.1-10.6 GHz, per la prima volta in modo non esclusivo. Il concetto che sta alla base della tecnologia UWB è quello di generare, trasmettere e ricevere impulsi a radio frequenza di durata temporale brevissima (da poche decine di picosecondi a poche decine di nanosecondi). Questo fa si che il segnale UWB abbia uno spettro frequenziale molto ampio (vari GigaHertz) e, pertanto, una densità di energia molto bassa. Tra le molteplici applicazioni per i quali i sistemi UWB sono stati pensati, una delle più promettenti è senz'altro quella del imaging medico.

Contrariamente alle tecniche tradizionali per il monitoraggio dell'attività cardiaca, quali l'elettrocardiogramma o l'impiego di trasduttori a ultrasuoni, i sistemi radar a microonde permettono il monitoraggio della parete cardiaca in maniera non invasiva, senza la necessità di applicare sensori a contatto con il corpo del paziente. Inoltre, a differenza dell'elettrocardiografo, permettono di monitorare direttamente la meccanica della parete cardiaca, anziché l'attività elettrica del cuore. Ci permetterebbe di rivelare l'insorgenza di numerose patologie cardiache che non si manifestano attraverso alcuna anomalia dell'attività elettrica del cuore ad esso associata.

La tecnologia che negli ultimi anni ha registrato il maggiore sviluppo e la maggiore accelerazione in termini di diffusione nel settore delle applicazioni consumer è certamente quella CMOS. Dunque, il sensore radar UWB per il monitoraggio della parete cardiaca può essere realizzato in maniera completamente integrata su un singolo chip, permettendo la realizzazione di dispositivi altamente miniaturizzati, a basso costo e disponibili per il mercato di massa. A questo punto è stata sviluppata l'idea di un sistema indossabile di nuova generazione per il monitor-

aggio costante della frequenza cardiaca e respiratoria, presentata in [OP2, OP8, OP9, OP11, OP12, OP14, OP15, OP16, OP17]. Il sistema è costituito da un sensore radar UWB e una interfaccia radio low-power (IEEE 802.15.4 ZigBee), che ha il compito di acquisire i dati provenienti dal sensore ed inviarli ad una unità remota di elaborazione dati, sia questa "on-body", o facente parte di una infrastruttura wireless tipo WLAN. La topologia di radar più promettente per questo tipo di applicazione è quella dei radar ad impulsi, per via della loro semplicità architetturale e dei ridotti consumi di potenza.

Per quanto riguarda il progetto del sistema radar, uno studio del canale nel quale l'impulso dovrà propagarsi è stato effettuato [OP2, OP9]. Tenendo conto dei vari tessuti del corpo umano e delle loro proprietà dielettriche, è stato sviluppato un modello di canale dipendente dalla frequenza, in modo da poter effettuare le analisi di sistema.

Simulazioni preliminari hanno permesso di individuare nella topologia di tipo correlatore la topologia di ricevitore che garantisce un maggior rapporto segnale-rumore all'uscita del ricevitore e una maggiore sensibilità a piccoli spostamenti della parete cardiaca. Un'analisi di sistema è stata effettuata in modo da ripartire le specifiche di sistema tra i vari blocchi del radar UWB. Un modello del canale, che descrive sia le perdite frequenza per frequenza, sia il movimento della parete cardiaca, è stato implementato in modo da poter essere inserito nel simulatore Ptolemy in Agilent ADS2005A™. Misure di canale sono state effettuate al fine di verificare la validità del modello proposto [OP2, OP15, OP16]. I risultati mostrano attenuazioni molto prossime ai valori predetti dal modello proposto e da altri lavori pubblicati in letteratura. L'intero sistema è stato simulato, e i risultati delle simulazioni di sistema hanno dimostrato la fattibilità del progetto [OP2, OP8, OP9, OP11, OP12, OP14].

I principali blocchi del sensore radar UWB (amplificatore a basso rumore (LNA), generatore di impulsi e generatore di ritardo) sono stati progettati e realizzati in tecnologia 90nm CMOS di ST-Microelectronics. I circuiti sono stati caratterizzati on-chip utilizzando micro-punte. Il LNA è costituito da un primo stadio a gate comune e due stadi successivi a source comune. Lo stadio di ingresso common gate realizza un adattamento di impedenza a banda larga in ingresso. I due stadi seguenti a source comune forniscono un ulteriore amplificazione di tensione. Le misure mostrano un guadagno di trasduttore di 22.7 dB a 5.2 GHz, una banda a 3-dB di circa 5 GHz, un coefficiente di riflessione in ingresso inferiore a -10.5 dB su tutta la banda, e un punto di compressione a 1-dB di -19.7 dBm, in eccellente accordo con i risultati delle simulazioni post-layout. La cifra di rumore è prossima a 5.5 dB su tutto il range 3.1-10.6 GHz. Il consumo di potenza è 34.8 mW (alimentazione 1.2 V) [OP15, OP16]. Il generatore di impulsi UWB genera un impulso monociclo quando attivato dal fronte negativo di un segnale di comando fornito da un micro-controllore, sfruttando il principio dei formatori d'onda non-lineari. Misure on-chip mostrano che il generatore di impulsi genera un impulso con una durata temporale pari a 430 ps e una ampiezza picco-picco di durata 660 mV. Il consumo di potenza è 19.8 mW (alimentazione 1.2 V) [OP10, OP16]. Il generatore di ritardo è in grado di ritardare, con un ritardo programmabile da 1 a 3 ns, il fronte di discesa di un segnale digitale, in modo da permettere la generazione ritardata (di un ritardo pari al tempo di volo dell'impulso dal radar

al cuore e di nuovo al radar) di una replica locale (on-chip) dell'impulso trasmesso per valutare quindi la correlazione tra questa e l'eco ricevuto proveniente dalla parete cardiaca. Il ritardo è programmabile mediante 5 bit [OP10, OP16].

Si è affrontato l'integrazione totale del sistema radar. Il layout dell'intero sistema radar è stato realizzato in tecnologia 90nm CMOS di ST-Microelectronics e mandato in fonderia.

Capitolo 3: Amplificatore a basso rumore (LNA) a 60 GHz in tecnologia standard 65nm CMOS

Un amplificatore a basso rumore (LNA) a 60 GHz in tecnologia 65nm CMOS di ST-Microelectronics è stato progettato presso il laboratorio IMS (Laboratoire de l'Intégration du Matériau au Système) con sede a Bordeaux (Francia), e presentato in [OP13].

È stata impiegata una nuova tecnica per l'adattamento di impedenza in ingresso, che prevede l'uso di un trasformatore integrato. Il primario del trasformatore è connesso tra l'ingresso a radio-frequenza e il gate del transistor a source comune di un amplificatore cascode, mentre il secondario è connesso tra il drain del transistor a source comune e il source del transistor cascode. Questa tecnica permette la realizzazione dell'adattamento di impedenza senza l'applicazione di una degenerazione sul source, che causa un abbassamento del guadagno dell'amplificatore, cosa indesiderata specie alle onde millimetriche.

È stato sviluppato un modello del transistor all'interno del simulatore ADS di Agilent per analizzare l'effetto dei parassiti sulle prestazioni del LNA. Dopo aver dimensionato i componenti del LNA, un trasformatore integrato è stato progettato con il simulatore elettromagnetico 3D HFSS di Ansoft™. Il LNA è stato realizzato mediante due stadi in cascata per raggiungere le specifiche di guadagno desiderate. Le simulazioni post-layout mostrano un guadagno di 10.02 dB a 60 GHz, ed un coefficiente di riflessione in ingresso di -16.84 dB a 61.45 GHz. Per minimizzare l'effetto dei pad sono stati inseriti degli induttori per risuonare con la capacità del pad alla frequenza di interesse. In fase di misura è stato riscontrato che la struttura risonante pad-induttore risuona fuori dal range di funzionamento del LNA. Simulazioni dei pad con simulatori elettromagnetici 3D (HFSS™) hanno confermato che l'estrattore di parassiti fallisce a frequenze così elevate, sovrastimando la capacità parassita del pad. Un re-design del circuito è in corso.

Sommaire

L'activité de recherche scientifique effectuée dans le cadre de mon doctorat de sciences s'est déroulé dans le secteur du projet de circuits intégrés radiofrèquences, pour des systèmes ultra-wideband (UWB) et aux ondes millimetriques, et s'est articulée comme suit: (i) circuits intégrés radiofrèquences pour émetteur-récepteur basse puissance pour réseaux locaux wireless; (ii) radar UWB complètement intégré pour la surveillance cardio-pulmonaire en technologie 90nm CMOS; (iii) amplificateurs à faible bruit (LNA) à 60 GHz en technologie standard 65nm CMOS.

Dans les Chapitre 1 une évaluation théorique de la distance opérationnelle des Radio Frequency Identification Device (RFID) passifs et le projet d'un émetteur-récepteur à basse puissance pour applications ZigBee (IEEE 802.15.4) à 2.4 GHz en technologie 0.35µm Bi-CMOS de Austriamicrosystems sont rapportés. En plus, il est présenté le projet d'un oscillateur contrôlé en tension (VCO) à 5-6 GHz en technologie 0.35µm de Austriamicrosystems. En particulier, les inductances ont été réalisées par une nouvelle version de l'inductance actif "Boot-Strapped Inductor" (BSI). Enfin, il est présenté un nouveau circuit équivalent large bande, avec composantes discrets indépendants de la fréquence, decrivant le comportement des inducteurs à spirale intégrés sur silicium.

Le Chapitre 2 est dédiée à la réalisation d'un système radar UWB portable pour la sourveillance cardio-pulmonaire complètement intégré en technologie 90nm CMOS. En détails, sont rapportés l'étudie de faisabilité, l'analyse de système et les résultats des simulations de système. En plus, il est rapporté le projet des principaux blocs du capteur radar UWB (l'amplificateur à faible bruit (LNA), le générateur d'impulsions et le générateur de retard) en technologie 90nm CMOS de ST-Microelectronics. Les test-chip ont été réalisés et caractérisés expérimentalement. Les résultats des mesures sont rapportés ici et présentant une excellent corrélation avec les résultats des simulations post-layout.

Dans le Chapitre 3, enfin, le projet d'un amplificateur à faible bruit (LNA) à 60 GHz en technologie 65nm CMOS de ST-Microelectronics est rapporté. Le LNA exploite un nouvelle topologie pour obtenir l'adaptation d'impédance en entrée basée sur l'emploie d'un transformateur intégré, qui permet la réalisation de l'adaptation d'impédance sans l'application d'une dégénérescence de source, qu'il cause un abaissement du gain de l'amplificateur, chose pas désirée en particulier aux ondes millimetriques.

Résumé

L'activité de recherche scientifique effectuée dans le cadre de mon doctorat de sciences s'est déroulé dans le secteur du projet de circuits intégrés radiofrèquences, pour des systèmes ultra-wideband (UWB) et aux ondes millimetriques, et s'est articulée comme suit: (i) circuits intégrés radiofrèquences pour émetteur-récepteur basse puissance pour réseaux locaux wireless; (ii) radar UWB complètement intégré pour la surveillance cardio-pulmonaire en tecnologie 90nm CMOS; (iii) amplificateurs à faible bruit (LNA) à 60 GHz en technologie standard 65nm CMOS.

Cette thèse de doctorat est organisée en trois chapitres, dont chacun traite un de ces thèmes sur énumérés affrontés pendant la recherche de doctorat.

Chapitre 1: Circuits Intégrés Radiofrèquences pour Émetteur-récepteur à Basse Puissance pour Réseaux Locaux Wireless

Depuis quelques années on observe un interêt croissant pour l'interesse en applications à bas débit, telles les Radio-Frequency Identification Device (RFID), et les réseaux de capteurs wireless. Avec lui elle a crû considérablement même la demande d'émetteur-récepteur à bas coût et bas consommation de puissance. Les systèmes RFID peuvent être classifiés dans passifs et actifs. Les dispositifs passifs peuvent être fabriqué à tres bas coûte, toutefois ils ont des range de fonctionnement de quelque mètre, qui dépend substantiellement de la puissance demandée du tag pour fonctionner. Une évaluation théorique de la distance opérationnelle de RFID passifs a été effectuée [OP1]. Étendre le range de fonctionnement des dispositifs RFID à des distances supérieures à une dizaine de mètres est possible en utilisant tag actifs.

Un émetteur-récepteur à basse consommation de puissance pour applications ZigBee (IEEE 802.15.4) à 2.4 GHz a été implémenté en technologie 0.35µm BiCMOS d'Austriamicrosystems et est présenté en [OP1, OP4]. Le récepteur, qui consiste en un LNA et un mélangeur I/Q, présente un facteur de bruit (NF) de 8.7 dB, un gain en tension de 26 dB, un point de intercepte de troisième ordre (IIP3) de -13 dBm, avec une consommation de puissance de 8.6 mW. L'émetteur comporte un amplificateur de puissance à deux étages (preamplificateur en classe A suivi d'un amplificateur en classe C) et deux mélangeurs doublement équilibrés à cellule de Gilbert. Il fournit une puissance de sortie de 6 dBm avec une consommée de puissance de 16 mW.

De même l'interêt pour des liens à hauts débit, telle les Wireless Local Area Network (WLAN), il a considérablement crû depuis quelques années. Un oscillateur contrôlé en tension (VCO) (que typiquement représente le bloc le plus

critique d'une chaîne Tx/Rx) à 5-6 GHz, a été realisé en technologie 0.35µm d'Austriamicrosystems, et est présenté en [OP3, OP7]. Pour pallier aux limites des inductances sur silicium, une nouvelle approche CMOS de l'inducteur actif à haut facteur de mérite "Boot-Strapped Inductor" (BSI) [OP6]a été mise en place. Cette nouvelle version de BSI CMOS est employée à la place des inductances du filtre self-résonant du VCO. Un modèle petit signale du nouveau BSI a été developpé avec MATLAB™, pour pouvoir efficacement dimensionner et optimiser l'inducteur actif.

Enfin, un nouveau modèle équivalent large bande, à composantes discrets indépendants de la fréquence, a été développé pour décrire le comportement d'inducteurs à spirale intégrés sur silicium et présenté en [OP5]. Ce nouveau modèle est capable de modèliser le comportement d'une inductance intégrée en présence ou moins d'un plan de masse au dessous (PGS). Les éléments RLC du circuit ont été extraits directement des paramètres S de l'inductance. Deux different procédures de correlation entre simulations et mesures sont ici proposés afin de dimensionner le modèle.

Chapitre 2: Radar UWB pour la Surveillance Cardio-pulmonaire en Technologie 90nm CMOS

En 2002 le Federal Communication Commission (FCC) a approuvé l'arrivée sur le marché de dispositifs qui exploitent un nouveau standard de communication qui emploie des signaux Ultra Large Bande (UWB). Pour les systèmes UWB elle a été allouée la bande de frequences 3.1-10.6 GHz, pour la première fois en mode pas exclusive. Le concept à la base de la technologie UWB est celui d'engendrer, transmettre et recevoir des impulsions radio-fréquence de durée temporelle tres brève (de quelque dizaines de picosecondes à quelque dizaines de nanosecondes). Le signale UWB présent par conséquent un spectre en fréquence très vaste (plusieurs GigaHertz) et une densité d'énergie faible. Parmi les multiples applications pour lesquelles les systèmes UWB ont été pensés, une des plus prometteur est la imagerie medicale.

Contrairement aux techniques traditionnelles pour l'observation de l'activité cardiaque, comme le l'électrocardiogramme ou l'emploi de transducteurs à ultrasons, les systèmes radar à micro-ondes permettent la surveillance du muscle cardiaque de manière peu envahissante, puisq'ils ne necessitent pas l'application de capteurs en contacte avec le corps du patient. D'autre part, en contrôlant ansi directement la mécanique du muscle cardiaque, cette technique permet de prévenir de nombreuses pathologies cardiaques non décelables au travers de la seule observation de l'activité electrique du coeur.

Parce que la technologie CMOS est la plus adaptée au marché de masse RF pour ses qualités d'intégration et de faible coût, le capteur UWB developpé ici, a été implémenté en technologie CMOS de longueur de grille 90 nm.

À ce point elle a été développée l'idée d'un système endossable de nouvelle génération pour la surveillance constant de les fréquences cardiaque et respiratoire, présentée en [OP2, OP8, OP9, OP11, OP12, OP14, OP15, OP16, OP17]. Le système est constitué d'un capteur radar UWB et d'une interface radio low-power (IEEE 802.15.4 ZigBee), qui réalise l'acquisition des données provenants du

capteur et les envoyer à une unité éloignée de traitment des signaux. Le topologie de radars la plus prometteuses pour ce type d'application est celle des radars à impulsions. Elles présente en effect une architecture simple permettant de réduir fortment la consommation de la partie radio.

En ce qui concerne le projet du système radar, un étudie du canal dans lequel l'impulsion devra se propager a été effectuée [OP2, OP9]. En tenant compte des divers tissus du corps humain et des leurs propriétés diélectriques, il a été développé un modèle de canal en function de la fréquence, pour pouvoir effectuer les analyses au niveau système.

Des simulations préliminaires ont permis de déterminer dans la topologie de type correlatore le topologie de récepteur guarantissant un rapport signal-bruit en sortie du récepteur et une sensibilité à des petits déplacements du muscle cardiaque maximum. Des analyses de système ont étés effectuée pour répartir les caractéristiques de système parmi les divers blocs du radar UWB. Un modèle du canal, qui décrit soit les pertes en fréquence, soit le mouvement du muscle cardiaque, a été realisé de façon à pouvoir être inséré dans le simulateur Ptolemy en Agilent ADS2005A™. Des mesures de canal ont été effectuées afin de vérifier la validité du modèle proposé [OP2, OP15, OP16]. Les résultats montrent des atténuations très proches du modèle proposé et d'autres travaux publiés en littérature. Le système entier a été simulé, et les résultats des simulations système ont montré la faisabilité du projet [OP2, OP8, OP9, OP11, OP12, OP14].

Les principaux blocs du capteur radar UWB (amplificateur à faible bruit (LNA), générateur d'impulsions et générateur de retard) ont été réalisés en technologie 90nm CMOS de ST-Microelectronics. Les circuits ont étés caractérisés sur puce en utilisant un banc de test sous pointes. Le LNA est constituée d'un étage grille commune, qui réalise l'adaptation d'entrée large bande, puis deux étages source commune pour l'amplification en tension. Les mesures montrent un gain de 22.7 dB à 5.2 GHz, une bande à 3-dB environ de 5 GHz, un coefficient de réflexion en entrée inférieure à -10.5 dB sur toute la bande, et un point de compression à 1-dB de -19.7 dBm. La chiffre de bruit est proche de 5.5 dB sur tout la bande 3.1-10.6 GHz. La consommation de puissance est de 34.8 mW (alimentation 1.2 V) [OP15, OP16]. Le générateur d'impulsions UWB, activé du front négatif de un signal de commande fourni par un micro-contrôleur, engendre une impulsion monocycle. Il exploite le principe des formateurs d'ondes non linéaires. Des mesures on-chip montrent que le générateur d'impulsions produit une impulsion avec un durée temporelle de 430 ps et une amplitude pic-pic de 660 mV. La consommation de puissance est 19.8 mW (alimentations 1.2 V) [OP10, OP16]. Le generator de retard présente un retard programmabile de 1 à 3 ns commandé par le front de descente de un signal numerique, pour génération tardée (d'un retard pair au temps de vol de l'impulsion du radar au coeur et de nouveau au radar) d'une réplique local (sur puce) de l'impulsion transmise pour évaluer la corrélation entre celle-ci et l'écho reçu provenant du muscle cardiaque. Le retard est programmabile au moyen de 5 bit [OP10, OP16].

L'intégration totale du système radar a été réalisé en technologie 90nm CMOS de ST-Microelectronics et le layout a été envoyé en fonderie.

Chapitre 3: Amplificateur à Faible Bruit (LNA) à 60 GHz en Technologie Standard 65nm CMOS

Un amplificateur à faible bruit (LNA) à 60 GHz en technologie 65nm CMOS de ST-Microelectronics a été conçu au sein du laboratoire IMS (Laboratoire de l'Intégration du Matériau au Système) avec siège à Bordeaux (France), et présenté en [OP13].

Une nouvelle technique d'adaptation d'entrée basée sur l'utilisation d'un transformateur a été mise au point. Le primaire, de ce transformateur, est en serie avec la grille du transistor d'entrée du cascode, le secondaire est relié au drain de ce dernier. Cette approche permet de s'affranchir de la technique traditionelle de degenerescence inductive, limitant fortment le gain dans le domaine mm-waves.

Il a été développé un modèle du transistor dans le simulateur ADS de Agilent™ pour analyser l'effet des parasites sur les caracteristiques du LNA. Après avoir dimensionné les composants, un transformateur intégré a été dessiné avec le simulateur électromagnétique 3D HFSS de Ansoft™. Le LNA final comporte deux étages. Les simulations post-layout montrent un gain de 10.02 dB à 60 GHz, et un coefficient de réflexion en entrée de -16.84 dB à 61.45 GHz. Pour minimiser l'effet des pad des inductances ont été insérées pour résonner avec la capacité du pad a 60 GHz. Lors de mesures, il s'est avéré que la resonnance du couple pad/inductance masque le comportement du LNA en aval. Nous n'avons donc pas pu valider les simulations post-layout et procedons actuallment à un re-design du circuit.

Abstract

The research activity carried out during this PhD consists on the design of radio-frequency integrated circuits, for ultra-wideband (UWB) and millimeter-wave systems, and covers the following topics: (i) radio-frequency integrated circuits for low-power transceivers for wireless local networks; (ii) fully integrated UWB radar for cardio-pulmonary monitoring in 90nm CMOS technology; (iii) 60-GHz low noise amplifier (LNA) in 65nm CMOS technology.

In Chapter 1 a qualitative analysis on the communication range of passive Radio-Frequency Identification Devices (RFID), and the design of a 2.4 GHz fully integrated low-power RF transceiver front-end in a low-cost 0.35 µm SiGe Bi-CMOS technology by Austriamicrosystems are reported. Furthermore, a novel fully integrated 5-6 GHz CMOS LC tank VCO designed in a 0.35 µm standard CMOS technology is presented. Particularly, the LC tanks have been implemented by introducing a new version of the CMOS Boot-Strapped Inductor (BSI) circuit. Finally, in Chapter 1 a new wide-band frequency-independent equivalent circuit single-Π model for on-chip spiral inductors is presented.

In Chapter 2 the research activity on a new system-on-a-chip radar sensor for next generation wearable wireless interfaces applied to the human health-care and safeguard is described. In detail, the feasibility study, system analysis and the results of system simulation have been reported. The main building blocks of this UWB radar have been realized in 90nm CMOS technology by ST-Microelectronics. The design of the main building blocks of the UWB (3.1-10.6 GHz) radar sensor (the LNA, the monocycle pulse generator and the digitally programmable delay generator) in 90nm CMOS technology by ST-Microelectronics is reported. The test-chips have been realized and their performance have been measured. The measurement results show a good agreement with post-layout simulations.

Finally, in Chapter 3, the design of a 60-GHz LNA in 65nm bulk CMOS technology is reported. The LNA exploits a novel topology to obtain the integrated input impedance matching based on an integrated transformer. This technique does not require any inductive source (emitter) degeneration, which decreases the gain at high frequency, especially in the range of the millimeter waves.

Preface

The opportunity offered by the modern silicon technologies (the transistors of the standard 65nm CMOS technology have cut-off frequencies up to 200 GHz) allows us to realize highly miniaturized, low cost and low power systems-on-a-chip (SoaC), operating up to the millimeter waves, suitable for mass-market applications.

The research activity carried out during the PhD has been focused on the design of radio-frequency transceivers, from several GigaHertz up to the millimeter-waves, for narrow-band and ultra-wideband applications, on standard silicon technologies. All the aspects of the design, from the study of the applications, the system analyses and simulations, to the circuit design, realization and measurements have been covered.

This PhD thesis is organized in three Chapters, whose each one concerns a specific application and design investigated during the PhD research. The presentation order follows the thesis schedule. The research theme regarding the design of an ultra-wideband (UWB) radar for cardio-pulmonary monitoring in 90nm CMOS technology, described in Chapter 2, has interested most of the research period.

The rising interest in low-data rate applications, such as Radio-Frequency Identification Devices (RFID) and wireless sensor networks, has increased the demand of low-cost and low-power wireless devices. On the other side, the demand for high data-rate links in spectrum regions at higher frequencies, as the 5-6 GHz band for wireless local area network (WLAN) multi-standard applications, has increased in the last years as well. Chapter 1 deals with the design of radio-frequency integrated circuits for 2.4-GHz ZigBee applications and 5-GHz WLAN applications.

In February 2002 the Federal Communications Commission (FCC) gave the permission for the marketing and operation of a new class of products incorporating ultra-wide-band (UWB) technology in the 3.1-10.6 GHz band. One of the most promising class of applications of the UWB systems consists of the medical imaging. Chapter 2 deals with the study and design of an innovative wearable wireless interface for cardio-pulmonary monitoring based on a fully integrated innovative UWB radar in 90nm CMOS technology.

In the last few years, the interest in the 60 GHz radio-frequency band has rapidly grown, since the great bandwidth available allows the implementation of very high (Gigabit/s) data-rate communication systems. Chapter 3 investigates the design of a 60-GHz Low Noise Amplifier (LNA) in a 65nm bulk CMOS technology by ST-Microelectronics, exploiting a new approach of input matching without inductive source degeneration, based on the employment of an integrated trans-

former.

The original contributions of this PhD thesis to the improvement of the state of the art are referred with the label OP (e.g. [OP1]), and reported in the List of Publications.

Contents

Chapter 1

Short-range Wireless LAN

1.1 Introduction

In the last years the interest in low-data rate applications, as radio-frequency identification devices (RFID) and wireless sensor networks has rapidly grown. As a consequence, the demand of low-cost and low-power wireless transceivers has hugely increased. On the other side, the demand for high data-rate links in spectrum regions at higher frequencies, as the 5-6 GHz band for wireless local area network (WLAN) multi-standard applications, has increased as well. In this chapter the design of some building blocks of radio-frequency transceivers for 2.4 GHz ZigBee and 5-GHz WLAN applications in 0.35µm Bi-CMOS technology by Austriamicrosystems are presented.

In order to realize portable wireless devices, a primary requirement for active transponders (tags) is the reduction of the power consumption in order to reasonably extend the battery lifetime.

After presenting the capabilities of passive and active RFID, a 2.4 GHz ultra low-power RF transceiver front-end for low data-rate wireless links compliant with IEEE 802.15.4 standard (ZigBee) [1, 2] applications designed in a low-cost 0.35µm Bi-CMOS technology is presented. The design criteria for an optimal trade-off between linearity and power consumption are reported.

Then, the design of a 5-6 GHz voltage controlled oscillator (VCO) employing a new version of the Boot-Strapped Inductor (BSI, an high-Q active inductor) is presented. Finally, a wide-band equivalent circuit single-Π model for on-chip spiral inductors employed in this design is presented.

1.2 RFID: Active vs. Passive and a Low-Power Transceiver for IEEE 802.15.4 (ZigBee) Standard

The RFID systems can be classified into two main groups: the passive and the active transponders (tags) [3]. The active RFID tags are battery assisted, whereas the passive tags are not. The passive tags draw the power supply by rectifying the incident radiofrequency (RF) power emitted by the reader device.

Passive RFID tags are very cheap, but they need to be very close to the reader. For a passive RFID tag, the maximum operating distance from the reader is limited

to a few meters because of the low power level which can be transmitted in the 2.4 GHz ISM band (4 W in the United States of America; 4 W in-building only or 0.5 W without any restriction in Europe [4]). Unlike passive tags, active tags can operate at distances up to tens of meters, making them an obliged choice for many applications.

1.2.1 Communication Range of Backscattered RFID Systems

The operating principle of a typical passive RFID system, which operates in the UHF or microwave range is shown in Fig. 1.1.

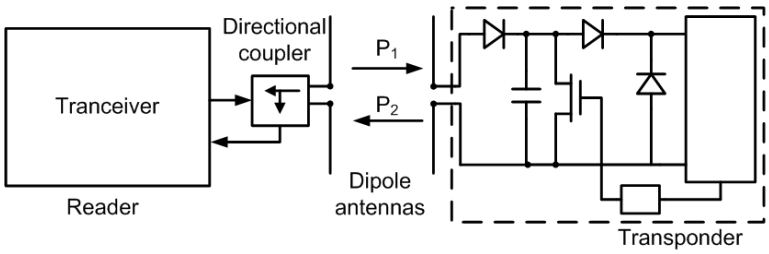

Figure 1.1: RFID backscattered system: scheme of principle.

These systems exploit the backscattering modulation. At first, the reader interrogates all the tags (transponders) in its operating range. During this time, it sends a radio-frequency signal (with power P_1) to the transponders. A part of the incident radio-frequency signal is rectified by the tag in order to obtain the power supply for its circuitry. In a second part of the communication protocol, the reader activates the communication only with the tag which corresponds to a specific code. During this time, the tag draws its power supply from a part of the energy irradiated by the reader in order to activate the tag circuitry which modulates the antenna impedance. Thus, the signal backscattered to the reader contains the information contained into the tag.

A simple theoretical model has been developed and reported in [OP1], and is herein summarized. The power density S at a distance r (range) from the antenna of the reader device is given by

$$S(r) = \frac{EIRP}{4\pi r^2} \tag{1.1}$$

where, $EIRP$ is the effective isotropic radiated power emitted by the reader. The effective area of an antenna is expressed by:

$$A_e = \frac{\lambda_0^2}{4\pi} G \tag{1.2}$$

where, λ_0 is the wavelength of the RF carrier and G is the antenna gain. An RFID system operates properly if the RF-to-DC power converted by the tag is higher or equal than its minimum power supply requirement (P_{TAG}), typically in the order

of some tens of mW. This means that,

$$P_{TAG} \leq \frac{EIRP}{4\pi r^2}\frac{\lambda_0^2}{4\pi}G_{TAG} \tag{1.3}$$

where G_{TAG} represents the antenna gain of the tag. Then, it derives that

$$r_{Reader-to-Tag} \leq \frac{\lambda_0}{4\pi}\sqrt{\frac{EIRP\ G_{TAG}}{P_{TAG}}} \tag{1.4}$$

which shows the upper limit of the communication range from the reader to the tag. In spite of that, limitations on the reverse communication path from the tag to the reader have to be considered. In fact, the RFID system operates properly if the power backscattered to the reader is higher than its sensitivity (S_{READER}), which is typically in the range from -110 to -70 dBm), according to the following expression

$$\frac{\lambda_0^2}{4\pi}G_{READER}\frac{1}{4\pi r^2}\frac{EIRP}{4\pi r^2}\frac{\lambda_0^2}{4\pi}G_{TAG} \geq S_{READER} \tag{1.5}$$

From (1.5) it results that,

$$r_{Tag-to-Reader} \leq \frac{\lambda_0}{4\pi}\sqrt[4]{\frac{EIRP\ G_{READER}\ G_{TAG}}{S_{READER}}} \tag{1.6}$$

Finally, the theoretical range of a RFID system is given by the minimum between the two ranges evaluated with (1.4) and (1.6),

$$r = \min\left\{r_{Reader-to-Tag},\, r_{Tag-to-Reader}\right\} \tag{1.7}$$

The theoretical maximum operating range versus the reader sensitivity are shown in Fig. 1.2.

These curves have been evaluated by (1.4) and (1.6), in the case of a tag operating at 2.45 GHz with P_{TAG} equal to 10 µW and G_{TAG} equal to 0 dB, and a 4 W EIRP reader with an antenna gain equal to 0 dB. To be noted that for lower values of the reader sensitivity, the maximum operating range is due to the limit introduced by (1.4), whereas for higher values of the reader sensitivity (> -75dBm) the limit is given by (1.6).

The maximum operating range of several passive transponder presented in literature have been compared with those obtained with the previously presented equations in [OP1]. The results of such comparison is shown Table 1.1. It can be noted the good agreement between the measured and the expected theoretical maximum range. However, the maximum measured range is slightly lower than that theoretical for all the cases, as we expected since the theoretical prediction does not take into account the electromagnetic complexity of the surrounding environment.

1.2.2 Low-Power Transceiver for IEEE 802.15.4 (ZigBee) Standard

A fully integrated and low-power RF transceiver has been designed in 0.35µm Bi-CMOS technology by Austriamicrosystems and presented in [OP1, OP4]. The proposed transceiver exploits a direct-conversion topology.

The direct-conversion I/Q receiver has been designed by using the available bipolar transistors in order to reduce the receiver noise figure and avoid the problems concerning the flicker noise corner frequency.

The direct up-conversion transmitter has been designed with the minimum channel-length n-MOS RF transistor. As far as the transmitter is concerned, the issue of the local oscillator pulling is mitigated by the low output power required for ZigBee applications (0 dBm).

Details on the derivation of the specifications of the receiver and the transmitters are reported in [OP1].

Receiver Design

The most widespread topology for the realization of integrated radio-frequency receivers [8, 9] on silicon is shown in Fig. 1.3. The low noise amplifier (LNA) shown in Fig. 1.3 is typically implemented by a transconductive cascode stage.

By a properly sizing of the transistor Q_1 and the inductors L_E and L_B, an almost perfect input integrated matching is realized, which allows us to simultaneously reach the maximum power transfer to the receiver and the minimum noise figure performance [10]. The input integrated matching technique imposes a constraint on the current drained by the LNA. In [11], it is shown that by adding a properly sized capacitance in parallel with C_{BE} of the transistor Q_1, then the input integrated matching can be achieved with reduced power consumption. The receiver shown in Fig. 1.3 provides a high gain, but the transconductive stage of the mixer introduces an additional non-linearity in excess to that introduced by the LNA. Thus, the increase of the linearity performance of such a receiver topol-

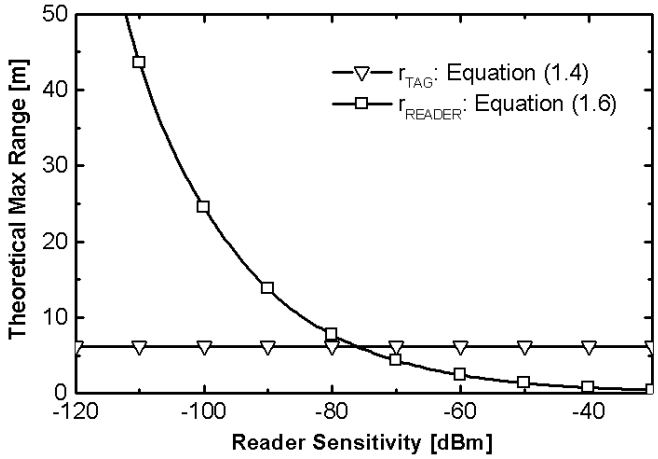

Figure 1.2: The theoretical maximum operating range vs. Reader sensitivity calculated by Equations (1.4) and (1.6), for the case of a tag operating at 2.45 GHz with P_{TAG} equal to 10 µW and G_{TAG} equal to 0 dB, and a 4 W EIRP reader with an antenna gain equal to 0 dB. The theoretical maximum operationg range is done by the minimum between the two curves.

Table 1.1: Comparison Between Experimental and Theoretical Range of Passive Tranceivers

Work	Frequency (MHz)	$EIRP$	P_{TAG} [μW]	Theoretical Range [m]	Experimental Range [m]
[5]	915	4W	16.7	12.05	9.25
[5]	2450	4W	50	2.75	2.6
[6]	915	4W	10	16.5	11
[7]	2450	4W	2.7	15	12

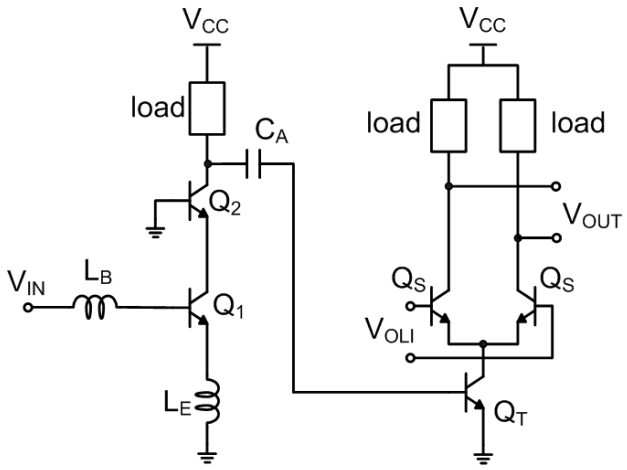

Figure 1.3: The most commonly employed receiver front-end topology. The LNA is implemented by means of an emitter degenerated cascode transconductive stage and the mixer is implemented with a typical Gilbert cell.

ogy requires an increase of the mixer bias current. A direct-conversion receiver topology [12] is proposed for the realization of a low-power receiver front-end for ZigBee based standard applications. The simplified schematic is shown in Fig. 1.4.

The LNA is implemented by means of a cascode transconductive stage. The inductances L_E and L_B realize the input integrated matching, whereas the additional capacitance C_{BE} reduces the power consumption of the LNA [11]. The LC filter resonates at the operating frequency. The small-signal current provided by the LNA flows directly into the transistor Q_3, which mirrors (according to the transistor areas ratio) its current into the transistors of the transconductive stage of the mixer (Q_I and Q_Q). Since this connection between LNA and mixer stages does not introduce ideally any non-linearity, a small bias current for the transistor Q_3 is allowed. As a consequence, R_1 is in the order of KΩ and then it does not impair the quality factor of the LC filter. In this way, the output current of the LNA can flow through the low-impedance path offered by the differential resistance of the transistor (diode) Q_3, and then into the transistors Q_I and Q_Q

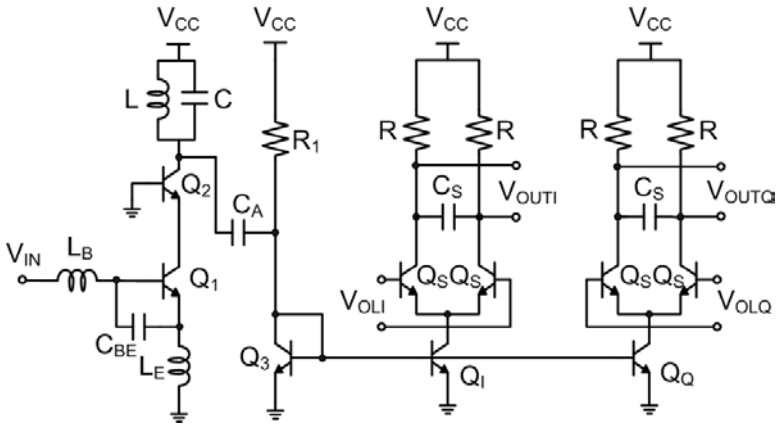

Figure 1.4: Simplified schematic of the direct down-conversion I/Q receiver front-end. The LNA output drives the two subsequent I/Q mixers by means of a current mirror, which amplifies the signal provided by the LNA without introducing significant distortions. C_A is a DC blocking capacitance.

of mixers.

To be noted that in a traditional design approach, the LC filter is not in parallel with any other components [10, 11], especially resistors, since they have a heavy impact on its quality factor degradation. Moreover, it is worth mentioning that the linearity benefits of the current mirror are well known in literature [13], but the technique is not used in the range of the radio-frequencies. In fact, in [14], it has been exploited at low frequencies for up-conversion operations. In addition, unlike the topology of Fig. 1.4, in [14] the current mirror is driven by an additional emitter follower stage, which introduces an extra degradation of the linearity performance that can be mitigated only by increasing the power consumption.

The benefits offered by the circuit of Fig. 1.4 in terms of linearity performance can be shown by a simplified circuit analysis reported hereinafter. If we consider the signal $i_{RF}(t) = i_{RFM}\cos(\omega_0 t)$ at the input of the LNA, then the small signal-current in Q_3 can be written as follows

$$i_{C3}(t) \approx \beta_{ac}\, i_{RF}(t) \tag{1.8}$$

where β_{ac} is the current gain of the LNA (in the order of ten in the radio-frequency range). The current $I_{CI}(t)$ ($I_{CQ}(t)$) into the RF trasconductive stage of the mixer is proportional to the exponential of voltage $V_{BE}(t)$, and then the small signal current is proportional to the small signal output current provided by the LNA

$$i_{CI}(t) \propto i_{C3}(t) \propto \beta_{ac}\, i_{RFM}\cos(\omega_0 t) \tag{1.9}$$

It can be noted that the non-linearities of the overall front-end are mainly due by those introduced by the LNA. Further aspects regarding the linearity have already been investigated in [15]. Moreover, the current mirror can be used as a

current amplifier as well: indeed, if k is the area ratio between the transistors Q_I (Q_Q) and Q_3, the value of i_{CI} (i_{CQ}) is k-times that of i_{C3}. Finally, for a proper design of the mixer, three parameters have been taken into account: i) the bias current I_{C30}, ii) the area of the transistor Q_3 and iii) the ratio k between the area of the transistors Q_I (Q_Q) and Q_3. In order to have a linear behaviour of Q_3, the peak value of the signal current (i_{C3M}) has to be lower than its bias current (I_{C30}). Therefore, in order to avoid current clipping (i.e. distortion), I_{C30} has to be

$$I_{C30} \geq \beta_{ac}\sqrt{\frac{P_{IN}}{2R_{IN}}} \tag{1.10}$$

where, P_{IN} is the maximum power at the input of the LNA and R_{IN} is its input impedance (resistive as in this case with the input integrated matching to the gate-source capacitance). The transistors area ratio k is chosen in order to achieve a good trade-off between the gain and power consumption. The down-conversion voltage gain (A_v) can be expressed as follows:

$$A_v = \frac{\beta_{ac}\, k \frac{2}{\pi} R}{2R_{IN}} = \frac{g_m k R}{\pi} \tag{1.11}$$

(1.11) shows that the down-conversion gain of the proposed receiver increases with higher values of k. However, a higher k causes an increasing of the mixer bias current as well. Finally, the area of Q_3 has to be set, in order to reach the best trade-off between gain and noise figure. These criteria have been applied for the case of IEEE 802.15.4 (Zigbee) standard applications at 2.45 GHz.

The circuit has been designed by using the SiGe HBTs available with the 0.35 µm Bi-CMOS process by Austriamicrosystems. The simulation results have been carried out by the SpectreRF™ circuit simulator. As for the LNA, with a bias current budget of 1.3 mA and an emitter area of Q_1 equal to 8 µm^2, it results an input referred 1-dB compression point ($\mathrm{ICP_{1dB}}$) of -20 dBm and a NFmin of 1.8 dB. C_{BE} is sized to obtain a NF very close to the NFmin with an input integrated matching to a 50Ω antenna, according to [11]. The bias current of Q_3 has been set equal to 700 µA. The current mirror gain (k) has been chosen equal to two. The voltage gain (A_V) and NF vs. the emitter length (the emitter width is fixed to 0.4 µm) are shown in Fig. 1.5.

By choosing an emitter length equal to 27 µm, a good trade-off between the NF and the voltage gain A_V equal to 26 dB (R_{load} is 400Ω, P_{AOL} is -10 dBm on a gate-source capacitance resistance of 50Ω) is obtained. The overall NF is reported in Fig. 1.6.

To be noted that the corner frequency of the flicker noise is quite lower than 10 KHz. A summary of the receiver performance and a comparison with the most representative works presented in literature are reported in Table 1.2. The solution herein reported represents one of the best performance tradeoffs between overall receiver performance and power consumption, among all those previously presented in the literature (for sake of clarity, our performance are obtained by simulations, while the performance of the other works reported in Table 1.2 are obtained by measurements).

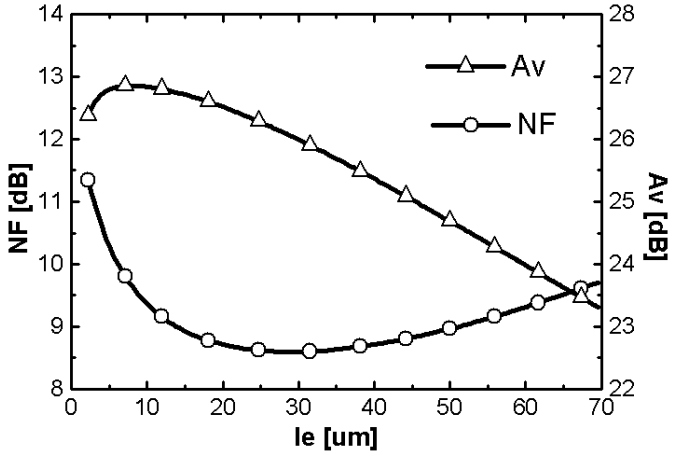

Figure 1.5: NF and A_V vs. Q_3 emitter length. The minimum of NF is obtained for an emitter length of 27 µm, with an associated A_v of 26 dB.

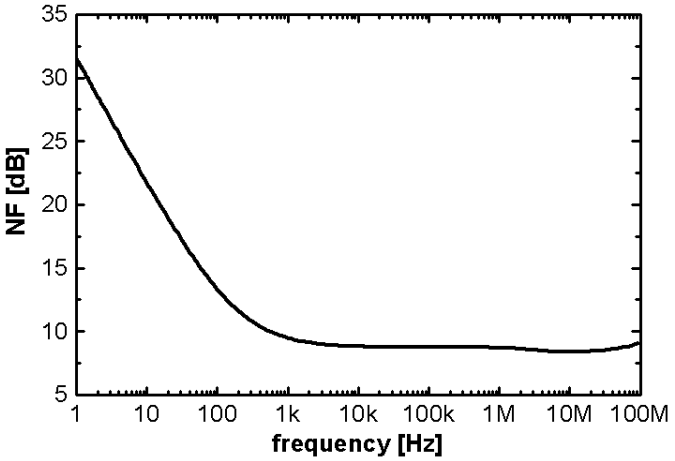

Figure 1.6: Noise Figure (NF) of the overall receiver vs. frequency.

Table 1.2: Summary of the Receiver Performance and Comparison with Previous Works

Work	Tech	V_{cc} [V]	A_v [dB]	NF [dB]	P_D [mW]	IIP_3 [dBm]
[9]	0.35µm CMOS	1	16	29	6	-18
[16]	0.25µm CMOS	2.5	50	6	10	-16
[17]	0.18µm CMOS	1.8	32	6.5	8.8	-9
[18]	0.18µm CMOS	1.8	30	-	5.4	-4
This work	SiGe*	1.8	26	8.7	8.6	-13

*0.35µm Bi-CMOS

Transmitter Design

The IEEE 802.15.4 standard states that the devices operate with a typical output power equal to 1 mW. This power is very low, so a direct up-conversion transmitter architecture may be used without suffering of local oscillator pulling. The radio-frequency carrier is modulated with a constant envelope offset QPSK modulation. This fact allows the employment of a high-efficiency non-linear amplifier, such as class-C amplifiers.

The proposed I/Q direct up-conversion transmitter consists of two double balanced mixers realized by a Gilbert cell mixer quad (I and Q channels) and a two-stage power amplifier (PA). The circuits have been designed by using the multi-finger n-MOS transistors (with the minimum channel length) of the 0.35 µm Bi-CMOS process, which, unlike the bipolar counterparts, allow us to not incur in extra dc power consumption due to the current drained from their bases. The integrated square spiral inductors and balun have been designed by means of the $2D\frac{1}{2}$ simulators (Momentum™, EM Sight™). Schematic and post-layout simulations have been carried out within Cadence Design Systems and Advanced Design System (ADS). The simplified schematic of the overall transmitter is shown in Fig. 1.7.

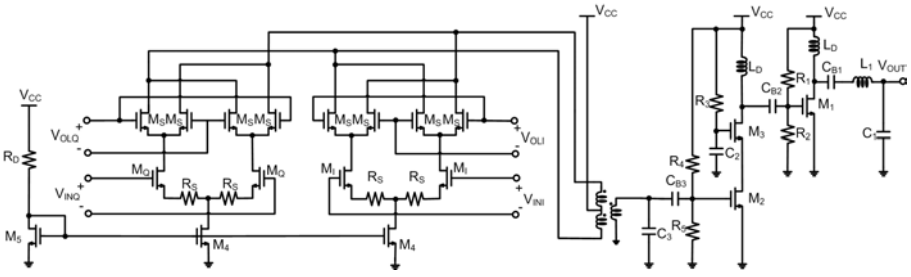

Figure 1.7: Schematic of the direct up-conversion I/Q transmitter front-end.

The power amplifier is realized by a class-A pre-amplifier (driver stage) that drives a high-efficiency class-C amplifier (power stage). The circuit has been designed in order to provide an overall output power level equal to +6 dBm, taking into account the possible reductions of performance due to the unpredictable losses caused by process parameters variations. As first design step, the class-C amplifier has been designed. For a class-C amplifier a higher efficiency can be achieved by reducing the conduction angle. On the other hand, this reduction also causes a reduction of the gain, so that a tradeoff is required. For the circuit solution herein proposed the transmitter has been designed for a conduction angle of 150 degrees, which has allowed the achievement of a good tradeoff between power efficiency and gain. Then, the optimal load impedance of the amplifier for the maximum power delivering has been found by performing a load-pull analysis both with Cadence™ and Advanced Design System™, by considering a standard gate-source capacitance impedance (50Ω) at the input of the class-C amplifier. The output matching network (L_1 is 210 pH, C_1 is 5 pF) realizes the impedance matching between the power stage and the load resistance. Large Signal S-Parameter simulations have

shown a drain efficiency (η) of 25% and a power-added efficiency (PAE) of and 22% at 6 dBm, where the drain efficiency and the power-added efficiency are defined as follows

$$\eta = \frac{P_{OUT,RF}}{P_{DC}} \tag{1.12}$$

$$PAE = \frac{P_{OUT,RF} - P_{IN}}{P_{DC}} \tag{1.13}$$

($P_{OUT,RF}$ is the power of the radio-frequency component of the output signal, P_{DC} is the DC power consumption and P_{IN} is the radio-frequency power at the input of the transmitter). The pre-amplifier has been implemented by a class-A amplifier (implemented by using a cascode stage), which allows us to properly set in a reliable way the circulation angle of the class-C. Moreover, this solution offers an almost constant input impedance, which represents a fundamental requisite for an efficient transformer-based power delivering from the output of the mixer stage [19]. The transistors of the driver stage have a gate width of 200 µm. The driver stage provides a power gain of 14 dB, an $\mathrm{ICP_{1dB}}$ nearly equal to -15 dBm and an $\mathrm{OCP_{1dB}}$ very close to 2 dBm. The circuit drains a current of 5.8 mA from a 1.8 V power supply. The input-output characteristic of the overall PA is shown in Fig. 1.8.

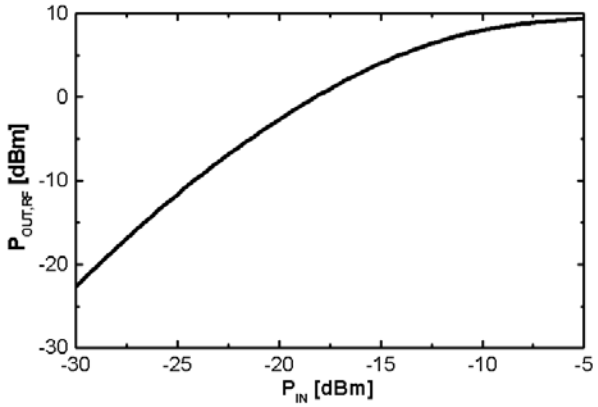

Figure 1.8: PA output power ($P_{OUT,RF}$) vs. input power (P_{IN}).

The PA provides an output power equal to +6 dBm when is driven by input power of -15 dBm supplied by the class-A driver stage. The saturation power level is nearly equal to +9 dBm. The overall PA reaches a drain efficiency equal to 16% and a power-added efficiency of 15% at +6 dBm of output power. The power added efficiency vs. the input power is shown in Fig. 1.9.

The up-conversion mixers are implemented by two double balanced Gilbert cells. This architecture allows the reduction of the phase noise effects and the LO-to-RF leakage. Since the $\mathrm{ICP_{1dB}}$ of the driver stage is -15 dBm, then each mixer has to exhibit an $\mathrm{OCP_{1dB}}$ lower than -18 dBm (the output sum signal is

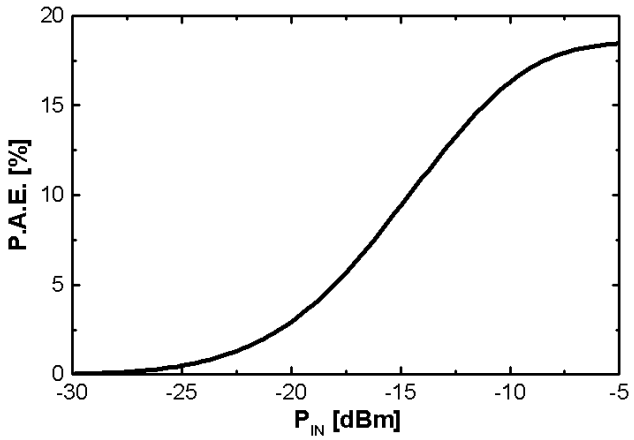

Figure 1.9: PA drain efficiency (PAE) vs. input power (P_{IN}).

3 dB higher). The I/Q differential currents provided by the mixer are collected to the input of the driver stage of the PA by means of the integrated symmetric balun. The transistors M_I and M_Q have a gate width (W) of 300 µm, whereas the transistors of the switching stages (M_S) have a width equal to 200 µm. The resistive gate-source capacitance degeneration (R_S) has been introduced in order to properly fix the conversion gain of the mixers. Each mixer drains a bias current of 1.5 mA with a 1.8 V power supply. The overall transmitter provides an output power up to +6 dBm while it is driven by an input power of 18 dBm. The power consumption of the transmitter is of 16 mW on a 1.8 V power supply. The comparison with the most representative solutions presented in literature is reported in Table 1.3. To be noted that the solution herein proposed attains one of the best trade-off between the power consumption and the output power level among the previous works reported in literature (for sake of clarity, our performance are obtained by simulations, while the performance of the other works reported in Table 1.3 are obtained by measurements).

Table 1.3: Summary of the Transmitter Performance and Comparison with Previous Works

Work	Tech	V_{cc} [V]	P_{OUT} [dBm]	P_D [mW]
[16]	0.25µm CMOS	2.5	0	16
[19]	0.18µm CMOS	1.8	0	18
[20]	0.18µm CMOS	1.8	-4	17
[21]	0.18µm CMOS	1.8	3.5	14.4
This work	SiGe*	1.8	+6*	16

*corresponding to the OCP_{1dB} of the preceding drive stage

1.3 5-6 GHz LC-Active VCO for CMOS RF Transceivers

In a radio-frequency front-end, the voltage controlled oscillator generate the signals that, by using of the phase locked loop (PLL), are provided as local oscillation (LO) for the mixers. The phase noise produced by the VCO strongly affects the noise performance of the mixers [22] and then of the overall transceiver. Thus, it is very important that the VCO exhibits a phase noise as low as possible.

Fully integrated VCOs with a lower phase noise are implemented by using LC tanks resonating at the frequency of interest. However, the phase noise performance are mainly limited by the low quality factor (Q) of the LC tank [23], which is mostly impaired by the loss mechanisms in the integrated spiral inductors.

Examples of high-Q passive inductors have been presented in literature [24]. These inductors are realized by means of additional steps in the fabrication process, which cause a dramatic increase of the chip fabrication costs.

For that reason there is a strong interest in the realization of high-Q inductors by means of active equivalent circuits. Several topologies of active inductors have been presented in literature [25, 26]. However, active inductors are not free of drawbacks, such as the production of an amount of excess noise and the limited linearity.

A novel fully integrated 5-6 GHz LC tank VCO for WLAN multi-standard applications has been designed in a 0.35 µm CMOS standard process by Austriamicrosystems and presented in [OP7, OP3]. In detail, the circuit exploits a new version of the CMOS Boot-Strapped Inductor (BSI) [27], presented in [OP6], which realizes the high-Q equivalent inductors of the LC tanks, playing a key role in reaching the best phase noise (PN) performance.

1.3.1 CMOS Boot-Strapped Inductor: The New Circuit

The active circuit named Boot-Strapped Inductor (BSI) has been originally developed in silicon bipolar technology [28]. The BSI consists of an integrated transformer and a current amplifier inserted between its primary and secondary spirals. If the current amplifier circuitry is properly sized, then an increase of the equivalent inductance seen from the primary and its quality factor (boot-strap effect) can be obtained.

Recently, the BSI circuit topology has been rearranged in CMOS technology as well [29, 27]. The small signal equivalent circuit of the CMOS BSI therein reported is shown in Fig. 1.10.

If the impedance Z_{in} is purely inductive ($Z_{in}(j\omega) \approx j\omega L_{in}$), then the impedance Z_{12} (seen from the nodes 1 and 2) can be written as follows

$$Z_{12}(j\omega) = \frac{j\omega L_{in}}{1 - \omega^2 L_{in} C_{GS}} \tag{1.14}$$

Typical values of the capacitance C_{GS} of the transistors in the BSI design are in the order of several tens of femtoFarad. Therefore, the effect of C_{GS} can be neglected in (1.14) if L_{in} is lower than a specific amount (i.e. at 5-6 GHz, the effect can be neglected if Lin is lower than 10 nH). In this condition, then

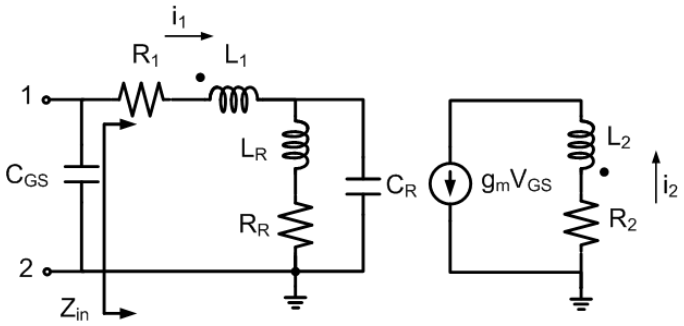

Figure 1.10: Small-signal equivalent circuit of the CMOS BSI. The inductorsL_1, L_2 and L_R are reported with their series loss resistances. g_{mc} is the total equivalent transconductance of the cascode stage (M_1 and M_2), which is mainly given by the contribution of the common gate-source capacitance stage.

$Z_{12}(j\omega) \approx Zin(j\omega) \approx j\omega L_{in}$. Then, Z_{12} can be approximately written as follows [29]

$$Z_{12}(j\omega) = \frac{(Z_P + R_1 + j\omega L_1)(1 + j\omega M\ g_{mc})}{1 + \omega^2 M^2\ g_{mc}^2} \tag{1.15}$$

where, M is the mutual inductance between L_1 and L_2, and Z_P is the parallel impedance of the inductor L_R and the capacitor C_R. At frequencies lower than the self-resonance frequency of Z_P and with proper values of g_{mc} and M, the BSI exhibits a high-Q inductive behaviour between the nodes 1 and 2.

A new version of the CMOS BSI (reported in Fig. 1.11) introduces several improvements for its efficient use in the RF CMOS design for the modern transceivers.

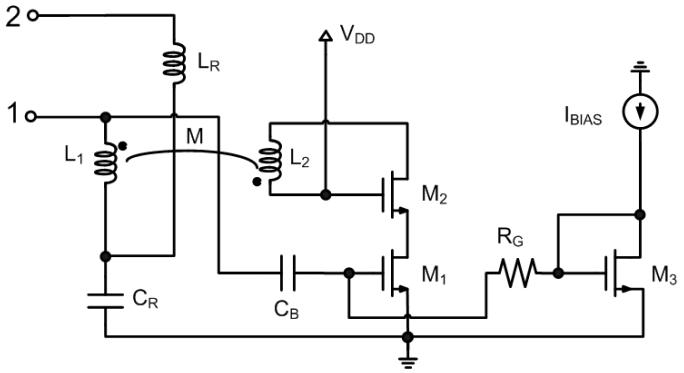

Figure 1.11: The new version of the CMOS BSI.

Unlike the BSI circuit described in [29], the DC biasing of the transistor M_1 is independent from the external circuitry connected to the nodes 1 and 2. In fact,

the placement of the inductor L_R has been changed and a DC blocking capacitor C_B (from the node 1 and the gate of M_1) has been introduced.

In detail, these changes allow us to wire the VCO to power supply without introducing additional components, which not only require additional area on die but introduce undesired parasitic effects that reduce the overall circuit performance. This makes independent the bias circuitry of the BSI from that of the rest of the circuit (e.g. the VCO core if the BSI is applied to VCO design). In this way a separate tuning of the BSI circuit performance and those of the rest of the circuit are allowed. If the reactance of the capacitor C_B can be neglected at the operating frequencies, and the node 2 is properly AC grounded, then the small signal equivalent circuit of the BSI herein presented becomes the same of that reported in [29] and shown in Fig. 1.10, so that the previous design considerations can be easily extended to the new circuit.

BSI Design

As first step, an extensive analytical description of the BSI has been derived in order to widely investigate its design space and reach an optimal circuit synthesis. This work has been reported in [OP6]. This analytic description allows us to properly size the circuit, in order to achieve the values of equivalent inductance suitable to be resonating with an integrated capacitor and simultaneously maximize its quality factor (Q). In Fig. 1.12, the Q factor of the BSI versus x ($x = \omega/\omega_R$, where $\omega_R = 1/\sqrt{L_R C_R}$) and α ($\alpha = \omega_R\ M\ g_m$) obtained by MATLAB™ simulations, is depicted.

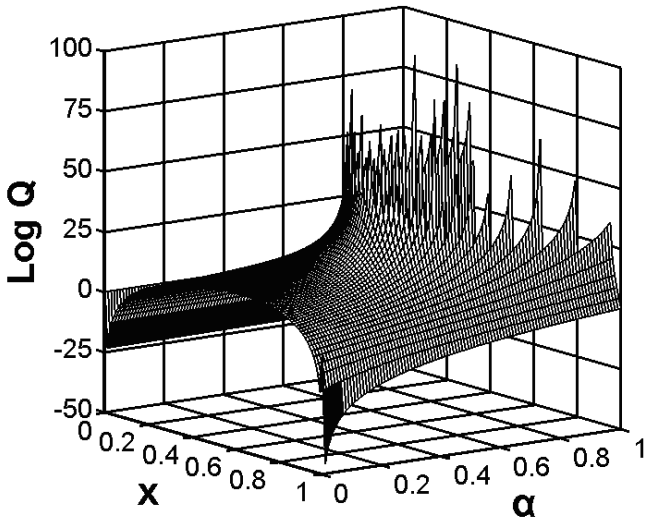

Figure 1.12: Q factor of the BSI circuit vs. x ($x = \omega/\omega_R$, where $\omega_R = 1/\sqrt{L_R C_R}$) and α ($\alpha = \omega_R\ M\ g_m$) obtained by the analytical description within MATLAB™.

The spiral inductor L_R and the integrated transformer (L_1 and L_2) have been

designed by means of 2D$\frac{1}{2}$ EM simulators (EMSight by AWR™ and Momentum by Agilent Technologies™). Then, for the 5-6 GHz case study, the quality factor of the spiral inductor L_R and the primary spiral of the integrated stacked transformer (L_1) are very close to eight, whereas that of the secondary spiral (L_2) is nearly equal to four. The mutual coupling factor (k) between the two spirals of the transformer is approximately equal to 0.88. Circuit simulations have shown a wide agreement with the mathematical description for small signals. Monte Carlo simulations have been carried out in order to evaluate the effects of the process spreading and make robust the VCO design. With α equal to 0.3 (high-Q regular region of the design space sufficiently far from the border) and a capacitance C_R of 150 fF, then the BSI provides an equivalent inductance nearly equal to 40 at 5.2 GHz. The equivalent inductance (L) and the quality factor (Q) versus frequency are reported in Fig. 1.13. The quality factor for several values of the bias current is shown in Fig. 1.14.

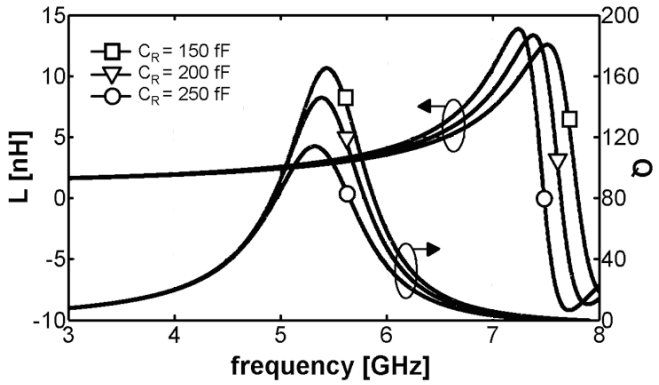

Figure 1.13: L and Q exhibited by the nodes 1 and 2 of the BSI circuit versus frequency for several values of C_R.

1.3.2 5-6 GHz BSI Based VCO Design

The most widespread 5-6 GHz WLAN standards (IEEE 802.11a [30] and HiPerLAN/2 [31]) operate in the 5.15-5.35 and 5.47-5.825 GHz frequency ranges . The BSI circuits adopted in the VCO design have exhibited a quality factor Q higher than 25 and inductance values lower than 3.5 nH over the all frequency range of interest.

Two solutions of BSI-based VCO have been designed. The former (namely, "L-tunable"), in which the capacitors C_R of the BSIs have been replaced by n-MOS varactors in order to vary the equivalent inductance exhibited by the BSI. The latter (namely, "C-tunable"), in which the capacitance of the LC tanks (C) has been replaced by n-MOS varactors. Both solutions have exhibited similar performance. The C-tunable solution is hereinafter reported and discussed. The schematic of the VCO is shown in Fig. 1.15.

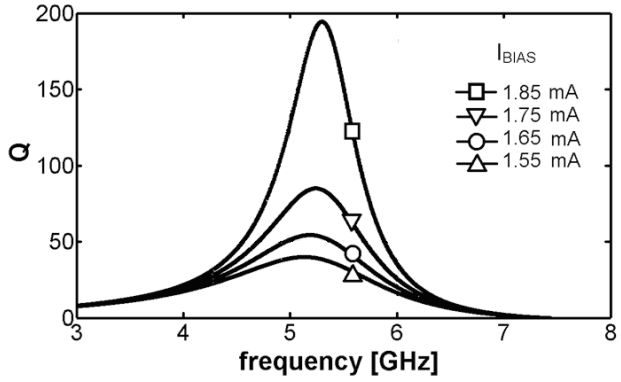

Figure 1.14: The Q-factor of the BSI versus frequency for several bias currents.

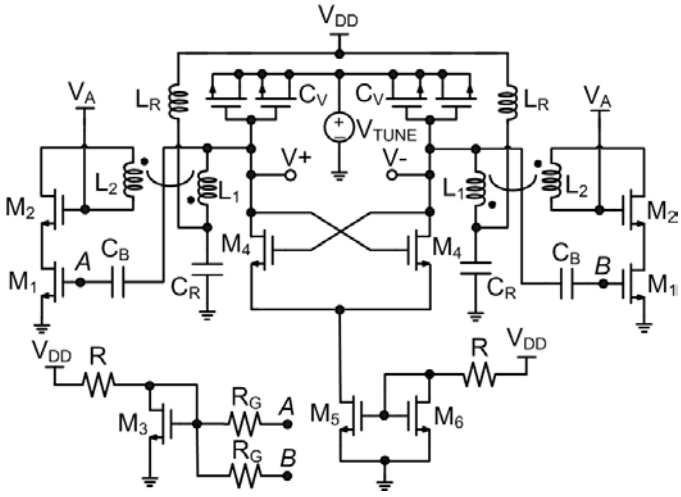

Figure 1.15: Simplified schematic of the BSI-based VCO. $V_A = V_{DD} = 1.8$V.

The n-MOS transistors (M_1 and M_2) of the BSIs have been sized with a gate width of 150 µm and 180 µm, respectively. The capacitance C_R of the BSIs is equal to 150 fF. The spiral inductors L_1, L_2, L_R are equal to 0.65 nH. Post-layout simulations have shown that the higher the bias current in the cascode stage of the BSI, the higher Q for the equivalent inductor is achieved (see Fig. 1.14). The specifications in terms of phase noise (-110 dBc/Hz at 1 MHz of frequency offset [32]) has been widely satisfied with a biasing current of the cascode stage of the BSI equal to 1.55 mA, which allows us to achieve a relevant power saving. Circuit simulations have shown an input equivalent noise power spectral density (between the nodes 1 and 2 of the BSI) lower than 2.4 $\mathrm{aV}^2/\mathrm{Hz}$ over the all frequency range, as reported in Fig. 1.16.

The transistors of the VCO core (M_4) have been sized with a total gate width of

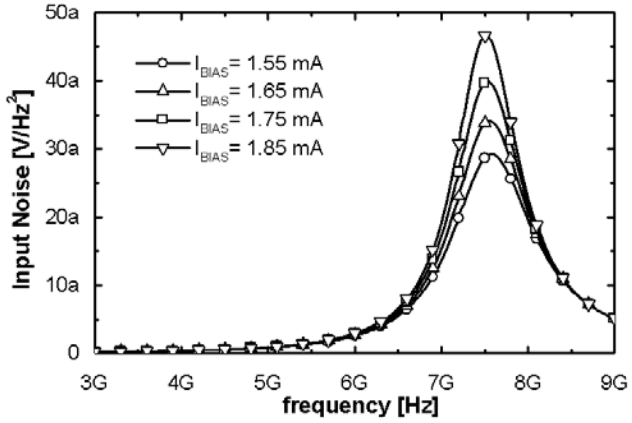

Figure 1.16: Squared equivalent input noise of the BSI used in the VCO.

20 µm and biased with 1.9 mA, with a 1.8 V power supply. Each varactor consists of two n-MOS transistors with a gate width of 130 µm, in order to provide a total equivalent capacitance resonating with the equivalent inductance of the BSI (2.86 nH) at 5.4 GHz. The power consumption (P_C) of the overall circuit (VCO core, BSIs and biasing circuitry) is 15.1 mW. The VCO provides an oscillation in the frequency range from 4.91 up to 5.93 GHz (which is wider than that required for direct-conversion transceivers both for IEEE 802.11a and HiPerLAN/2 standards), by acting on the control voltage V_{TUNE} (0-3 V), as reported in Fig. 1.17.

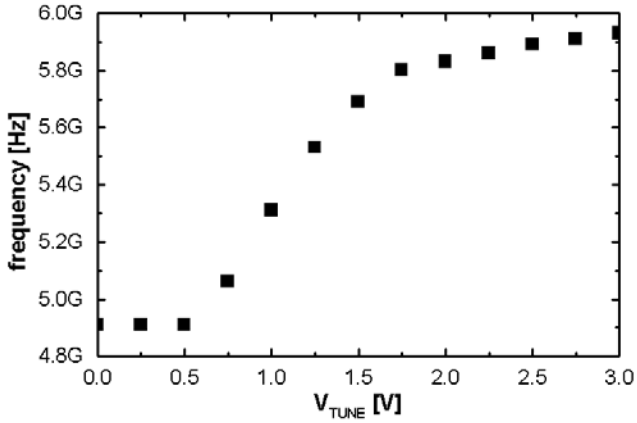

Figure 1.17: Oscillation frequency of the VCO vs. tuning voltage.

The tuning range is approximately equal to 19%. The amplitude of the oscillation is higher than 1.5 V peak-to-peak over the entire WLANs frequency range. The simulations have shown a phase noise (PN) lower than 114.9 dBc/Hz (obtained in the worst case at 5.825 GHz, whereas it is equal to -129 and -141.1 dBc/Hz at

5.4 and 5.15 GHz, respectively) at 1 MHz of frequency offset over the all frequency range. The PN obtained at the limits of the 5-GHz WLANs frequency band are reported in Fig. 1.18.

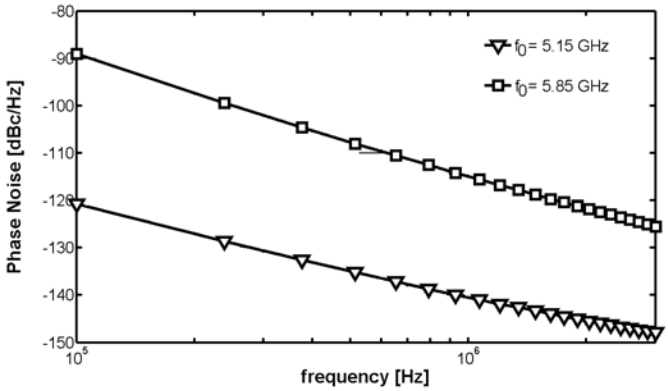

Figure 1.18: VCO Phase Noise at the limits of the overall 5-GHz WLANs frequency band.

To be noted that our VCO achieves a very good phase noise and a very high FOM [33], reported as follows

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1\mathrm{m}W}\right) \tag{1.16}$$

where $L\Delta f$ is the Phase Noise, Δf is the frequency offset, f_0 is the central frequency of oscillation and P_{DC} is the power consumption.

In detail, the achieved FOM at the central frequency is equal to 189.5 dBc/Hz at 100 KHz and 194.1 dBc/Hz at 1 MHz, which are the best results if compared with the previous works both for active [34, 35] and passive inductors and very close to those obtained in the case of VCO based on high-Q passive inductors realized with additional steps in the fabrication process [24].

1.4 Wide-Band Frequency-Independent Equivalent Circuit Model for Integrated Spiral Inductors

The quality factor and the prediction accuracy of on-chip spiral inductors considerably affect the performances of the Radio-Frequency Integrated Circuits (RFICs). For these reasons, inductors are accurately designed by using the currently widespread 2D and 3D electro-magnetic (EM) simulators (e.g. ASITIC, Momentum, HFSS, EMSight, etc.) [36, 37], which provide frequency domain descriptions in terms of S, Z and Y parameters. In a typical RF design flow, such a description is included in the circuit simulators (e.g. Cadence Design System™, Advanced Design Systems™, etc.) both for schematic and post-layout simulations. Time-domain simulators (e.g. SpectreRF™ within Cadence Design System™) are formulated to

solve sets of first-order ordinary-differential equations. However, distributed components, such as spiral inductors, are described with partial-differential equations [22]. Usually, the former are converted to a set of the latter using some form of discretization or computing the impulse response for a distributed component from its frequency-domain description. Convergence problems during periodic steady-state and transient analysis are encountered for both operations. In order to overcome these limits and reduce the computation time, frequency descriptions have to be replaced by lumped equivalent. The widespread equivalent circuit for inductor modeling is the single-Π structure shown in Fig. 1.19.

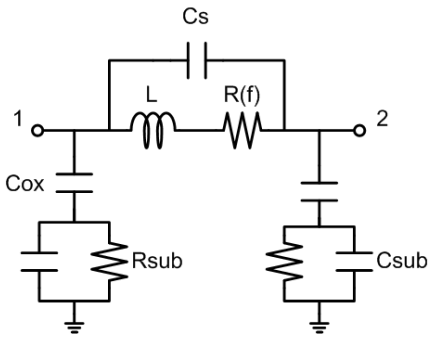

Figure 1.19: Traditional single-Π inductor model.

In this model, RLC networks are used to model the behavior of the device, taking into account the interactions between spiral and substrate [38]. This model is simple, but is not capable to provide a wideband equivalent description of the inductor [39]. To improve its effectiveness, the approach presented in [40] uses a frequency-dependent resistance $R(f)$ in order to take into account the losses in the metal conductor at high frequencies. However, nearly all simulators do not accept a frequency-dependent description for a lumped component at the graphic schematic entry level. Another very efficient inductor model can be directly derived by the inductor layout and physical process details [39]. However, accurate descriptions of the technology process parameters and geometries are necessary, but they are not always available to RF designers. In addition, it is not mentioned how to proceed in the case of spiral inductors on patterned ground shield (PGS). Moreover, if there are any information about the chip layout and only the S parameters are available (e.g. by measurements) the circuit model cannot be derived.

A new wideband equivalent circuit for integrated spiral inductors with frequency-independent lumped elements, derived from a description in terms of its S parameters obtained with EM simulations or measurements, has been developed and presented in [OP5]. In this new model, lumped element values are obtained using a fitting procedure (based on MATLAB™) instead of using the layout parameters [39, 41]. Thus, the obtained model allows us to perform both steady-state and transient analyses of time domain simulators (e.g. SpectreRF™) and can be used over a wide frequency range extended up to the inductance peak and for all the common layout geometries, with or without patterned ground shield.

1.4.1 New equivalent Wideband Circuit Model

The new circuit model for spiral inductors presented in this paper has been derived from the well-known single-Π structure shown in Fig. 1.20a.

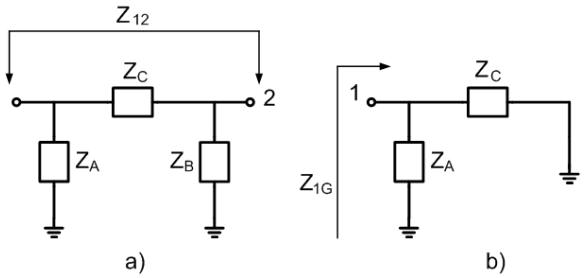

Figure 1.20: a) Generic single-π circuit; b) generic single-Pi circuit with the port 2 connected to the ground.

The impedances Z_A, Z_B, and Z_C can be derived by simulated or measured S or Y parameters of the inductor, as reported below.

$$\begin{cases} Z_A = \frac{1}{Y_{11}+Y_{12}} \\ Z_B = \frac{1}{Y_{22}+Y_{12}} \\ Z_C = -\frac{1}{Y_{12}} \end{cases} \tag{1.17}$$

The new equivalent circuit for integrated spiral inductors herein proposed is shown in Fig. 1.21.

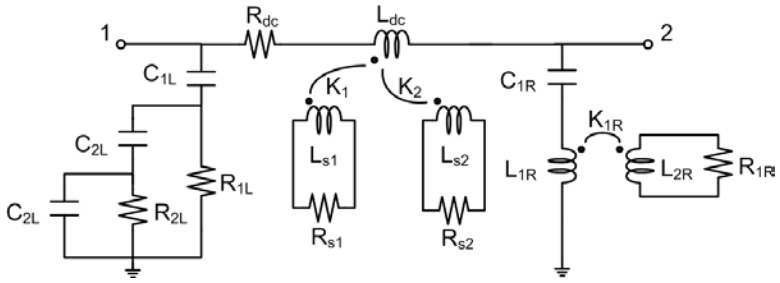

Figure 1.21: The new equivalent circuit model for spiral inductors.

With respect to the model of Fig. 1.19, Z_A includes the capacitor C_{2L} and resistance R_{2L} which allow increasing the freedom degrees for a better fitting accuracy. As far as the impedance Z_C is concerned, it uses a two loop circuit based on transformers as presented in [42]. It has been demonstrated to be capable to keep the effects of frequency-dependent losses in the spiral inductors, especially those due to the eddy current in low resistivity silicon substrates [43]. Two loops have been adopted as a trade-off between the fitting procedure accuracy and the circuit branch complexity (in terms of number of elements, as coupled mutual inductors and resistors).

Moreover, in the inductor model herein proposed the aforementioned approach [42] is adopted to fit the high frequency behavior of Z_B, as explained in [OP5].

A one-loop structure has been demonstrated to be capable to provide a good fitting accuracy. With reference to Fig. 1.21, the R_{dc} resistance allows keeping the DC behavior of the spiral inductor and its value can be extracted by EM simulations at low frequencies. To be noted that R_{dc} introduces a constraint in the fitting procedure. However, if there is not interest on DC analysis, this parameter can be removed obtaining a more simplified circuit and a better accuracy. In order to validate the effectiveness of the new model, 2D$\frac{1}{2}$ EM simulations have been carried out with Momentum™ and EMSight™ simulators on several square spiral inductors. Then, by using MATLAB™ Curve Fitting ToolBox, separate fitting procedures between the obtained simulation results for imaginary and real parts of Z_A, Z_B and Z_C and their relative literal expressions (by Mathematica™) have been performed. In this way, the values of the lumped components (C_{1L}, C_{2L}, R_{1L}, R_{2L}, R_{dc}, L_{dc}, L_{S1}, R_{S1}, K_1, L_{S2}, R_{S2}, K_2, C_{1R}, L_{1R}, K_{1R}, L_{2R}, R_{1R}) obtained from the two fitting are not univocal. Thus, a simultaneous fitting procedure for both real and imaginary part is needed.

Therefore, the aforementioned procedure with Curve Fitting ToolBox used to derive the proposed equivalent circuit model has been replaced by a MATLAB™ procedure based on the least squares method. The key factor of this new procedure is the definition of an error function (ϕ, see hereinafter) depending on the values of the circuit lumped elements, and a routine capable to simultaneously minimize the errors both on the real and the imaginary parts of the impedances (details are reported in [OP5]).

Unfortunately, ϕ consists of a polynomial expression which is not defined for a large number of values of the lumped elements. In order to avoid the sub-optimal solutions relative to local minima, a tunneling technique that allows skipping from local minima has been exploited. This technique has been efficiently implemented by exploiting an automatic searching of the global minimum solution.

1.4.2 Model Validation and Results

In order to prove the effectiveness of our equivalent circuit model, the impedance seen between the ports 1 and 2 have been calculated and compared with those directly obtained by EM simulations. Particularly, Z_{12} and Z_{1G} (see Fig. 1.20) have been considered. These impedances can be directly obtained from Y parameters, as follows:

$$\begin{cases} Z_{1G} = \frac{1}{Y_{11}} \\ Z_{12} = \frac{Y_{11}+Y_{22}+2\cdot Y_{12}}{Y_{11}\cdot Y_{22}-Y_{12}^2} \end{cases} \tag{1.18}$$

The comparison can be carried out taking directly into account the inductance value (L) and quality factor (Q), defined as follows:

$$L = \frac{Im\{Z\}}{\omega}, \quad Q = \frac{Im\{Z\}}{Re\{Z\}} \tag{1.19}$$

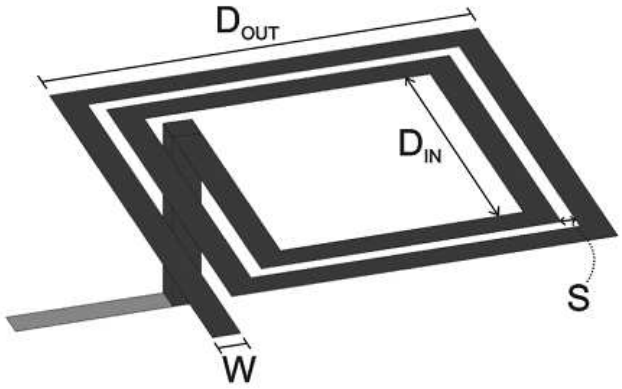

Figure 1.22: Layout (not in scale) of a square spiral inductor and its characteristic dimensions.

Several spiral inductors have been designed and modeled using the proposed approach. Particularly, a test set of six single layer square spiral inductors (see Fig. 1.22) have been designed on a standard SiGe 0.35 µm Bi-CMOS technology with four metal levels (top metal thickness of 2.5 µm).

Two different fitting procedures have been implemented. In the former, hereinafter called single-branch approach, Z_{1G} and Z_{12} have been evaluated considering the equivalent circuit obtained by a separate fitting of each branch (Z_A, Z_B, Z_C). In the latter, namely direct approach, Z_{1G} and Z_{12} have been obtained by means of a direct fitting of the overall circuit.

This approach is characterized by a short computation time and an error function ϕ with a low complexity. On the other hand, the results accuracy is acceptable but sub-optimal.

When a higher accuracy is needed, the fitting procedure can be applied directly on Z_{12} and Z_{1G} taking into account all the elements of the proposed inductor model. Thus, more variables are included in ϕ and then the computation time increases. Besides, with this approach the optimal solution (global minimum of ϕ) can not be easily achieved. Actually, ϕ contains a larger number of variables, and thus sometimes convergence problems may occur. However, this problem can be solved performing a larger number of iterations by properly setting the tunneling parameters of the automatic fitting procedure. As an example, the L and Q obtained for Z_{1G} in the case of a 1.2 nH inductor with PGS are reported in Fig. 1.23.

In this case, the mean values of percent errors obtained by the direct approach are lower than those exhibited by the single branch approach, as shown in [OP5]. The proposed equivalent circuit model provides excellent accuracy for all the test set inductors with and without PGS.

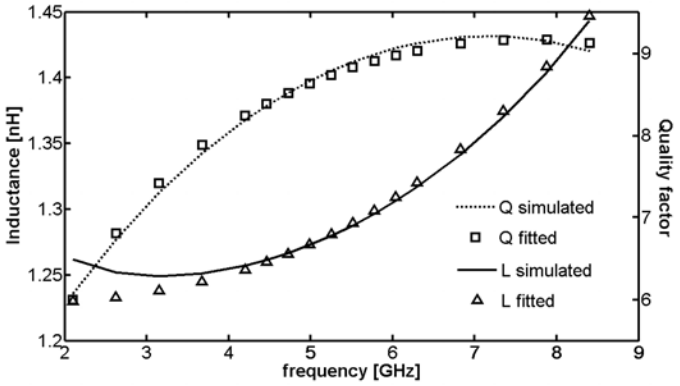

Figure 1.23: L and Q obtained by direct approach fitting.

1.5 Remarks

A theoretical evaluation of the maximum operating range of passive RFID tags has been presented and the comparison with the experimental results obtained by the solutions presented in literature has been carried out. Particularly, passive tags reach a maximum range of a few meters, which depends essentially on the power required by the tags. The maximum range ever reached experimentally is equal to 12 meters, which has been obtained with a solution realized by means of a silicon-on-sapphire CMOS process, for a power required by the tag equal to 2.7 µW and with an associated tag antenna gain of 2 dB. From this overview, it results that extending the range up to tens of meters is possible only by using active tags. RF transceivers architectures have been compared in order to drive the choice for the realization of low-power low-cost active tags solutions, in agreement with the specifications reported by the emerging IEEE 802.15.4 (ZigBee) standard. From this investigation, it derives that the direct conversion fits all the standards requirements. The design of a novel ultra low power RF transceiver suitable for RFID and wireless sensor networks applications has been presented. The transceiver front-end has been designed by using a 0.35 µm Bi-CMOS low-cost process by Austriamicrosystems. The circuits performance have been compared with those obtained with the most representative solutions in literature and represent one of the best tradeoff between output power and power consumption.

A novel fully integrated LC tunable VCO has been presented. The circuit exploits a new version of the active circuit named Boot-Strapped Inductor, which allows the realization of LC-active tanks with a high quality factor and a low noise contribution. The design space and criteria of the Boot-Strapped Inductor and VCO circuits have been widely investigated and the major results have been herein summarized. A case study for 5-6 GHz multi-standard WLAN applications has been presented, in order to verify the high potential of the presented solution, both for the exhibited performance and design reliability, and validate the design approach. The circuit has been designed in a standard 0.35 µm CMOS technology. The integrated spiral inductors and transformers of the BSIs have been designed

and optimized for the 5-6 GHz frequency range by using $2D\frac{1}{2}$ EM simulators.

The circuit model has shown an excellent agreement with the real circuit and the exhibited performance are widely compliant with the most widespread standards (IEEE 802.11a and HiPerLAN/2).

A new single-Π frequency independent equivalent circuit model for on-chip spiral inductors has been developed. The new model allows keeping the increasing losses with frequency arising for the inductors with an underneath ground pattern shield. The proposed model can be derived by S parameters without requiring any physical descriptions in terms of process cross section and layout geometry. Moreover, with respect to the previous models, the proposed equivalent circuit allows to model the integrated inductors with patterned ground shield as well.

Chapter 2

UWB Radar for Cardio-Pulmonary Monitoring

2.1 Introduction

In February 2002, the Federal Communications Commission (FCC) gave the permission for the marketing and operation of a new class of products incorporating (UWB) technology [44]. The FCC, through a modification of the 47 CRF Part 15 regulations [45], decided to allocate for the UWB systems an unlicensed band 7.5 GHz wide (for the first time, in a non-exclusive way), in the range of the radio-frequency spectrum 3.1-10.6 GHz. The mask of the maximum power spectral density (PSD) allowed for UWB devices has been set to very low values (-41.3 dBm/MHz in the 3.1-10-6 GHz band), since UWB systems have been released to operate in regions of spectrum in which other services are already operating. Asia and Europe have recently adopted similar regulations for the UWB systems in the same frequency band [46, 47].

Traditional radio-frequency wireless systems transmit information by means of one or more continuous wave (CW) modulated carriers. The base concept of UWB systems is to generate, send and receive extremely short radio-frequency pulses, with a time duration in the range of tens of picoseconds - tens of nanoseconds. For this reason, the frequency spectrum of such signals will result very wide in frequency and with an extremely low power spectral density.

UWB devices can be employed for several applications: ground penetrating radar (GPR) systems, wall and through wall imaging systems, surveillance systems, high data rate communication systems and medical imaging.

One of the most promising applications of the UWB systems consists of low-cost medical imaging. In particular, a UWB radar sensor can be employed to monitor the heart wall and chest movements, in order to detect in real time the heart and breath rates, respectively.

The recent advances in CMOS technologies (the transistors of the standard 90nm CMOS technology reach a maximum cut-off frequency higher than 150 GHz) enable the realization of the entire wireless systems on a single silicon microchip. This innovative system-on-a-chip (SoaC) device could extend the capability of the wireless body area network (WBAN), from the wireless connectivity around the

body to a new class of applications based on the radio-frequency sensing.

This chapter is focused on this opportunity to realize a novel wearable wireless sensor interface for the monitoring of the heart beat and breath rates [OP2, OP8, OP9, OP11, OP12, OP14, OP15, OP16, OP17]. In detail, the feasibility study of a UWB fully integrated radar in 90nm CMOS technology carried out by means of theoretical and CAD analysis will be reported. The main radio-frequency building blocks of the radar have been realized in 90nm CMOS technology by ST-Microelectronics and their performance have been measured. Finally, the UWB radar on a single silicon chip in 90nm CMOS technology has been designed and its layout has been sent to the foundry (ST-Microelectronics) for its realization.

2.2 Radar in Medicine

Microwave Doppler radars have been used to detect the respiration rate since 1975 [48, 49]. These first devices were bulky and expensive, but recently CMOS fully integrated versions of a radar for non-contact cardio-pulmonary monitoring have been presented [49]. Doppler radars transmit a CW signal and receive the echo reflected from the target. Such a radar system realizes the beating between the received wave and the replica of the transmitted one. The resulting signal will have a non-zero frequency if the target, which generates the echo, has a non-zero relative velocity with respect to the radar.

Another class of radar employed in the monitoring of vital parameters are pulse radars. Pulse radars operate by sending short electro-magnetic pulses and by receiving the echoes reflected by the target. The time delay between the pulse transmitted and the pulse received is proportional to the distance from the target to the radar. Examples of pulse radars for the detection of vital parameters are reported in literature [50, 51]. The principle of operation consists of sending extremely short electro-magnetic pulses towards the heart, and receiving the echo reflected at the surface of separation between the heart muscle and the blood that flows inside it, since the characteristic impedance of these two media is different.

There are great advantages from the employment of radar systems for the monitoring vital parameters with respect to the traditional methods. The radar systems allow the monitoring of the heart activity in a non-invasive and contact-less way [52], unlike the traditional techniques. For instance, the electrocardiograph requires the application of wires on the body of the person under observation, the echocardiograph requires the application of gel on the chest and should be used by an expert operator, the pulsed oximetry requires the application of sensors on the fingers or earlobes. Moreover, a radar system can monitor directly the heart wall movement, instead of its electrical activity (as the electrocardiograph), allowing the detection of those hearth diseases that do not manifest anomalies in the electrical activity (i.e. arrhythmias).

UWB transceivers present a lower complexity with respect to traditional radio-frequency systems, from a circuit implementation point of view, leading to a low-power consumption for a long life of the battery. In fact, with respect to the electrocardiograph, UWB systems does not require a stable frequency reference, which typically requires a large area on silicon die and is power hungry. Last

but not least, the extremely low level of transmitted power density (lower than -41.3 dBm/MHz) of the UWB radar should reduce the risk of molecular ionization [53, 54, 55, 56, 57, 58].

2.3 UWB radar for heart wall monitoring: system overview and operating principle

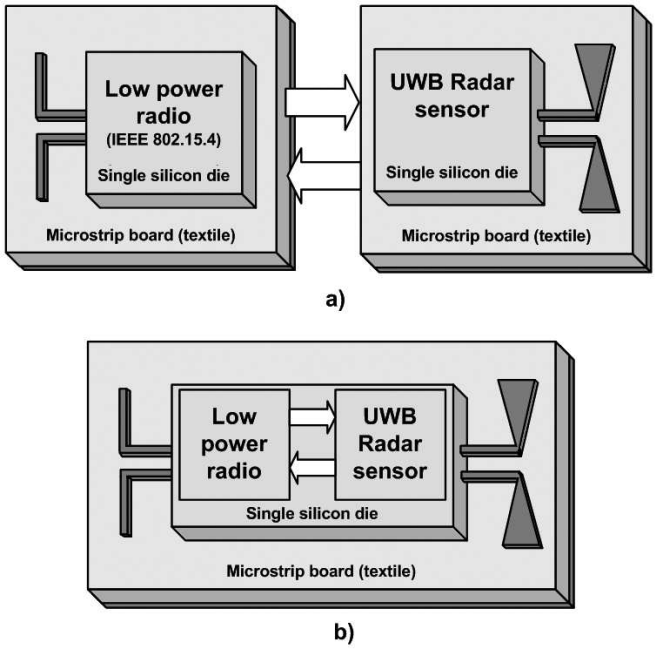

Figure 2.1: Wearable wireless radio interface for the monitoring of thecardio-pulmonary activity: a) system idea; b) future perspective: integration on a single silicon chip of both the low power ZigBee transceiver and the UWB Radar .

Given this promising contest, the realization of a wearable wireless radio interface for the monitoring of the cardio-pulmonary activity, is very interesting opportunity. For this application the miniaturization a the key factor for the realization of a wearable device. Therefore, the design of a fully integrated UWB radar for the cardio-pulmonary monitoring has been broached. The system idea is shown in Fig. 2.3. It consists of a fully integrated UWB radar sensor and low-power radio interface. The radar sensor and the low data-rate wireless transceiver will be implemented in a standard 90nm CMOS technology by ST-Microelectronics. Each antenna is realized on a microstrip substrate; however, in a most advanced realization, they can be realized directly by means of proper conductive layers tissues within clothes [59]. These interfaces will be inserted into an inner garment worn by emergency operators, as we reported in [OP12]. The data acquired by the UWB radar sensor will be transferred to a personal or remote data acquisition

and signal processing unit by means of the low-power radio data link realized by a wireless transceiver based on the IEEE 802.15.4 (ZigBee) standard. These data can be even sent directly to a medical staff, which can monitor in real time the person under observation (see Fig. 2.3). By means of the low-power transceiver the UWB radar sensor can be remotely programmed, increasing the system flexibility.

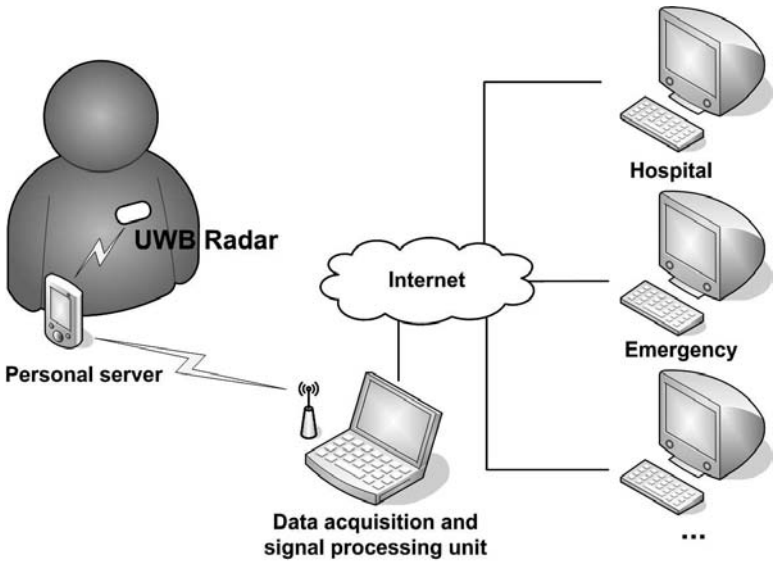

Figure 2.2: Scenary of application of the system-on-a-chip wireless sensor network interface.

The architecture adopted for the radar system is shown in Fig. 2.3.

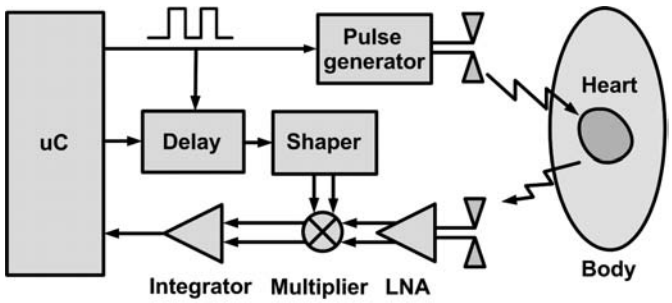

Figure 2.3: Block diagram of the fully integrated UWB radar sensor.

A correlator-based receiver has been adopted for its implementation in a modern silicon technology, since the cross-correlator has a frequency response equal to that of a matched filter. In particular, it can be demonstrated that the matched filter allows us to obtain the best signal-to-noise-ratio (SNR) at the output [60]. Preliminary simulations have shown that this topology allows us to achieve the

best performance in terms of output SNR and sensitivity to small variations of the position of the heart wall with respect to other topologies, like that in which the receiver is simply turned on by the command given by the delayed replica of the transmitted pulse [50, 51].

The operating principle of a this cross-correlator radar is explained hereinafter. The pulse generator transmits a train of extremely short (the time duration should be around 200-400 ps) electro-magnetic pulses toward the target (the heart). Since the heart muscle and the blood that flows inside have different characteristic impedance, part of the energy of the transmitted pulses is reflected at the surface of separation of these two different media [50]. A pulse repetition frequency (PRF) greater than 1 MHz allows us to consider the heart almost "motionless" between two consecutive pulses. After a time delay approximately equal to the flight time of the pulse from the transmitter to the receiver (about two nanoseconds), the echoes received from the target are multiplied with a delayed local replica of the transmitted pulses generated by the shaper block (see Fig. 2.3). If the time delay is fixed, a fixed range gate is monitored by the radar , and the amplitude of the signal at the output of the multiplier is related to the position of the heart. The output signal will reach its maximum in the case of perfect time alignment between the two signal at the input of the multiplier itself. The output signal of the multiplier is then integrated. The integrator averages a great number of pulses, in order to increase the output SNR and to have an output signal that contains the frequencies of the vital parameters under observation. Since the vital parameters vary with frequencies in the order of one Hertz, an integrator bandwidth of 100 Hz will be large enough to properly detect them. The output of the integrator will contain both the heart beat and the breath tones, since the distance radar -heart wall varies both with the heart contraction-expansion and with inspiration-expiration. Measurements with a discrete pulse radar for the heart monitoring reported in literature [51] show this fact. In spite of all, one of the most relevant task at this stage of the study consists of deriving a descriptive model of the human chest, which could allow us to carry out a complete system analysis and its verification by means of system simulation. In fact, the pulses transmitted will be strongly attenuated in the human chest and their shape will be modified since the spectral components of the signal will be attenuated differently.

2.4 Feasibility Study of the System-on-a-Chip UWB Radar for the Heart Monitoring

A complete feasibility study of the UWB radar sensor has been carried out in this doctoral research [OP2, OP9]. A theoretical model of the intra-body channel in which the electromagnetic pulse propagates has been developed. The specifications of the single blocks of the radar have been derived, by taking into account the performance achievable by means of its implementation in a standard 90nm CMOS technology by ST-Microelectronics. System simulations have been performed by means of CAD tools in order to verify the feasibility of the proposed UWB sensor radar. In particular, CAD tool system analysis has been carried out by including accurate models at different level of abstraction and non ideal effects

(noise contribution and bandwidth limitation of the building blocks) associated with the technology process.

2.4.1 Propagation Channel Model

A proper channel model has to be developed in order to carry out system analyses and system simulations. The transmitted pulses will be strongly attenuated in the human chest. Moreover, the shape of the pulse will be modified since the spectral components of the signal will be attenuated differently. In order to perform system simulations, it is also important that the channel model takes into account the variation of the time flight of the pulses from the transmitter to the receiver, due to the periodic variation of the distance radar-heart wall.

A frequency dependent model (in the band 1-12 GHz) for the loss estimation in the channel has been developed. The overall loss ($Loss$) takes into account the following contributions: i) path loss ($PL(f)$); ii) attenuation in the tissues ($Att(f)$); iii) losses due to the reflections at the interface between different tissues ($Rfl(f)$). The properties of the body tissues have been extracted by the parametric model of the dielectric properties of the body tissues developed by C. Gabriel and colleagues at the Brooks Air Force Base (U.S.A.) [61, 62]. As for the thickness of the tissues layers, the model proposed in [52], based on the Visible Human Project and the Gabriel's data book, has been considered.

Since the system-on-a-chip radar (and then its antenna) will be positioned very close to the skin in proximity of the heart region (wearable system), near field equations [63, 64] have been used in order to evaluate the path and reflection losses.

The path loss term has been estimated as follows

$$\begin{aligned} P_{RX} &= \frac{P_{TX}\ G_{TX}\ G_{RX}}{4}\left(\frac{1}{(2kr)^2}-\frac{1}{(2kr)^4}+\frac{1}{(2kr)^6}\right)= \\ &= \frac{P_{TX}\ G_{TX}\ G_{RX}}{4}\left(\left(\frac{\lambda_m(f)}{4\pi r}\right)^2-\left(\frac{\lambda_m(f)}{4\pi r}\right)^4+\left(\frac{\lambda_m(f)}{4\pi r}\right)^6\right) \end{aligned} \tag{2.1}$$

where G_{TX} is the transmitter antenna gain, G_{RX} is the receiver antenna gain, λ_m is the average wavelenght of the electromagnetic radiation in the tissues of the human chest, k is the wave number, r is the distance radar -heart, and f is the frequency. The term $2r$ takes into account the losses both in the path from the radar to the heart and the reverse path from the heart to the radar. An antenna gain equal to 1.8 (2.5 dB) has been chosen to calculate the contribution of the path loss, by referring to an antenna realized, which has been proposed in [65].

The attenuation in the tissues has been calculated as follows

$$Att(f)=\prod_{i=0}^{5}\exp\left(-\frac{2r_i}{\delta_i(f)}\right) \tag{2.2}$$

where δ_i and r_i are the penetration depth of the electromagnetic radiation and the thickness of each i^{th} tissue between the skin and the heart muscle (the index

0 refers to the air, the index 1 to the fat, the index 2 to the muscle, the index 3 to the cartilage, the index 4 to the lung and the index 5 to the heart muscle). As for (2.1), $2r_i$ takes into account the losses both in the path from the radar to the heart and the reverse path from the heart to the radar .

The loss due to the reflections ($Rfl(f)$) has been evaluated by taking into account the signal transmitted at each interface between different tissues, both in the radar-heart and the heart-radar paths ((2.3) and (2.4), respectively), and the signal reflected at the interface heart-blood (2.5).

$$\tau_1(f) = \prod_{i=0}^{4} \frac{2Z_{W,i+1}(f)}{Z_{W,i+1}(f) + Z_{W,i}(f)} \tag{2.3}$$

$$\tau_2(f) = \prod_{i=0}^{4} \frac{2Z_{W,i}(f)}{Z_{W,i+1}(f) + Z_{W,i}(f)} \tag{2.4}$$

$$\Gamma_{5,6}(f) = \frac{Z_{W6}(f) - Z_{W5}(f)}{Z_{W6}(f) + Z_{W5}(f)} \tag{2.5}$$

$$Rfl(f) = \tau_1(f)\ \Gamma_{5,6}(f)\ \tau_2(f) \tag{2.6}$$

where $Z_{W,i}$ are the wave impedances estimated for the i^{th} tissues of the human chest, as mentioned above (the index 6 refers to the blood).

Between the three loss components described above, the attenuation into the tissues results largely the most relevant, especially at high frequencies and this is due to the high conductivity of the body tissues. The overall channel loss evaluated from 1 to 12 GHz is shown in Fig. 2.4. Simulation results show that the average power loss of the pulse in the 3.1-10.6 GHz band amounts to about 80 dB.

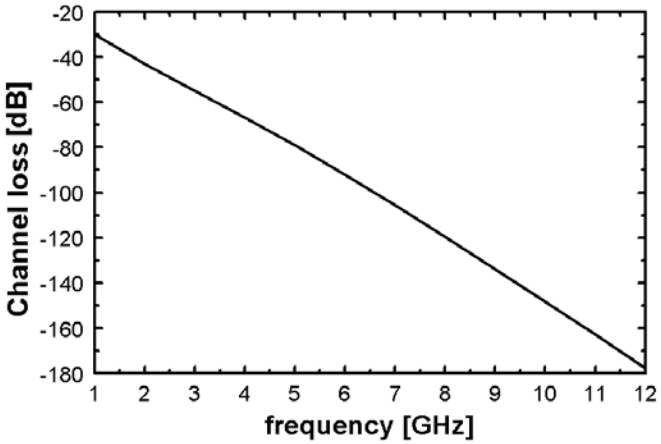

Figure 2.4: Channel loss vs. frequency of the model of intra-body channel.

As regarding the time-of-flight of the electromagnetic pulse from the radar antenna to the heart and back, it has been estimated in two nanoseconds, by

dividing the distance radar-heart by the speed of the electromagnetic radiation in the chest tissues. This value is confirmed in the literature [50, 52].

With the hypothesis that the radar is motionless, the flight time of the electromagnetic pulse varies with the position of the heart wall. In [66] it is stated that the maximum displacement of the heart (d) is 1.5 cm. This implies that the maximum time difference in the flight time (ΔT_{SMAX}) of about 470 ps, by considering the mean speed of the radiation in the tissues. Thus, the maximum difference in the time of flight of the electromagnetic pulses in the path radar-heart-radar can be estimated in a few hundred of picoseconds.

Experimental Validation of The Channel Model

The proposed channel model has been validated by experimental characterization [OP2, OP15, OP16]. To validate the theoretical channel loss model developer, a set of several antennas, each operating at a different frequency (from around 2 to 14 GHz), has been realized in order to carry out the channel loss measurements over all the frequency range of interest. The antennas have been designed by means of Momentum, the EM simulator within Agilent Technologies™, and then characterized by means of the vector network analyzer (VNA) 37369D by Anritsu™.

The experimental characterization of the intra-body losses has been carried out by means of the VNA, by placing two identical antenna, one in front of the chest of the subject under test, and the others on the back of the chest [OP2, OP15, OP16]. Each antenna irradiate towards the other antenna. The measurement setup is shown in Fig. 2.5a.

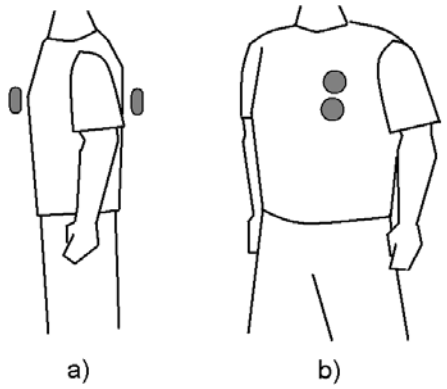

Figure 2.5: a) Placement of the antennas for the intra-body channel loss experimental characterization. b) For the theoretical model, the antennas have been considered on the same side of the chest.

The antennas are placed at one cm of distance from the skin (by means of plastic structure, which do not impair the electromagnetic behavior). Several tests have been carried out by varying the distance between the antenna and the skin,

showing that the measurement results obtained do not vary significantly for distances up to five millimeters. This results are in agreement with the measurement reported in another work [59].

A mean loss of around 78 dB in the UWB band has been measured. Since the antenna realized have a mean antenna gain of 10 dB, to calculate the real loss 20 dB have to be summed to the mean measured S_{21} parameter (10 for the transmitting antenna and 10 for the receiving antenna), leading to a mean channel loss of 98 dB. The measurement setup is different from that considered for the development of the channel model (for the model the case of a radiation crossing the tissue from the front of the chest to the heart and then to the front of the chest again has been considered), because we wanted to avoid the unwanted interaction of antennas placed on the same side. These measurement results are important to validate our model. In fact, the values of intra-body channel loss found are in agreement with a similar test reported in [67] (in [67], a mean loss in the UWB band of 109 dB is reported). Moreover, in [67], measurements of the intra-body channel between two antennas placed on the same side of the chest (see Fig. 2.5b) in the UWB band in anechoic chamber have been reported. A mean loss of 80 dB has been found, in perfect agreement with our theoretical model.

2.4.2 Theoretical System Analysis

The transmitted pulse has to be very short in order to have a range resolution in the order of the centimeter, as well as the maximum displacement of the heart. A duration time (τ) of the pulse of about 200 picoseconds allows us to achieve both the accurate range resolution and maximum of the power spectral density at 5 GHz (within the 3.1-10.6 GHz band), since the maximum of the frequency spectrum of a gaussian monocycle pulse is placed at the frequency $1/\tau$.

The gaussian monocycle has been preferred to the gaussian pulse because it has not a dc component and its spectrum fits well the FCC emission level mask. Moreover, the gaussian monocycle pulse can be implemented with an integrated differential transmitter [68]. By considering that the radar will be realized in a standard 90nm CMOS technology by ST-Microelectronics, which is characterized by a power supply of 1.2 V, the peak-to-peak voltage of the pulse has been chosen equal to 1.2 V (the theoretical maximum peak-to-peak voltage of the pulse generated by the differential transmitter is twice the supply voltage, without considering the voltage drops in the transistors).

As for the receiver, the minimum power (S_{min}) of a received signal, for a given SNR (SNR_{out}) at the output of the receiver, can be estimated by means of the following equation

$$S_{min} = k\ T\ B\ NF\ SNR_{out} \tag{2.7}$$

where k is the Boltzmann's constant (1.38×10^{-23}), T is the equivalent temperature of the antenna, NF is the receiver noise figure, B is the bandwidth of the receiver and SNR_{out} is the signal-to-noise ratio at the output of the receiver. Considering an average channel loss equal to 80 dB in the 3.1-10.6 GHz band, a noise figure lower than -11.5 dB would be required in order to have an output SNR greater than 10 dB (for a single pulse).

This result is clearly not reachable in practice, so that an improvement is required. The increase of the output SNR of the radar receiver can be obtained by integrating several pulse received [69]. The charateristic frequencies of the vital parameters under observation are within a few Hertz, then an integrator band of 100 Hz is wide enough to keep properly the heart and breath rates. The case of an integrator with a bandwidth of 1 KHz and a PRF in the range of 1-10 MHz have been investigated. For a PRF equal to 10 MHz, 10000 pulses at a time are averaged. In particular, an integration over 10000 pulses allows an improvement of the SNR (SNR_{imp}) at the output of the receiver of about 40 dB, as shown in [69] (tables are therein). This result is confirmed by the rough estimation given by the following equation

$$SNR_{imp} \approx 10 \ \log\left(\frac{PRF}{B_{int}}\right) = +40 \ \text{dB} \tag{2.8}$$

where B_{int} is the band of the integrator. The receiver front-end (LNA and multiplier) specifications are thus relaxed by the integration of a great number of pulses. In these conditions the noise figure of the receiver front-end has to be lower than

$$NF_{max} = -11.5 + 40 = 28.5 \ \text{dB} \tag{2.9}$$

This specific of NF for the receiver is achievable very easily by an implementation in a standard 90nm CMOS technology. For the system simulations (described in the next Subsection) the following specifications have been considered, by taking into account the opportunity of the 90nm CMOS technology. The specifications have been set in a power gain of 15 dB and a noise figure of 5 dB for the LNA, whereas in a voltage gain of 0 dB and a noise figure of 10 dB for the multiplier. With these specifications, the noise figure of the overall receiver front-end will result largely lower than the maximum NF allowed for a proper detection.

By considering this framework, a large integrator voltage gain is required. In fact, the dc component of the signal at the output of the multiplier, in the case of perfect time alignment between the signal received and the replica delayed of the transmitted pulse, has been estimated in a few hundreds of nano-Volts. An integrator gain of 120 dB has been considered for the system simulations, in order to have an amplitude voltage of a few hundreds of milli-Volts at the integrator output [OP2, OP9].

2.4.3 CAD System Simulations

The first-order theoretical analysis represents the first step but this does not take into consideration secondary, but non negligible, aspects mainly related with the technology issues. For this reason, the overall radar system has been implemented and simulated by means of the Ptolemy simulator within the CAD tool ADS2005A™ by Agilent Technologies™. The Ptolemy simulator allows to simulate the UWB radar in the time domain. Each block of the overall radar system has been implemented in the simulator by functional blocks, which take into account their bandwidth limitations and noise contributions. The Ptolemy simulator also

allows the co-simulation of different blocks (schematics, S-parameter files, MATLAB™ files, et al.), thus when the building blocks are realized their measured performance can be inserted in the worksheet in order to make a more realistic system simulation.

The channel model (of the human chest) has been implemented by a frequency dependent loss block, and an additional block realizing a variable (periodic) flight-time to emulate the movement of the heart wall (see Fig. 2.6).

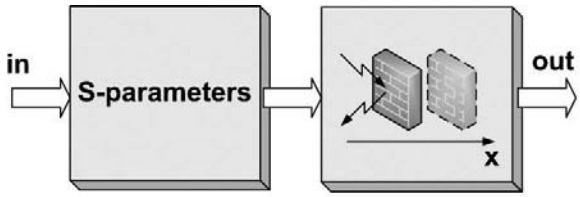

Figure 2.6: Simplified block diagram of the channel model implemented in ADS2005A. It consist of a S-parameter file (1-12 GHz) and a variable delay block that simulate two different position of the heart-wall with respect to the radar .

In particular, the first block consists of a set of S-parameters which provides a behavior in terms of frequency response equivalent to the theoretical channel model presented in the previous Section. The second block emulates a two-position heart-wall by providing a difference of 470 picoseconds in the arrival time of the signal received for the two positions.

For sake of clarity, the wall moving period has been set in 20 milliseconds (that is faster than the period of the heart beat; the time has been compressed with respect to the real heart moving in order to reduce the simulation time and alleviate the computational hardware resources). Moreover, an additional noise source (white thermal noise) has been included in the channel in order to take into account the antenna noise at the input of the receiver. Both the antennas of the transmitter and receiver have been implemented in the simulator by means of a 7.5 GHz band filter (centered at 6.85 GHz, with a slope of -20 dB/dec). The LNA block has a band of 3.1-10.6 GHz and an out-band slope of the frequency response equal to -20 dB/dec.

A two-step simulation has been carried out, because of the extremely different time constants of the radio-frequency and the base-band parts of the radar. In fact, the radio-frequency part has to be simulated with a time-step of about one tenth of the pulse width (i.e. the duration time), whereas the base-band part require a simulation time of at least several tens of milliseconds. A time step of 10 ps has been adopted for the RF section. Simulation results have shown a good agreement with the results obtained by the theoretical system analysis. In particular, the simulations shows that the increase of the SNR from the output of the multiplier to the output of the integrator is of about 40 dB, as predicted by the theoretical system analysis. The PSD of a train of pulses with duration time of 200 ps and 1.2 Volt peak-to-peak pulses with a PRF equal to 1 MHz, at the input and output of an antenna filter, are shown in Fig. 2.7, with the FCC mask for the UWB medical imaging applications.

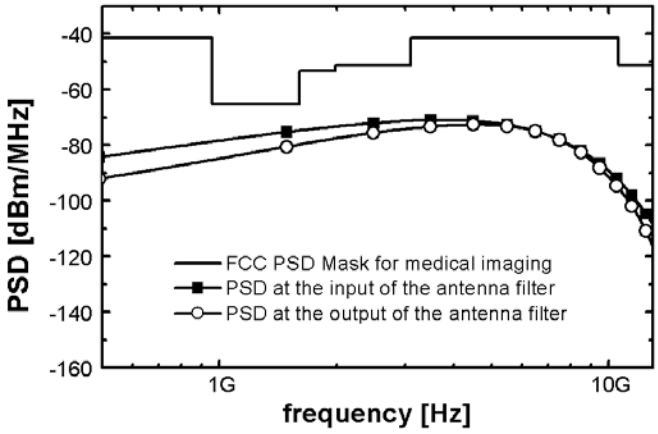

Figure 2.7: Power Spectral Densitiy (PSD) of a train of gaussian monocycle pulses of 200 ps and 1.2 Volts peak-to-peak, with a PRF of 1 MHz, both at the input and output of the transmitter antenna filter.

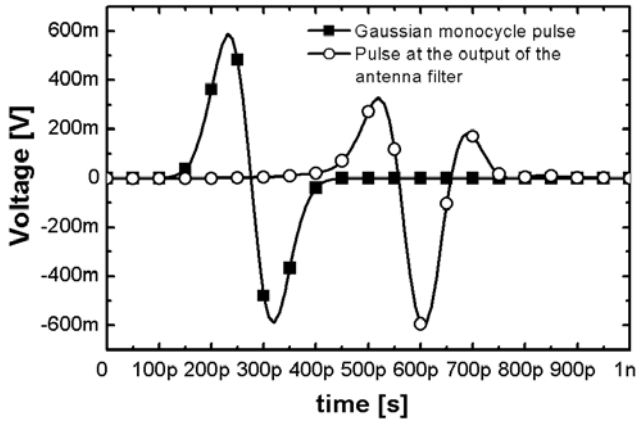

Figure 2.8: A 1.2-V peak-to-peak gaussian monocycle pulse at the input of the transmitter antenna filter, and the pulse at the output of the filter.

The 1.2-V peak-to-peak gaussian monocycle pulse at the input of the transmitter antenna filter, and the pulse obtained at the output of the antenna filter, are shown in Fig. 2.8.

The pulse at the input of the receiver (at the output of the antenna filter of the receiver), in presence of noise, is shown in Fig. 2.9. The received pulse results to be distorted strongly by the human chest (i.e. the S-parameter block), in particular it stretched out because the higher frequencies are attenuated mostly. The output voltage of the integrator is shown in Fig. 2.10.

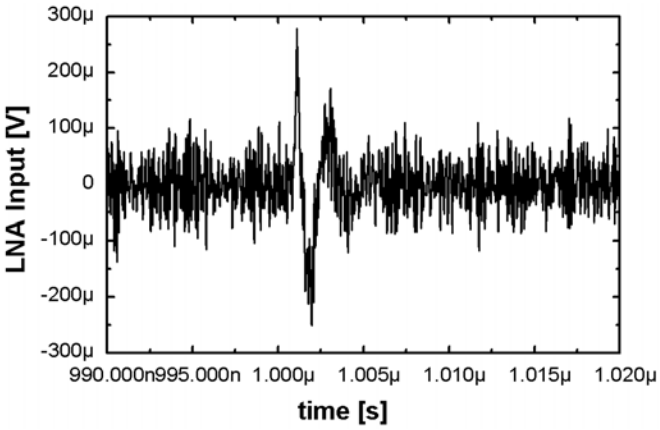

Figure 2.9: The input signal of the LNA (in presence of noise). Note that the pulse shape has been distorted strongly after the human-chest crossing.

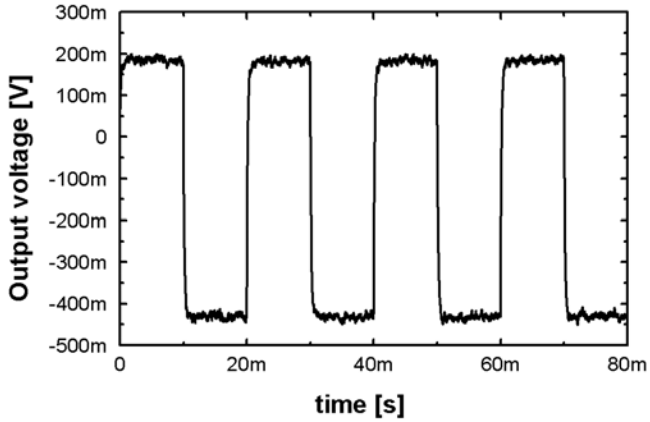

Figure 2.10: Output voltage of the integrator. A heart movement having a period of 20 mS has been considered (the time has been compressed with respect to the real heart moving in order to reduce the simulation time. This does not impair the analysis since the radar reaches the steady state widely within ten milli-seconds).

2.5 Building Blocks in 90nm CMOS technology

The main radio-frequency building blocks of the system-on-a-chip UWB radar have been then realized stand alone in 90nm CMOS technology by ST-Microelectronics. In detail, the low-noise amplifier, the monocycle pulse generator and the delay generator have been designed in 90nm CMOS technology by ST-Microelectronics, using Cadence Design Systems™. The test-chips have been characterized with on-chip measurements and their performance are reported hereinafter.

2.5.1 UWB LNA

The simplified schematic of the UWB LNA [OP15, OP16] is shown in Fig. 2.11.

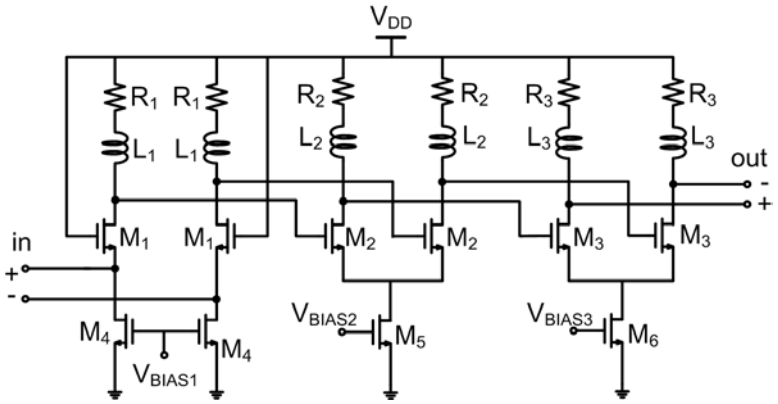

Figure 2.11: Simplified schematic of the UWB LNA.

The UWB LNA consists of three stages: a first common-gate stage, and two subsequent differential pair stages. The first common gate stage provides a wide-band input impedance matching, and the two subsequent differential pair stages provide an adequate power gain. A fully differential topology has been adopted in order to make the circuit more robust with respect to unwanted common mode signals and to allow the achievement of a wider (ideally +3 dB) output linear dynamic range. By contrast, this solution leads to double the power consumption with respect to a single-ended implementation. Because of the 1.2-V supply voltage allowed for sub-micrometer CMOS technologies, common source stages have been preferred to differential cascode stages in order to privilege the overall linearity performance. With such a choice, each stage presents only two transistors stacked from V_{DD} to ground instead of three transistors required by the differential cascode topology.

By neglecting the impedance seen from the drain of M_4 toward ground, the input impedance of the circuit of Fig. 2.11 can be roughly expressed as follows

$$Z_{in}(j\omega) = \frac{2}{g_{m1}} \frac{1}{1 + j\frac{\omega C_{gs1}}{g_{m1}}} \tag{2.10}$$

where g_{m1} and C_{gs1} are the transconductance and the gate to source capacitance of the transistor M_1, respectively, and ω is the frequency expressed in [rad/s]. The transistors M_4 in Fig. 2.11 have a non-minimum channel length in order to present a higher drain impedance.

If $\omega C_{gs1} \ll g_{m1}$, then the input impedance of the LNA shown in Fig. 2.11 becomes approximately equal to $2/g_{m1}$. For a 100Ω differential input impedance then a transconductance equal to 20 mS is required (50Ω per side).

The two subsequent stages consist of n-MOSFET two differential pair stages. In order to flatten the LNA frequency response, a resistor is inserted in series with the load inductor of each stage (i.e. R_1, R_2 and R_3).

In a first approximation, the transducer gain of the proposed UWB LNA can be expressed as reported in (2.11), which has been obtained by neglecting the gate to drain capacitance and the output conductances of the transistors

$$G_T(j\omega) \approx \frac{8R_S}{R_L}\left\{\frac{g_{m1}}{2+R_S g_{m1}} g_{m2}g_{m3}Z_{P1}(j\omega)Z_{P2}(j\omega)\left(Z_{P3}(j\omega) \parallel R_L\right)\right\}^2 \quad (2.11)$$

where R_S is the source impedance of the LNA, R_L is the output load resistance, and Z_{P1}, Z_{P2} and Z_{P3} are expressed as follows

$$Z_{P1}(j\omega) = (R_1 + j\omega L_1) \parallel \frac{1}{j\omega\left(C_{d1} + C_{gs2}\right)} \quad (2.12)$$

$$Z_{P2}(j\omega) = (R_2 + j\omega L_2) \parallel \frac{1}{j\omega\left(C_{d2} + C_{gs3}\right)} \quad (2.13)$$

$$Z_{P3}(j\omega) = (R_3 + j\omega L_3) \parallel \frac{1}{j\omega C_{d3}} \quad (2.14)$$

where C_{d1}, C_{d2} and C_{d3} are the capacitances seen from the drain of the transistors M_1, M_2 and M_3, respectively. The LNA frequency response is shaped by the impedances Z_{P1}, Z_{P2} and Z_{P3}. All these impedances can be written in the following form

$$Z(j\omega) = R\frac{1 + j\omega\frac{L}{R}}{1 + j\omega RC - \omega^2 LC} \quad (2.15)$$

Then, R, L and C allow us to shape properly the frequency response, in accordance with the requirements of the specific application. The series resistance R allows the bandwidth enhancement to the detriment of the peak of $|Z(j\omega)|$: the lower R, the narrower the bandwidth and the higher the resonance peak. The details of the LNA sizing are reported in Table 2.1.

Table 2.1: LNA Devices Sizing

MOSFET	L(µm)	W(µm)	R,L,C	Value
M_1	0.1	40	R_1	80 Ω
M_2, M_3	0.1	100	R_2	35 Ω
M_4	0.5	20	R_3	10 Ω
M_5, M_6	0.3	30× 2	L_1, L_2	2.2 nH
			L_3	2.5 nH

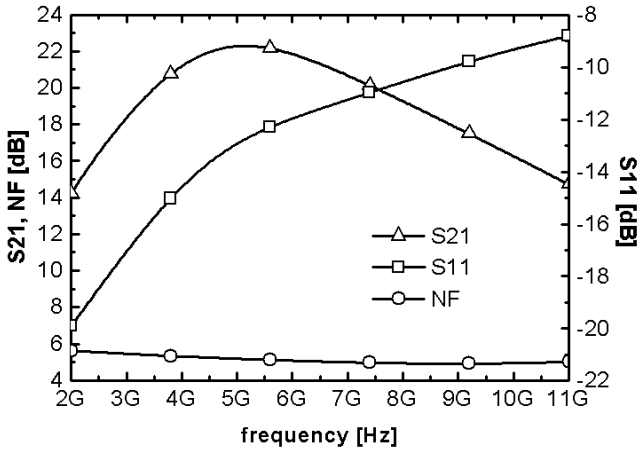

Figure 2.12: S_{21}, S_{11} and noise figure (NF) of the UWB LNA, obtained by PLS and including the input pads effects.

Post-Layout Simulations

Post-layout simulation (PLS) results, obtained by including the input pads effects only are shown in Fig. 2.12.

The effects of the output pads have been not considered since in the SoaC radar the LNA will be connected directly on-chip to the input of the subsequent wideband analog multiplier.

System simulations of the UWB radar for the cardio-pulmonary monitoring have shown that the relevant part of the energy of the signal received (i.e. echo) is concentrated in the lower region of the UWB spectrum range (3.1-10.6 GHz) [OP2].

The LNA exhibits a peak gain of 22.3 at 5.2 GHz, a minus-three-dB band (B_{3dB}) from 3.2 to 8 GHz, a S_{11} parameter lower than 10.4 dB in the 3-dB band and lower than -9 dB over all the UWB frequency range.

Measurement Results

The micrograph of the test chip is reported in Fig. 2.13. The total area is 0.685 mm^2 (ESD protected pads included).

On-chip measurements have been carried out by using GSGSG micro-probes (Z-Probe) by Suss Microtec™ with a 100µm pitch. S-parameter measurements have been carried out by means of the vector network analyzer (VNA) 37369D by Anritsu™. UWB microstrip home-made baluns have been used to connect the 50Ω single ended ports of the VNA to the GSGSG micro-probes. The measurement setup is shown in Fig. 2.14.

If not specified differently, all the results reported hereinafter have been obtained by de-embedding only the output pads, with the method "open pad de-embedding" [70].

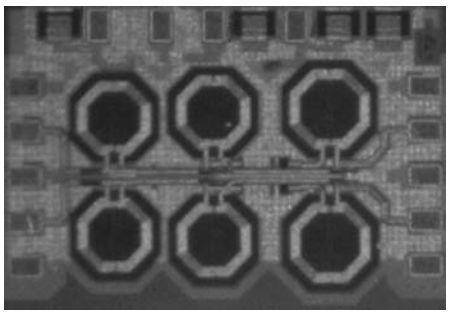

Figure 2.13: Test-chip die of the UWB LNA.

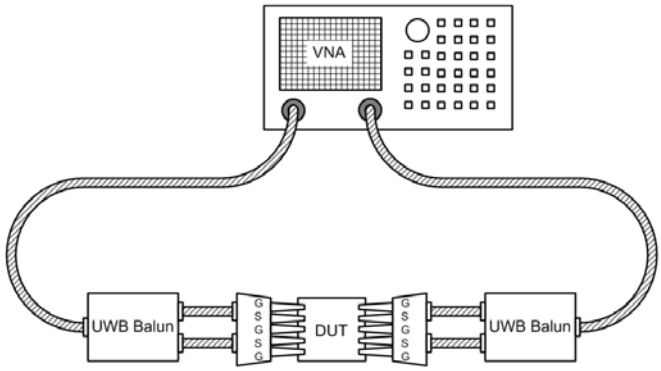

Figure 2.14: UWB LNA S-parameters of the measurement setup.

The S-parameters obtained directly from the on-chip measurement, those obtained by de-embedding the effect of the input and output pads, and those obtained by de-embedding the effect of the output only, are reported. A stand-alone GSGSG pad structure has been realized in order to measure its impedance. The measured pad capacitance is about 240 fF. The measurements obtained by de-embedding the output pads are the most relevant since in the SoC radar system the input of the LNA will be accessible to the antenna by means of the pads, whereas the output of the LNA will be connected directly on-chip to the input of the subsequent wideband analog multiplier (correlation-based radar architecture).

The S_{21} and S_{11} parameters of the LNA test-chip are shown in Fig. 2.15.

The peak gain is 22.7 dB at 5.2 GHz and the 3-dB band is between 3.56 and 8.46 GHz. It is worth mentioning that the direct measurements (i.e. without any de-embedding of the pad effects) show a peak of S_{21} of 22.58 dB at 5.16 GHz, and a 3-dB band from 3.4 to 7.9 GHz. S_{11} is lower than -10.5 dB over the all -3dB band, with a minimum equal to -16.7 dB at 3.4 GHz (S_{11} is lower than -9.33 dB over the all 3.1-10.6 GHz UWB band).

The measured S_{22} and S_{12} parameters are lower than -6.9 dB and -43 dB in the B_{3dB} (-6.5 and -43 over all the UWB band), respectively.

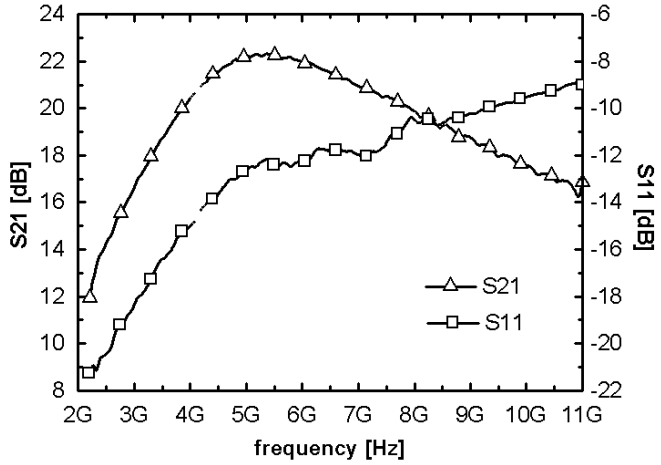

Figure 2.15: Measured S_{21} and S_{11} parameters of the UWB LNA.

The noise figure has been measured by means of the Noise Figure Analyzer N8975A with an external Smart Noise Source 4002A by Agilent Technologies™ (Fig. 2.16). The NF measured directly on the LNA test-chip (input and output pads inclusive) is reported in Fig. 2.17. It results lower than 6.5 dB over the all UWB band. This includes the noise contribution of the UWB baluns and cables, around 1 dB.

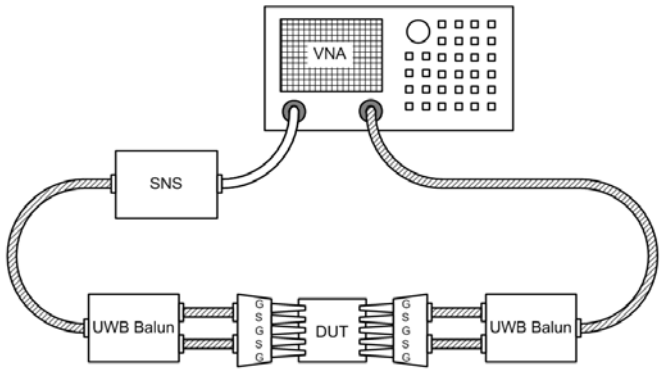

Figure 2.16: Measurement setup of the noise figure of the UWB LNA.

The overall power consumption is 34.8 mW from a 1.2-V power supply. The input-referred 1-dB compression point (ICP_{1dB}) for an input tone at the maximum gain frequency (i.e. 5.2 GHz) is -19.7 dBm, as shown in Fig. 2.18.

It can be noted that all the measured performance are in very good agreement with the PLS results.

A summary of the UWB LNA performance and the comparison with those

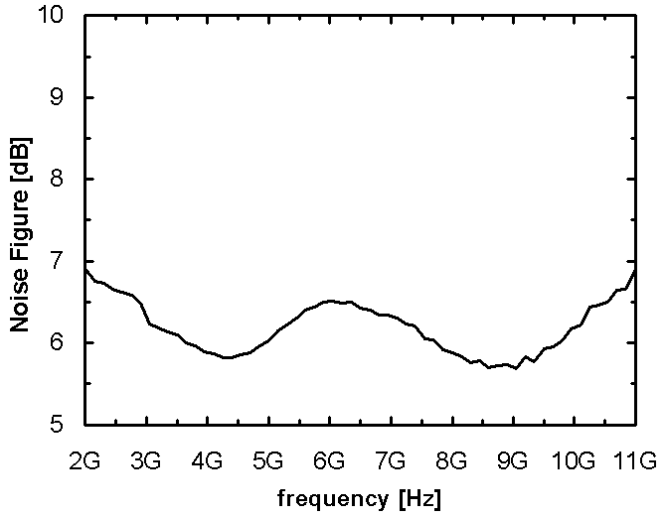

Figure 2.17: Measurement Noise Figure of the UWB LNA, including the noise contribution of the UWB baluns and cables, estimated to 1 dB.

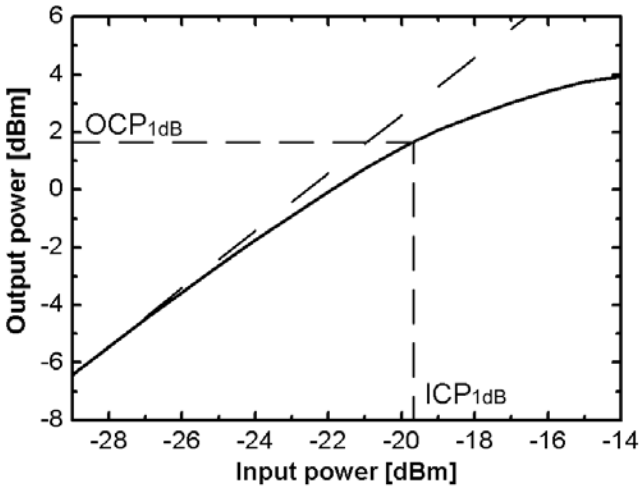

Figure 2.18: Measured CP_{1dB}. ICP_{1dB}=-19.7 dBm, OCP_{1dB}=1.88 dBm.

obtained by other relevant works in the literature are reported in Table 2.2.

It is worth mentioning that the presented UWB LNA exhibits the higher peak power gain, one of the smaller silicon area in spite of a fully differential implementation, and one of the highest linear-range output power (i.e. OCP_{1dB}).

Moreover, by considering the half of the circuit and then half of the power consumption (i.e. 17.4 mW) for a reasonable comparison with all the other solutions related with single-ended implementations, this new solution exhibits one of the

lowest power consumption.

Table 2.2: Summary of the Performance and Comparison with the State of the Art

Work	tech.	$\|S_{11}\|$ [dB]	S_{21} [dB]	B_{3dB} [GHz]	NF [dB]	ICP_{1dB} [dBm]	P_C [mW]
[71]	0.18µm CMOS	<-9.9	9.3	2.3-9.2	4	-15	9
[72]	SiGe	<-10	21	3-10	2.5-4.2	-14.7(1)	30
[73]	0.18µm CMOS	<-11	9.7	1.2-11.9	4.5-5.1(2)	-	20
[74]	0.18µm CMOS	<-5	19.1	2.8-7.2	3.8	-	32
[75]	0.18µm CMOS	<-12	8	0.1-11	2.9 dB	-	21.6
[76]	0.18µm CMOS	<-10	12.4	0.4-10	4.4-6.5	-	12.5
This work	90nm CMOS	<-10.5	22.7	3.56-8.46	<6.5(3)	-19.7(4)	34.8

(1)in 3.4-5.4 GHz; (2)in 3.1-10.6 GHz;
(3)in 3.1-10.6 GHz, including UWB baluns and cables noise; (4)at 5.2 GHz.
This work is fully differential, all the others are single ended.

2.5.2 Pulse Generator

The pulse generator herein described, and presented in [OP10, OP16], has been developed in [77]. It consists of driving a CMOS source coupled differential pair (i.e. the shaping network) by means of a triangular monocycle pulse. The block diagram of the pulse generator is shown in Fig. 2.19.

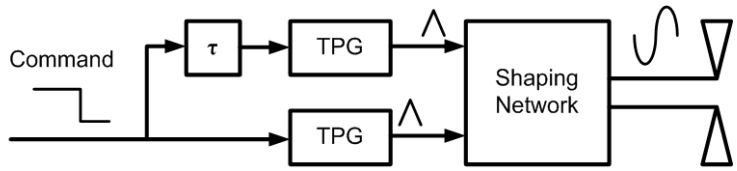

Figure 2.19: Block diagram of the novel pulse generator. TPG is the Triangular pulse generator, whereas τ is the delay block.

The circuit provides a monocycle pulse at each occurrence of the negative edge of a digital control signal provided by a microcontroller (i.e. the signal *Command*).

The triangular monocycle pulse is realized using of the combination of two triangular pulses, both obtained by two identical triangular pulse generators, of which the second one is activated after a proper delay (τ).

When the shaping network is driven by a properly large triangular monocycle, it provides a differential output voltage on the load resistance (i.e. the antenna) very close to a sinusoidal monocycle [78], in accordance with the principle of the non-linear waveform shapers.

Triangular Pulse Generator

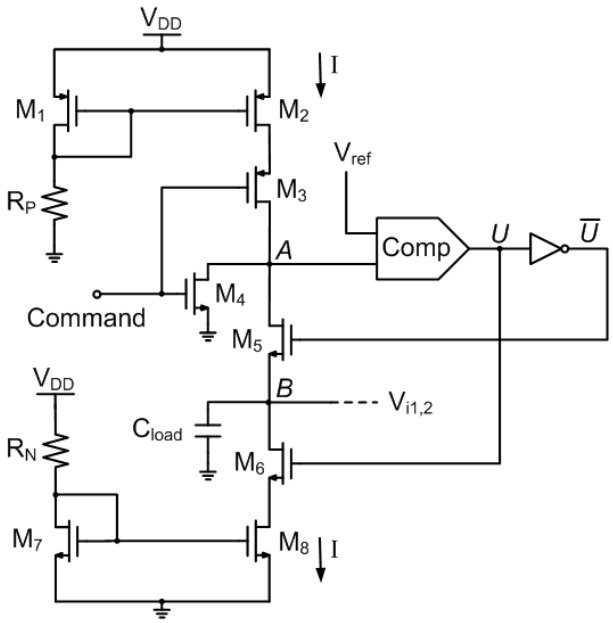

Figure 2.20: Simplified circuit of the triangular pulse generator. The triangular pulse (V_i) is provided at the node B. V_{ref} is an internal voltage reference (Reference therein [77])

.

Each triangular pulse is obtained by the network (i.e. triangular pulse generator) shown in Fig. 2.20. The command signal of the second triangular pulse generator is derived by the same command digital signal by introducing a delay time (τ) realized by means of an additional buffer properly sized.

In practice, the triangular pulse generator exploits the concept of charging and discharging a capacitor by means of a constant current. By acting on the charge current (i.e. I, see Fig. 2.20) and on the delay time τ, a triangular pulse with a variable duration time can be generated. The operating principle is detailed hereinafter.

When the negative edge of the digital signal *Command* occurs, then the transistor M_4 is switched off and the transistor M_3 is switched on. As long as the voltage at the node A is lower than V_{ref}, the output of the comparator (U) is in the low state (i. e. 0V). Thus, the transistor M_5 is on, while the transistor M_6 is off. The constant current flows through M_3 and M_5, and then into C_{load}. Thus, the voltage at the node B grows up linearly, and the voltage at the node A arises. When the voltage at the node A becomes equal to V_{ref} (i.e. the threshold voltage of the comparator), then the output of the comparator becomes high (i.e. 1.2 V), and the transistor M_5 turns off and M_6 turns on. The capacitor C_{load} begins its discharge at constant current through the transistor M_6 and the voltage at the

node B decreases, in principle, linearly until it reaches its minimum value (i.e. 0 V).

In the triangular pulse generator the comparator has been realized by means of a cascade of two CMOS inverters.

The reference voltage of the comparator is equal to $V_{DD}/2$, which has been obtained by sizing the width of the p-MOSFETs M_P as two times larger than the n-MOSFETs M_N width. The delay (i.e. τ, see Fig. 2.19) has been implemented by means of a cascade of twelve CMOS inverters (as well as those adopted in the comparator circuit). The propagation time (i.e. τ) of the delay generator is close to 125 ps (i.e. approximately equal to the relevant duration time of each triangular pulse). The two triangular pulses provided by the two identical triangular pulse generators at the inputs of the shaping network are shown in Fig. 2.21.

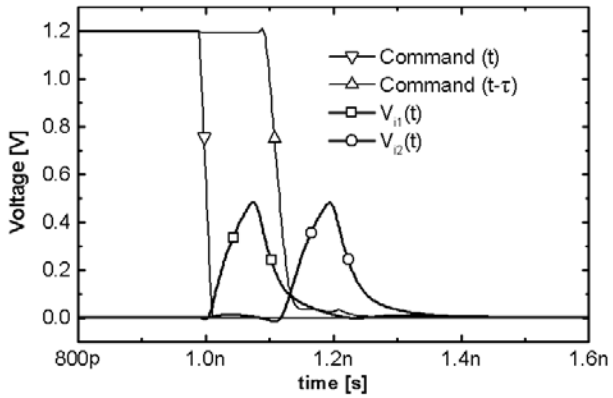

Figure 2.21: The triangular pulses provided by the two triangular pulse generators at the inputs of the shaping network (post-layout simulations). Note that they are delayed of approximately the triangular pulse time width.

The maximum value of the amplitude of the triangular pulse is close to $V_{DD}/2$. In particular, the post-layout simulations show that a triangular pulse with an amplitude of 530 mV (open load) can be obtained from a 1.2-V supply voltage.

Shaping Network

The schematic of the shaping network is shown in Fig. 2.22.

The shaping network provides a differential output voltage (on the antenna load) very close to a sinusoidal monocycle when it is driven by the triangular pulse generator.

As for the operating principle of the shaping network, the idea consists of driving the differential pair by means of a triangular pulse. Then, by the unbalance of the differential pair, the monocycle pulse is obtained on the output load (i.e. the antenna).

In detail, when the triangular pulses are not applied to the inputs of the CMOS differential pair, the voltage at the nodes C and D are at their DC level ($V_C = V_D$).

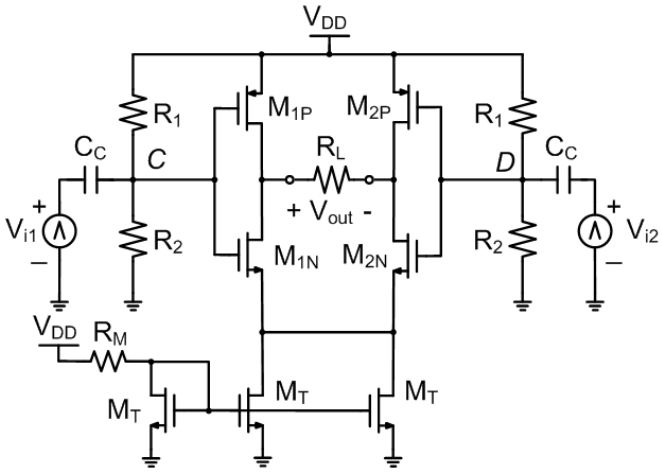

Figure 2.22: Schematic of the shaping network.

When the large triangular pulse (i.e. V_{i1}) starts to be applied to the node C (the voltage at the node D is at its DC level), then the transistors M_{2P} and M_{1N} are switched on, while M_{2N} and M_{1P} are off. During this time, the CMOS differential pair is unbalanced and the drain currents of M_{2P} and M_{1N} flow through the load R_L. When the triangular pulse V_{i1} ends (the voltage at the note C is returned at the DC level), the second large triangular pulse (i.e. $V_{i2}(t) = V_{i1}(t-\tau)$, where τ is the duration time of the triangular pulse) starts to be applied to the node D, the transistors M_{2P} and M_{1N} are off, while M_{1P} and M_{2N} are switched on, and then the drain currents of M_{1P} and M_{2N} flow through the load R_L as in the previous case but in the opposite direction.

The input voltage of the shaping network is equal to $V_{id}(t) = V_C(t) - V_D(t)$.

The trans-characteristic of the shaping network of Fig. 2.22 is very close to that of the n-MOSFETs source-coupled differential pair, in particular it results (by considering the short channel equations for the drain currents of the branches)

$$V_{out} = -R_L \Delta I_d = -R_L \frac{k'}{2} W E_{SAT} V_{id} \tag{2.16}$$

where R_L is the load resistance, ΔI_d is the current into the load, W is the n-MOSFETs width and E_{SAT} is the field strength of saturation of the carriers velocity. The p-MOSFETs width is the double of the n-MOSFETs width in order to compensate the different mobility of the electrons and holes into the channel and then to reach an almost perfect balance of the trans-characteristic.

Given the load impedance and the input and output voltage swings, two parameters have to be sized: i) the drain current and ii) the channel width of the CMOS transistors.

The output pulse amplitude is equal to $|V_{od}|_{MAX} = R_L I_{BIAS}$, where R_L represents the antenna load resistance (i.e. 100Ω). By considering the requirement

in term of pulse amplitude (i.e. 1V peak-to-peak), then the bias current required can be derived as follows

$$I_{BIAS} = \frac{|V_{od}|_{MAX}}{R_L} \approx 5 \text{ mA} \tag{2.17}$$

Thus, if a monocycle pulse of about 1V peak-to-peak (V_{pp}) is required on a 100Ω differential antenna, then the drain current has to be 5 mA. It is worth noting that the current consumption, then the power consumption, depends on the peak-to-peak amplitude required on a specific load resistance. The lower the peak-to-peak amplitude and the higher the load resistance, the lower the power consumption.

When the triangular pulse generator drives the shaping network of Fig. 2.22, the peak value of the triangular pulse (530 mV, obtained by post-layout simulations) is reduced to a value of 480 mV and the gate voltage of the CMOS transistors is unbalanced, with respect to its DC value, for a maximum value ($|V_{id}|_{MAX}$) close to 440 mV (i.e. due to the capacitive partition). $|V_{id}|_{MAX}$ is clearly a function of the width of the n-MOSFETs of the shaping network.

In order to have $|V_{id}|_{MAX} \approx 440$ mV, W_N has been sized to 60 µm and W_P to 120 µm. This choice guarantees that the triangular pulse overdrives the shaping network in spite of the spreading of the process parameters.

The monocycle pulse obtained by post-layout simulations is shown in Fig. 2.23, which is in accordance with the value predicted by (2.16). In spite of this choice of W does not consider primarely the proximity to the ideal sinusoidal monocycle, we can observe that the monocycle pulse obtained has a satisfactory sinusoidal-like shape.

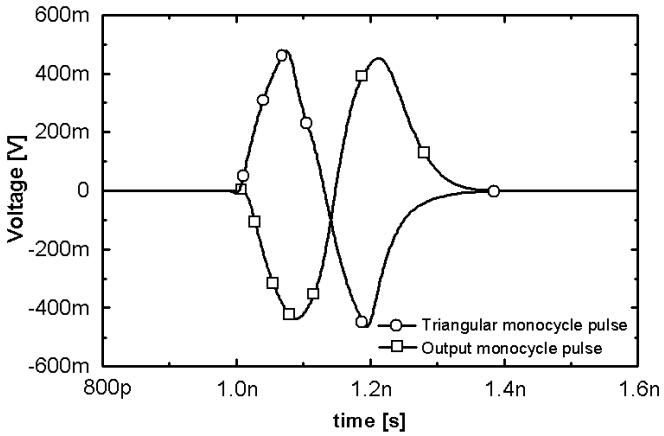

Figure 2.23: Input (triangular) and output monocycles of the shaping network, obtained by the post-layout simulations (pads inclusive).

The sequence of the pulses obtained, each at the negative edge of the signal *Command*, is shown in Fig. 2.24.

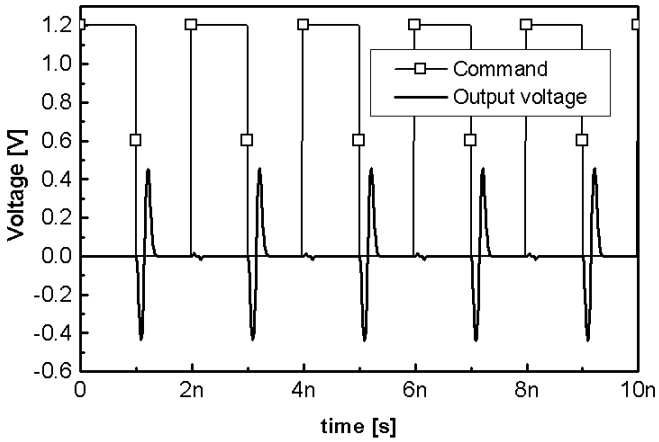

Figure 2.24: Sequence of the pulses obtained by the application of a square-wave signal *Command*.

As an additional consideration, both the triangular pulse generator and the shaping network provide monocycle pulses with a comparable peak-to-peak amplitude. However, even if they have very similar frequency spectra, only the shaping network is able to drive the antenna.

The energy of each monocycle pulse amounts approximately to 0.3 pJ.

The supply voltage is equal to 1.2 V and the total power consumption amounts to 19.8 mW.

Measurement Results

The testchip has been realized through the CMP's multi-wafer projects. The testchip micrograph is reported in Fig. 2.25.

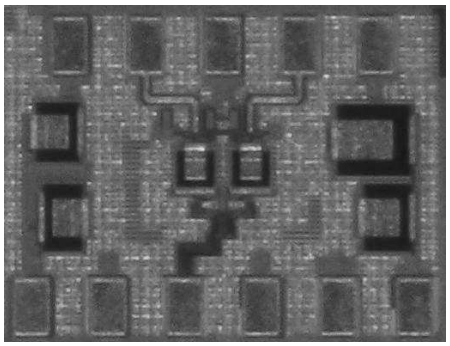

Figure 2.25: Die micrograph of the pulse generator test-chip.

The experimental characterization of the testchip has been carried out by means of on-wafer measurements, by exploiting GSGSG micro-probes with a

100µm pitch by Suss Microtec™. The scheme of principle of the measurement setup is shown in Fig. 2.26.

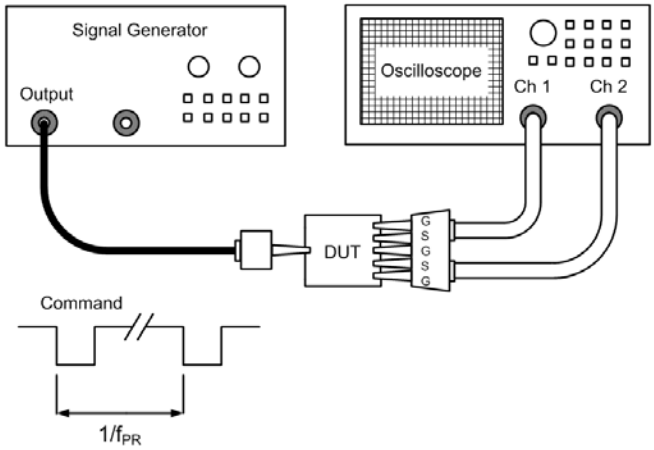

Figure 2.26: Scheme of the measurement setup of the pulse generator. The signal *Command* has a period equal to $1/f_{PR}$ where f_{PR} is the pulse repetition frequency.

The digital command signal, which activates the triangular pulse generator (then, the UWB pulse generator), consists of a square wave with an amplitude equal to 1.2V and a pulse repetion frequency (f_{PR}) from 1 to 10 MHz. This has been provided by a pulse generator HP 8082A. The output-signal of the pulse generator has been captured on two 50Ω impedance channels of a DSA (Digital Sampling Analyzer) 91304A real time oscilloscope (40 Gs/sec, 13 GHz bandwidth) by Agilent Technologies™. The pulse provided by the pulse generator is shown in Fig. 2.27.

The pulse has an amplitude peak-to-peak of about 660 mV and a relevant duration time of about 430 ps.

It can be noted that the first part of the monocycle has a longer duration time with respect to the second part of the pulse. This is due to the limited fall time of the command signal generator (the shortest available in our laboratory is 1 ns). In fact, the second part is immune from the fall time since the signal *Command* derived for the second triangular pulse generator by means of a regenerative buffer (i.e. the delay circuit, see Fig. 2.19). In principle, it is worth mentioning that the circuit does not depends dramatically from the fall time (obviously, the faster the fall time, the shorter the duration time of the first part of the monocycle), but this was quite larger with respect to that adopted during the circuit design and simulations. However, this is not a problem in the system-on-chip integration of the UWB radar, since the signal *Command* will be first buffered and then derived for both the triangular pulse generators.

The power spectral density of the measured pulse, for a pulse repetition frequency (f_{PR}) of 1 MHz, is shown in Fig. 2.28, which reports also the power spectral density of the sequence of the pulses after an ideal UWB antenna filter (i.e. a first-order band-pass 3.1-10.6 GHz Butterworth's filter).

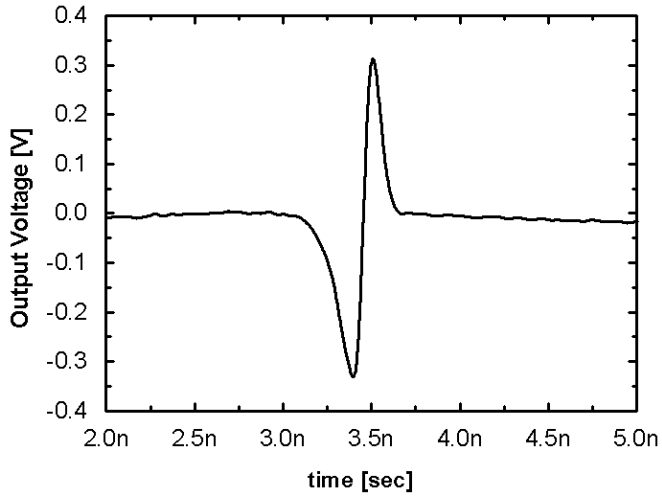

Figure 2.27: Monocycle pulse provided by the novel pulse generator. This has been measured by means of a dual-channel DSA (channel 1 - channel 2, 50-Ω input impedance each).

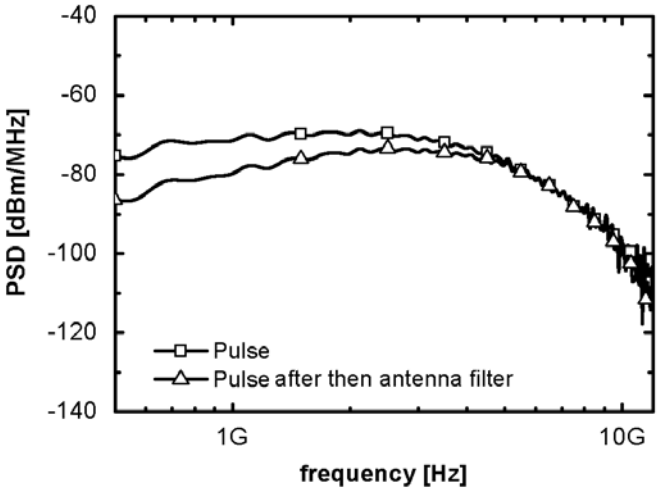

Figure 2.28: Spectrum of the measured pulse, before and after an ideal UWB antenna filter (i.e. a first-order band-pass 3.1-10.6 GHz Butterworth's filter), for a pulse repetition frequency of 1 MHz.

The measured performance are summarized in Table 2.3, which reports also the results of the state of the art.

This novel solution exhibits the widest pulse peak-to-peak amplitude (i.e. 660 mV) from the lowest supply voltage (i.e. 1.2 V), if compared with the state of the art for the monocycle pulse generators fully integrated on silicon [79, 80, 81], which

Table 2.3: Summary of Performance and Comparison with the State-of-the-Art

Work	Tech	T_D [ps]	V_{PP} [mV]	V_{DD} [V]	P_C [mW]
[79]	CMOS 0.18 µm	375	175	1.8	45
[80]	CMOS 0.35 µm	750	1.8	3.3	27.4*
[81]	CMOS 0.18 µm	460	35	1.8	21.6
Our	CMOS 90 nm	430	660	1.2	19.8

* reference therein [82]

are based on different approaches and provide Gaussian-like monocycle pulses.

2.5.3 5-bit Digitally Programmable 1-3 ns Delay Generator

The programmable delay generator [OP10, OP16] delays the negative edge of the digital signal (*Command*) that activates the pulse generator. The delay generator is digitally programmable by means of five bits, obtaining $2^5 = 32$ different delays. The design has been optimized to drive properly the capacitive input impedance (close to 40 fF) of the triangular pulse generator of the shaper block (which is the same of the pulse generator described above).

The topology proposed in [83] has been adopted, since it is very robust with respect to the spreading of the process parameters and temperature variations. The schematic of the delay generator is shown in Fig. 2.29.

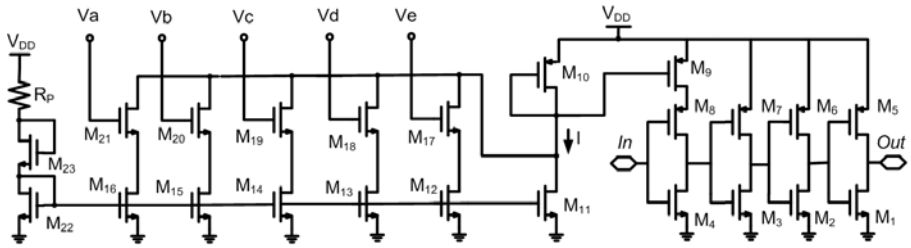

Figure 2.29: Schematic of the delay generator.

The circuit operates by imposing the charge current at the output node of the inverter constituted by the transistors M_4 and M_8, in order to vary the slope of the voltage ramp from the high to the low level at that node.

The transistor M_9 is smaller than M_8 in order to impose the charging current of the node gate of M_3-M_7. Only the charging current can be imposed by transistor M_9 (and not the discharging current), since only the delay of the falling edge of the digital signal *Command* is required.

The inverters M_1-M_5 and M_2-M_6 allows a more rapid transition from the high to low levels of the output voltage.

The channel width of the PMOS transistors of the inverters is twice the width of the NMOS, in order to provide a falling time equal to the rising time (μ_n is

approximately equal to $2\mu_p$). The drain current of the transistor M_{10} (i.e. the control current mirrored in M_9) is imposed by acting on the digital input vector *abcde*.

Width and length of the transistors M_{12}-M_{16} have been chosen in accordance to the design criteria reported in [83], which allow us to have a control current linearly dependent from the input vector. At first, M_{11} is sized in order to have the maximum delay desired. Then, a transistor M_0 (not present in the schematic) in parallel with M_{11} is sized in order to have the minimum delay. This transistor M_0 is "splitted" in the five transistors M_{17}-M_{21}, sized as follows

$$(W/L)_{M_i} = \frac{2^{i-1}}{2^5 - 1}(W/L)_{M_0}, \quad i = 1, ..., 5 \tag{2.18}$$

The transistor area sizing is reported in Table 2.4. The transistors M_{17}-M_{21} act as digitally driven switches.

Table 2.4: Delay Generator Transistor Area Sizing*

	M_1-M_4	M_5-M_8	M_9	M_{10}	M_{11}
W/L	16/0.1	32/0.1	16/1	16/1	16/1
	M_{12}	M_{13}	M_{14}	M_{15}	M_{16}
W/L	0.6/6.2	1.2/6.2	2.4/6.2	4.8/6.2	9.6/6.2

*units are in µm.

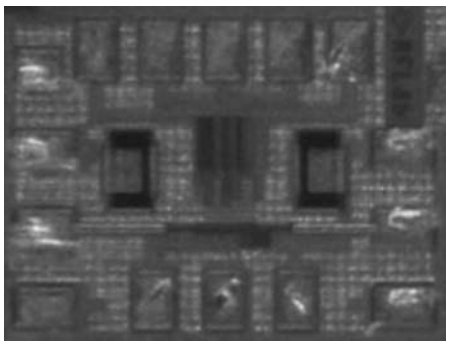

Figure 2.30: Delay generator chip micrograph.

The chip micrograph is shown in Fig. 2.30.

Post-layout simulation results are shown in Figs. 2.31 and 2.32. The delay vs. input vector is shown in Fig. 2.31, whereas the output voltage in the cases of three different input vectors is shown Fig. 2.32. When the input vector is '00000', the control current is given by only the drain current of M_1, which amounts to 15 µA, and provides a delay of 3.1 ns. When the input vector is '11111', the control current is given by summing up the drain currents of M_{11} and M_{17}-M_{21}, which amounts to 53 µA and provides a delay of about 1 nanosecond. Monte Carlo

analyses have shown that this design is very robust with the spread of the process parameters and the variations of temperature.

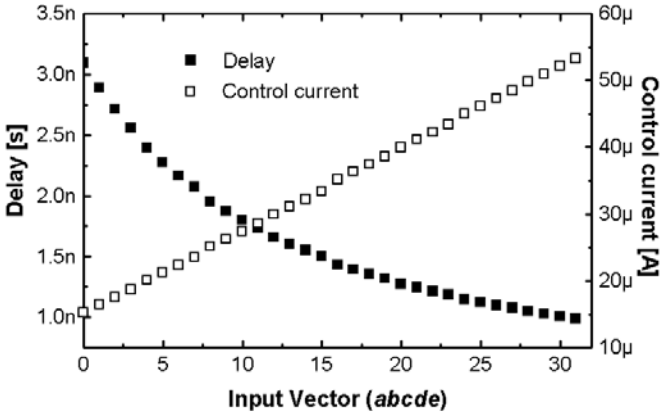

Figure 2.31: Simulated delay and control current vs. the input vector.

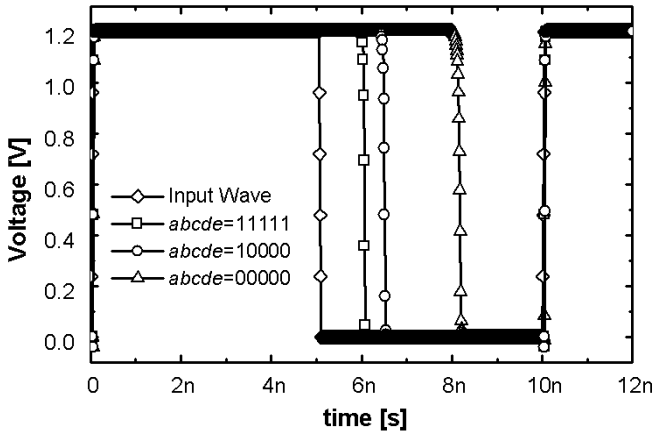

Figure 2.32: Simulated input and output signals vs. time for three different input vectors.

The total area on chip amounts to 0.2 mm^2 (ESD-protected pads inclusive). On-chip measurements have been carried out by means of GSG micro-probes. The measurement setup is shown in Fig. 2.33. The delay generator has been driven by a pulse generator HP 8082A. The input and the outputs (by varying the input vector) have been captured by means of a Tektronix TDS 3054B oscilloscope.

Measurement results have shown a range of obtainable delays (up to 6 ns, see Fig. 2.34) wider than that shown by PLS simulations. This is in part due to the parasitic capacitances of the micro-probes, cables and most of all of the oscilloscope used to capture the output waveform. In fact, the Tektronix TDS

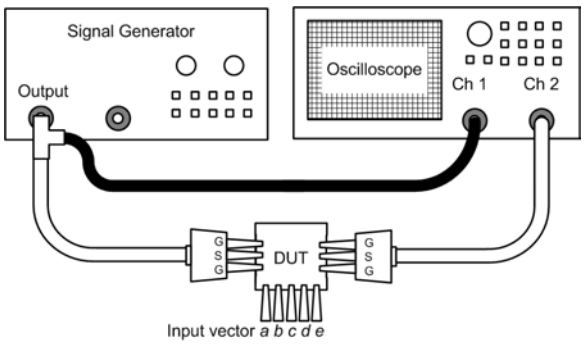

Figure 2.33: Measurement setup of the delay generator.

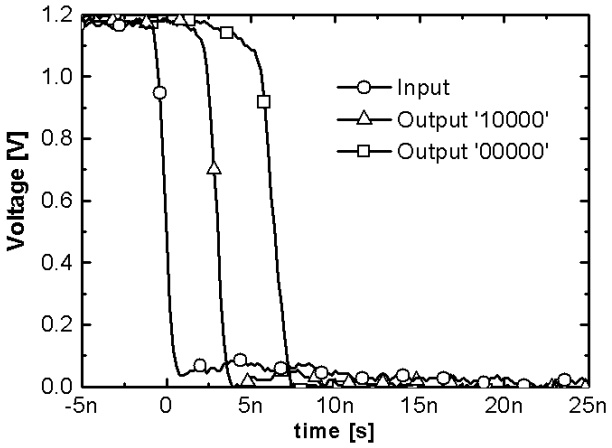

Figure 2.34: Input and output voltage (measured) of the delay generator for two different values of the input vector, captured by an oscilloscope with input impedance of 1 MΩ in parallel with 13 pF (in addition to the parasitic capacitances of the cables).

3054B oscilloscope presents an input impedance of 1 MΩ in parallel with 13 pF (that is significantly higher than the 40 fF load for which the delay generator has been designed), in addition to the parasitic capacitances of the cables. This fact has been confirmed by simulations.

2.6 System-on-a-Chip UWB Radar for The Cardio-Pulmonary Monitoring in 90nm CMOS Technology

The co-integration of all the building blocks of the UWB radar shown in Fig. 2.3 has been done. The UWB radar has been designed in 90nm CMOS technology by ST-Microelectronics into a single chip. The layout is shown in Fig. 2.35, and has been sent to the foundry (ST-Microelectronics) for its realization.

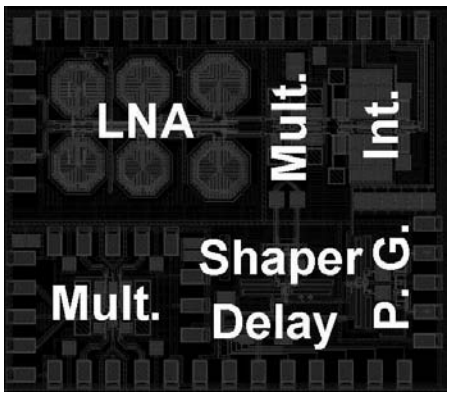

Figure 2.35: Layout of the system-on-a-chip UWB radar for the Cardio-Pulmonary Monitoring. *Mult.*, *Int.* and *P.G.* are the multiplier, the integrator and the pulse generator. An additional cell multiplier is present on the chip in order to be measured stand-alone.

In the top side of Fig. 2.35 there is the receiver, constituted by the LNA, the multiplier (designed by Martina Mincica, University of Pisa) and the integrator (designed by Alessandro Fonte, University of Pisa). At the bottom, there are the pulse generator, the shaper (based on a review of the pulse generator), and the delay generator. In this implementation, a regenerative buffer has been designed at the input of the pulse generator, in order to regenerate the slope of the driver signal of the pulse generator. In this way, the duration of the first monocycle of the output waveform provide by the pulse generator is independent from the slope of the digital *Command* signal.

2.7 Remarks

The recent advances in silicon CMOS technology allow the realization of even more miniaturized, low-cost and low-power integrated system-on-a-chip sensors. These sensors can be employed in the wireless body area networks, for advanced and continuous monitoring of vital parameters. In particular, the system overview of a next generation wearable wireless sensors for human health care and safeguard has been presented. Such a system is composed by a novel fully integrated ultra-wide-band radar sensor for the detection of the heart and breath rates and a low-power radio interface (IEEE 802.15.4, ZigBee), which collects the data provided by the sensor and sends these data to a remote data acquisition unit or even in the

Internet by means of a personal server. Thus, the physiological data of a person under observation can be sent in real time to the hospital to be analyzed and, then, the doctors could act in-time in case of anomalies in the vital parameters monitored.

A detailed feasibility study of the UWB radar on silicon technology (90nm CMOS) has been carried out, by means of both theoretical analysis and CAD tool simulations. The simulation results have shown a wide agreement with the theoretical model of the radar, demonstrating the feasibility of the proposed system-on-a-chip radar in a modern silicon technology.

Moreover, the main critical building blocks of the radar sensor (low noise amplifier, pulse generator and delay generator) have been designed, prototyped in 90nm CMOS process by ST-Microelectronics. The performance of the test-chip have been measured. Measurement results are in good agreement with post-layout simulation results.

Finally, the co-integration of all the building blocks of the UWB radar has been done, and the test-chip has been sent to the foundry for its realization.

Chapter 3

60-GHz Low Noise Amplifier

3.1 Introduction

In the last few years, the interest in the 60 GHz radio-frequency band has rapidly grown, since the great bandwidth available allows the implementation of very high (Gigabit/s) data-rate communication systems.

The latest advances in silicon technologies allow the realization of fully integrated, highly miniaturized and low cost systems operating up to the millimeter wave frequency band [84, 85]. However, at this frequency, one of the most important challenge consists of reaching an adequate gain, especially by using MOSFETs of a standard CMOS process.

Most of the CMOS millimeter-wave amplifiers presented in literature are implemented by a distributed approach, based on the realization of the passive elements by means of integrated microstrip lines [86]. However, some works presented recently [85] have demonstrated the feasibility of 60-GHz amplifiers even by using passive lumped components, obtaining a great saving of silicon area with respect to distributed solutions.

The input impedance matching of these amplifiers is realized typically by using the traditional techniques, such as passive impedance-transformer matching networks at the input of the amplifier, or the input integrated matching with source degeneration [87].

In this chapter a novel low noise amplifier topology, in a 65nm bulk CMOS technology by ST- Microelectronics, is presented. The input integrated matching has been realized by exploiting a novel technique based on the employment of an integrated transformer [OP13]. In detail, the novel transformer-based technique adopted for realizing the input matching is presented, and its application on the design of a 60-GHz LNA in a bulk 65nm CMOS technology by ST-Microelectronics is presented.

3.2 A Novel Technique to Achieve the Input Matching of a Low Noise Amplifier

The most widespread topology employed to realize low noise amplifiers is the cascode topology, because of its higher output resistance, higher gain and bandwidth

due to the reduced Miller effect, and high reverse isolation with respect to the single-transistor common source topology.

Since the input impedance of a MOS transistor is almost capacitive, some techniques have to be employed in order to match the input impedance of the LNA to a resistive source impedance in order to maximize the power transfer. The most widespread techniques to match the LNA with a 50Ω source consist of the use of passive impedance-transformer matching networks (see Fig. 3.1a), and the input integrated matching with inductive degeneration, based on two inductances in series with the gate and the source of the MOS transistor respectively (see Fig. 3.1b) [87]. The latter approach is also derived with a spiral of an integrated transformer [88, 89].

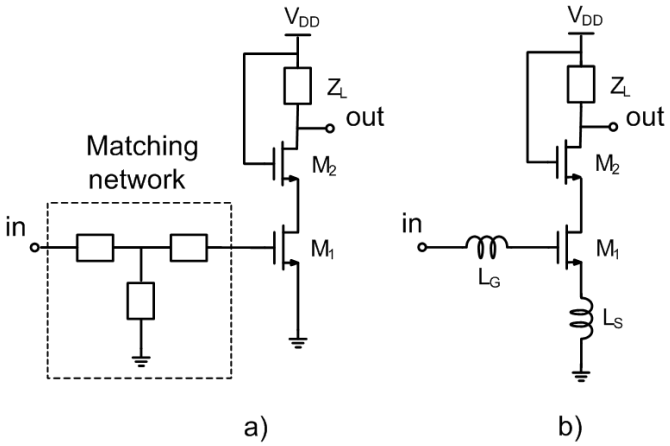

Figure 3.1: LNA configurations, with: a) input impedance matching realized by means of a passive matching network between the input-source and the amplifier; b) input impedance matching realized by means of inductive degeneration and an inductance in series with the gate of M_1.

At very high frequencies, such as 60 GHz, the gain of MOS transistors is very low. The introduction of an inductive degeneration on the source performs the real part of the input impedance equal to 50Ω but also reduces the gain of the amplifier. In fact, by considering the simplest small-signal equivalent circuit of a MOS transistor (see Fig. 3.2a), including only the gate-source capacitance C_{gs} and the transconductance g_m (3.1), the total equivalent transconductance gain of the cascode amplifier with a source inductive degeneration (see Fig. 3.3) can be expressed as in (3.2),

$$g_m(\omega) = \frac{\partial I_{ds}(\omega)}{\partial V_{gs}(\omega)} \tag{3.1}$$

$$g_m^*(\omega) = \frac{\partial I_{ds}(\omega)}{\partial V_{in}(\omega)} = \frac{g_m(\omega)}{1 + j\omega L_s(g_m + j\omega C_{gs})} \tag{3.2}$$

where I_{ds} is the drain-to-source current, V_{gs} is the gate-to-source voltage, L_s is the inductance on the source and ω is the operating frequency expressed in [rad/s].

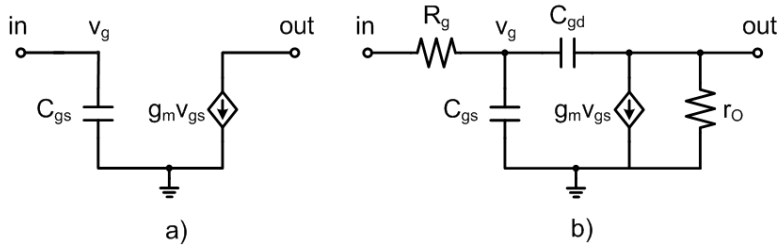

Figure 3.2: a) Simple model of an ideal MOS transistor. b) Simple model of a MOS transistor including the gate resistance R_g, the gate-drain capacitance C_{gd} and the output resistance r_O.

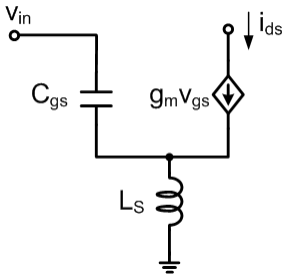

Figure 3.3: Small-signal equivalent circuit of a MOS cascode amplifier with a source inductive degeneration.

The novel input impedance matching technique herein proposed allows the realization of the input integrated matching without requiring any source degeneration, and thus it is well suited especially for high frequency amplifiers, where fair gain is hard achieved. The proposed input matching technique exploits the mutual coupling between the spirals of an integrated transformer: the primary spiral is connected between the radio-frequency input and the gate of the common-source transistor of the cascode amplifier, whereas the secondary spiral is connected in series between the drain of the above mentioned transistor and the source of the common-gate transistor. The novel LNA topology herein presented is shown in Fig. 3.4.

By considering the simplest small-signal model of a MOS transistor, the input impedance of the amplifier (Z_{in}) results equal to

$$Z_{in} = sL_1 + \frac{1}{sC_{gs}} + \frac{Mg_m}{C_{gs}} \tag{3.3}$$

From (3.3) it can be seen that thanks to the mutual coupling (M) of the spirals L_1 and L_2, the input impedance of the amplifier of Fig. 3.4 presents a real part, which can be made equal to 50Ω by properly sizing the transformer. Moreover, the inductance of the secondary spiral of the transformer can be also exploited for compensating the inter-stage loss [85].

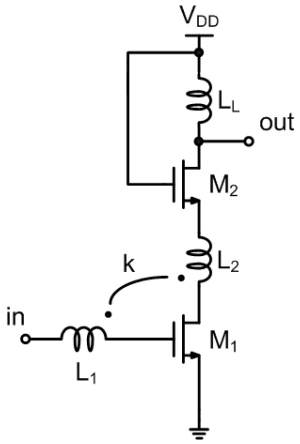

Figure 3.4: Schematic of the novel LNA topology. This exploits the mutual coupling between the primary spiral (L_1) and the secondary spiral (L_2) of an integrated transformer in order to provide the input impedance matching with a 50Ω source.

Unfortunately, the simplified small signal equivalent circuit of the MOS transistor of Fig. 3.2a is appropriate only for long-channel devices, and only when the operating frequency is far (e.g. a roughly one tenth) from the cut-off frequency. Actually, the 65nm CMOS bulk technology by ST-Microelectronics provides n-MOS transistors with a maximum cut-off frequency of about 200 GHz. An operating frequency of 60 GHz is not much lower than the cut-off frequency exhibited by the MOSFETs. Thus, the parasitic components can not be neglected in the calculation of Z_{in}, especially the gate-drain capacitance C_{gd} and the output resistance r_O (see Fig. 3.2b). By replacing the simplified small-signal equivalent circuit of the MOS transistor of Fig. 3.2b in the LNA of Fig. 3.4, the expression of Z_{in} becomes intricate and depends on a lot of design parameters.

3.2.1 Calculation of The Input Impedance of the Transformer-Based LNA

By considering the simplest model of the MOS transistor (see Fig. 3.2a), the input impedance of the transformer-based LNA, shown in Fig. 3.4, can be easily expressed by Equation 3.3. However, for short channel devices, and especially operating at millimeter-waves, some parasitic effects can not be neglected.

Hereinafter the calculation of the input impedance of the LNA has been reported, in the case of the simple (but more complex that those of Fig. 3.2a) equivalent small-signal circuit of the MOS transistor shown in Fig. 3.2b.

By considering the MOS transistor model of Fig. 3.2b, in order to calculate the input impedance of the LNA of Fig. 3.4, its equivalent small-signal circuit can be represented as in Fig. 3.5, where Z_L is the impedance seen in the source of the common-gate stage $\left(Z_L \approx \frac{1}{g_{m2}} \parallel \frac{1}{j\omega C_{gs2}}\right)$.

By considering the impedances Z_1 and Z_2

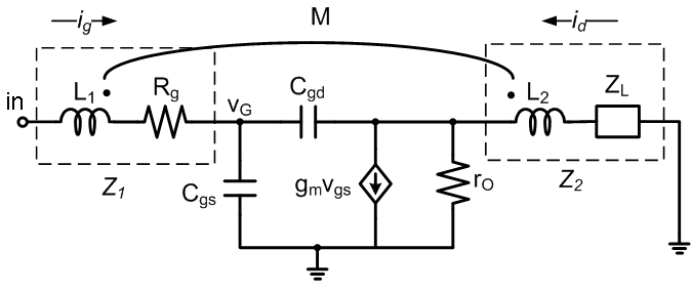

Figure 3.5: Simple equivalent circuit of the LNA of Fig. 3.4 (for the only purpose of evaluating the input impedance).

$$Z_1 = R_g + j\omega L_1 + j\omega M \frac{i_d}{i_g} \tag{3.4}$$

$$Z_2 = Z_L + j\omega L_2 + j\omega M \frac{i_g}{i_d} \tag{3.5}$$

were R_g is the gate resistance, L_1 and L_2 are the inductances of the primary spiral and the secondary spiral of the transformer respectively and M is the mutual coupling between the spirals and i_d and i_g are the drain and gate signal currents, the input impedance Z_{in} can be written as follows

$$Z_{in} = Z_1 + \frac{sC_{gd}r_O Z_2}{s^2 C_{gs}C_{gd}r_O Z_2 + sC_{gd}(r_O + Z_2 + g_m r_O Z_2) + sC_{gs}(r_O + Z_2)} \tag{3.6}$$

Z_1 and Z_2 are a function of i_d/i_g.

$$\begin{aligned}\frac{i_g}{i_d} =& \frac{s^3 C_{gs}C_{gd}r_O L_2 + s^2[(C_{gs}C_{gd}Z_L + g_m C_{gd}L_2)r_O + (C_{gs}+C_{gd})L_2]}{s^3 M C_{gs}C_{gd}r_O + s^2 M(C_{gs}+C_{gd}+g_m C_{gd}r_O) + sC_{gd}r_O - g_m r_O} + \\ &+ \frac{s[(g_m C_{gd}Z_L + C_{gs} + C_{gd})r_O + C_{gs}Z_L + C_{gd}Z_L]}{s^3 M C_{gs}C_{gd}r_O + s^2 M(C_{gs}+C_{gd}+g_m C_{gd}r_O) + sC_{gd}r_O - g_m r_O}\end{aligned} \tag{3.7}$$

The expression of i_g/i_d is reported in (3.7). By substituting (3.7) in (3.4) and (3.5), and then (3.4) and (3.5) in (3.6), the expression of Z_{in} became very complex and its dependence from all the variables is not clear.

In order to investigate the behavior of the LNA as a function of the MOS transistor parameters, and to evaluate the detriment of performance due to the parasitic components of the MOSFETs (C_{gd} and r_O), the simple model of Fig. 3.5 has been implemented in ADS2005A by Agilent Technologies™.

The simulations have shown results very close to those obtained from the full model available directly from the design-kit within SpectreRF™ in the Cadence™ environment. In particular, with respect to the results obtained with (3.3), the simulations including the simplified MOSFET model (see Fig. 3.2b) have shown

that C_{gd} and r_O decrease the real part of the input impedance of the LNA (Z_{in}) (see Fig. 3.6) and make the imaginary part of Z_{in} dependent on the mutual inductance M of the transformer. Then, the value of the input impedance Z_{in} can be refined by acting properly on the gate width W and transconductance.

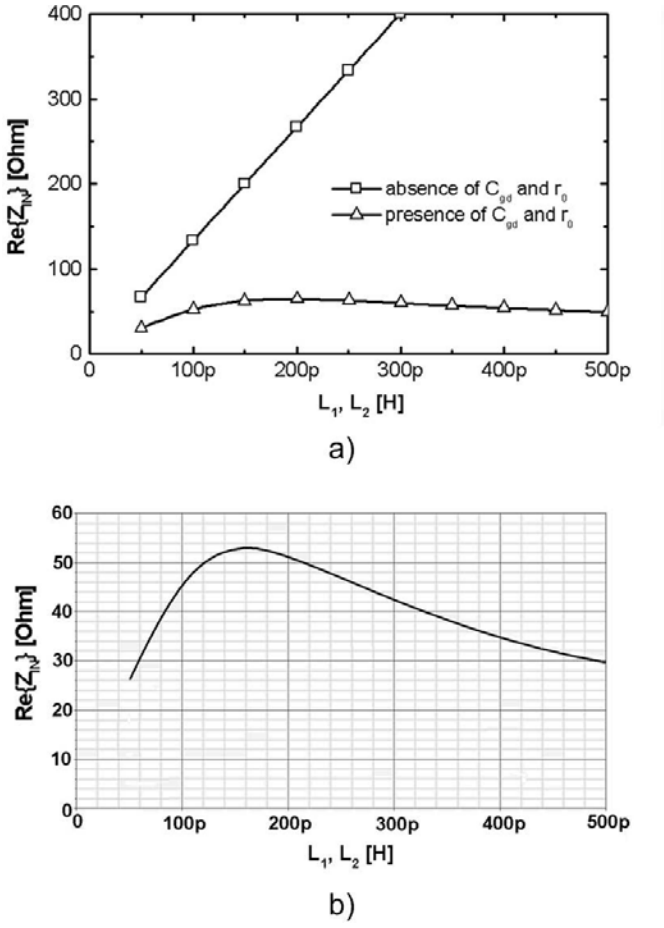

Figure 3.6: Real part of the input impedance of the LNA of Fig. 3.4 (in the case of transformer 1:1 with coupling factor equal to 1, and transistors with $W = 60$ µm) vs. the value of the inductances of the spirals: a) obtained by simulations within ADS2005A™, by using the simple transistor model of Fig. 3.2a (without parasitics) and of Fig. 3.2b (with the parasitics C_{gd} and r_0); b) obtained by simulations within Cadence™ by using the MOSFET model provided in the design kit. It can be noted that the parasitic components C_{gd} and r_0 reduces the real part of the input impedance of the LNA with respect to the ideal case.

3.2.2 Design Criteria

After investigating the effects of the MOS transistor parasitics on the LNA input matching, the influence of the main design parameters (the inductance value of the transformer spirals L_1 and L_2, the coupling factor between the spirals (k), the gate width of the transistors M_1 and M_2 and the cascode bias current I, see Fig. 3.4) on the real and imaginary parts of the LNA input impedance have been investigated.

At first the width of the transistor of the cascode stage, and the bias current of the cascode have been chosen, in order to provide the best available gain at the frequency of interest (60 GHz, in our case). A maximum-gain criterium has been adopted (instead, for example, a minimum noise or minimum power dissipation criteria) since at the millimeter-wave the transistor gain is a critical parameter, especially in a bulk CMOS technology. Then, the range of the gate width of the transistors of the LNA for which the available gain is higher than a minimum acceptable value has been identified. This has been done in order to know the range in which we can tune the transistors gate width for future refinements of the LNA input impedance.

Then, the transformer has been sized (at schematic level), in order to have the input impedance of the LNA equal to 50Ω. The inductance of the secondary spiral of the transformer (L_2) can be chosen in order to resonate with the capacitance seen at the drain of the common-source transistor of the cascode stage, in order to increase the cut-off frequency of the amplifier.

3.3 LNA Design at 60 GHz

The new topology of cascode LNA has been employed for the design of a 60-GHz LNA in bulk 65nm CMOS technology by ST-Microelectronics. With respect to the most relevant works presented in the literature for the millimeter-waves frequency range [86, 90], which use passive inductors realized by means of microstrip lines, this design has been approached by using lumped-component. In fact, recently, several works have demonstrated the feasibility of lumped passive inductors with self resonating frequencies greater than 100 GHz [85, 91] , which allow a relevant area saving on die. However, in principle, this novel LNA design can be approached by using coupled microstrip lines and bipolar process as well.

The design of the integrated transformer and the design of the LNA are reported in the following subsections.

3.3.1 Transformer Design

From the analysis carried out, it results that, in order to have an input impedance of the LNA equal to about 50Ω, a transformer with the following characteristics has to be designed

- $L_1 \simeq 250$ pH
- $L_2 \simeq 100$ pH
- $k \simeq 0.6$

The transformer has been designed by means of the 3D EM simulator HFSS™. The structure adopted to implement the transformer is shown in Fig. 3.7.

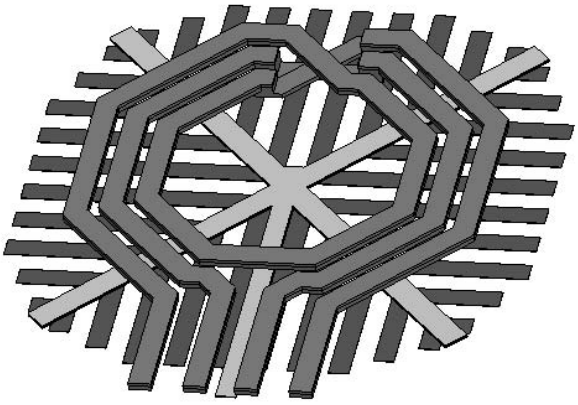

Figure 3.7: The proposed 60-GHz transformer, designed by means of the 3D EM simulator HFSS™ by Ansoft™.

Since the value of the mutual coupling required is relatively low, a planar transformer, instead of a stacked transformer, has been designed. Moreover, simulations have shown that in a planar transformer the integrated spirals have an higher cut-off frequency with respect to a stacked transformer. Indeed the inter-metal parasitic capacitance between the spirals is quite high and lowers the maximum frequency of operation of the transformer in stacked transformer.

The transformer has been designed on a patterned ground shield (PGS) in order to decouple the electromagnetic fields from the substrate, in spite of simulated results have shown that performance were a little better without PGS.

As starting point for the transformer sizing, the equations reported in [41, 92] have been employed.

The primary of the transformer is constituted by two turns, while the secondary is constituted by a spiral between the turns of the primary.

The primary and secondary spiral of the transformer have been designed in the top thick metal level (metal 7) and alucap, while the underpass of the primary is designed in metal 6 (thick) and the underpass of the secondary in metal 5. The outer diameter of the transformer is equal to 80 µm, the metal width is equal to 4.4 µm and the spacing between the spirals is equal to 2 µm. The inductances and quality factors of the spirals have been computed with the following equations [OP5]

$$L_{12} = \frac{\mathrm{Im}\left\{\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right\}}{\omega} \tag{3.8}$$

$$Q_{12} = \frac{\omega L_{12}}{R_{12}} \tag{3.9}$$

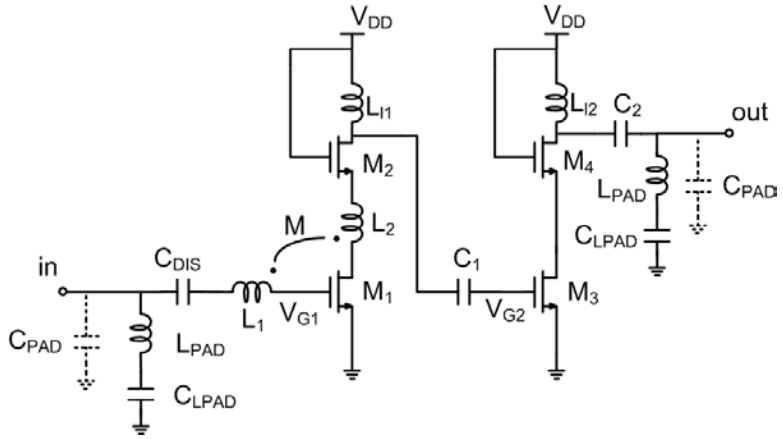

Figure 3.8: Simplified schematic of the 60-GHz LNA herein presented.

where the indexes 1 and 2 are referred to the two terminals of each spiral. By using these expressions, the self-inductance of the primary results equal to 240 pH with an associated quality factor of about 8.5 at 60 GHz. The self-inductance of the secondary results close to 85 pH with an associated quality factor of about 8 at 60 GHz. The coupling factor has been evaluated by using the expression reported in [93] and it has resulted close to 0.6 at 60 GHz. The S-parameters of the transformer obtained by the EM simulations have been inserted in the Cadence design flow in order to perform the overall LNA simulations.

3.3.2 LNA Design

The simplified schematic of the LNA is reported in Fig. 3.8.

A traditional cascode stage has been implemented as second stage in order to provide an adequate overall gain at 60 GHz. The RF pads connected to the circuit present an overall parasitic capacitance close to 80 fF (C_{PAD}). At 60 GHz, the magnitude of the equivalent impedance is about 35Ω thus leading to a severe mismatching of input and output impedances. To mitigate such inopportune effect, two inductors (L_{PAD}) have been introduced in parallel to the input and output pads in order to resonate with C_{PAD} at the frequency of interest. Unfortunately, this compensation reduces the LNA bandwidth, whereas the parasitic resistance of such additional inductors increases the noise figure.

The transistors M_1, M_2, M_3 and M_4 have a gate width of 30, 50, 36 and 46 µm, respectively. The inductance L_{l1} and L_{l2} are equal to 90 pH. The capacitances C_1 and C_2 are equal to 36 fF and 30 fF, respectively. The inductances L_{PAD} are equal to 90 pH.

3.4 Post Layout Simulations

The post-layout simulations of the 2-stage LNA proposed in Fig. 3.8 have been carried out (inclusive of the additional inductors in parallel to the input and output pads). The S_{11} parameter presented in Fig. 3.9 reaches -17 dB at 61.45 GHz. It remains lower than -10dB from 59 to 64.6 GHz, which covers the overall frequency band allocated for European personal wireless area network (WPAN) applications.

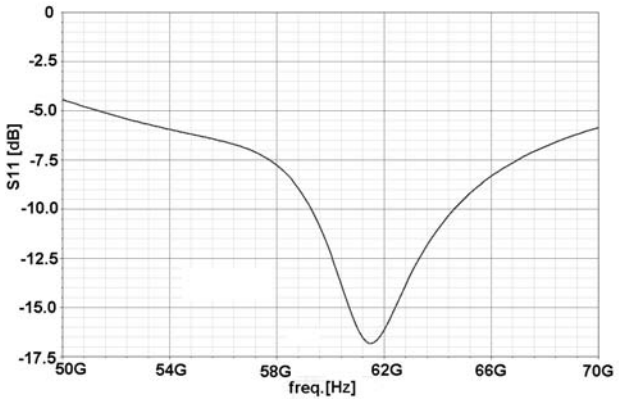

Figure 3.9: S_{11} parameter obtained by post-layout simulations.

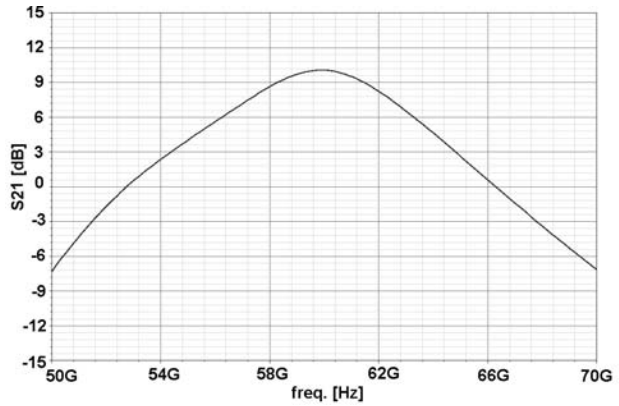

Figure 3.10: S_{21} parameter obtained by post-layout simulations.

As far as the S_{21} parameter is concerned, it reaches 10 dB at 60 GHz, as shown in Fig. 3.10. The overall power consumption (P_C) amounts to 18.5 mW with a 1.2 V supply voltage. The noise figure (NF) and the noise figure minimum ($NFmin$) are reported in Fig. 3.11. They are equal to 8.68 dB at 60 GHz. The noise contribution due to the additional inductor L_{PAD} is estimated to 2.5 dB. The input-referred 1 dB compression point ($\mathrm{ICP_{1dB}}$) is equal to -13 dBm.

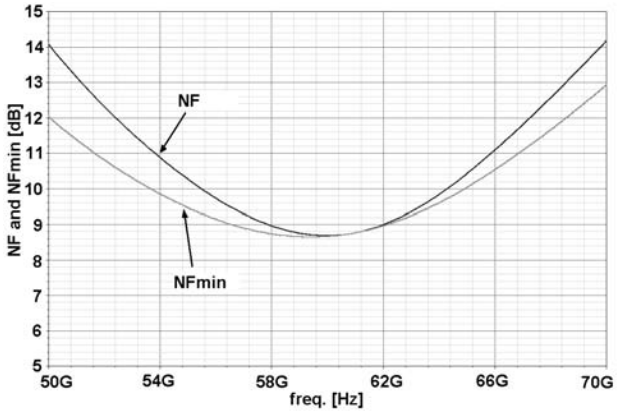

Figure 3.11: NF and $NFmin$ parameters obtained by post-layout simulations.

A summary of the performance and the comparison with the state-of-the-art for 60-GHz LNA realized in standard CMOS technology are reported in Table 3.1. Our work and [85] exploit a lumped component approach, which require a lower area occupation with respect to [86]. Moreover, with respect to [86], the above same performances in terms of gain, NF and S_{11} are achieved while depicting less than half the power supply. For sake of clarity, it is worth mentioning that our performance are obtained by simulations, while the performance of the other works reported in Table 3.1 are obtained by measurements.

Table 3.1: Summary of The LNA Performance and Comparison with The State of The Art of CMOS 60-GHz LNA

Work	tech.	$\lvert S_{11min}\rvert$ [dB]	S_{21MAX} [dB]	NF [dB]	P_C [mW]	V_{DD} [V]	Area [mm^2]	Meas. (M) or Sim. (S)
[85]	90nm	-10	14.6	<5.5	24	1.5	0.15	M
[86]	0.13µm	-10	12	8.8	54	1.8	1.3	M
Our	65nm	-16.45	10.02	8.68	18.5	1.2	0.43	S

3.5 Measurements

The micrograph of the 60-GHz LNA test-chip is shown in Fig. 3.12. Passive structures (i.e. the transformer, see Fig. 3.13) designed has been integrated stand-alone in order to validate the results of HFSS™ simulations. Measurements on the passive structures have confirmed the 3D EM simulation results.

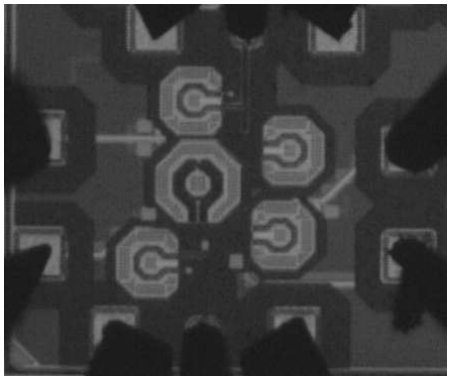

Figure 3.12: Micrograph of the 60-GHz LNA.

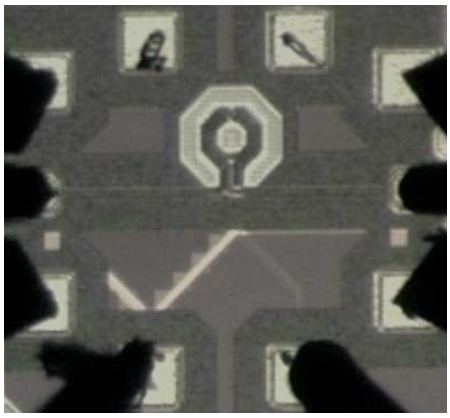

Figure 3.13: Micrograph of the transformer stand alone.

As for the LNA, it has not been possible to measure properly, since the pad capacitance and the inductors L_{PAD} resonate at a frequency out of band of operation of the LNA (i.e. resonate at about 86 GHz). This fact is due to the inaccurate estimation of the pad parasitic capacitances (i.e. over-estimated, as confirmed by 3D EM simulations, see Fig. 3.14) obtained by the parasitic extractor.

A redesign of the 60-GHz LNA is in progress at the present moment.

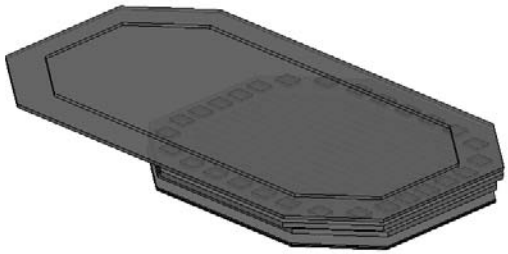

Figure 3.14: Pad structure simulated by HFSS™.

3.6 Remarks

A novel low noise amplifier topology, which exploits a new technique for realizing the input integrated matching (simultaneous noise and impedance matching), has been presented. Based on the integration of a transformer into the cascode LNA, this new technique (named as transformer-based input integrated matching in cascode amplifiers or TIIMCA) allows us to avoid any gain reduction at high frequency due to the inductive degeneration. As case of study, the novel LNA topology has been implemented as the first stage of a two-stage LNA, which has been designed in 65nm CMOS bulk technology for 60 GHz millimeter-wave applications. The transformer has been designed with the 3D electromagnetic simulator HFSS™, and the S-parameters obtained by simulation have been included in the Cadence design framework for a proper design of the TIIMCA topology. The post-layout simulations of the two-stage LNA have shown a good input impedance matching in terms of S_{11} equal to -16.84 dB, with an associated gain in terms of S_{21} equal to 10.02 dB, at 61.45 GHz. The noise figure is 8.68 dB at 60 GHz, showing an almost perfect matching to the minimum noise figure. The overall power consumption is 18.5 mW under a 1.2 V supply voltage.

Conclusions

The recent advances in silicon CMOS technology allow us to realize highly miniaturized, low cost and low power systems-on-a-chip (SoaC). The opportunity for realize complex system on a single silicon die will allow the realization of low-cost devices for mass-market applications.

In Chapter 1, the design of radio-frequency integrated circuits for 2.4-GHz RFID and 5-GHz WLAN has been reported, showing the potentiality of bring into play low-power and low-cost systems for these emerging applications in silicon technologies such as the 0.35µm (Bi)CMOS by Austriamicrosystems.

In Chapter 2, the feasibility of a system-on-a-chip based on an ultra-wideband (UWB) radar for the cardio-pulmonary monitoring has been reported. It has been demonstrated that such a system has all the potential to be integrated in a modern silicon technology as well as the 90nm CMOS by ST-Microelectronics. Moreover, the design of the most critical building blocks has been dealt with, and the measurement results have confirmed the performance obtained by post-layout simulations.

In Chapter 3, the design of a 60-GHz low noise amplifier (LNA), based on a novel topology that allows the achievement of the integrated input impedance matching based on an integrated transformer has been reported, demonstrating the opportunities to realize in standard silicon technologies such as the 65nm CMOS fully integrated transceivers operating up to the millimeter waves.

In conclusion, these works have shown the potentiality of CMOS silicon technologies to be employed profitably for the implementation of modern fully integrated systems as UWB and millimeter-wave wireless transceivers.

List of Publications

International Journals

[OP1] D. Zito, D. Pepe and B. Neri, "RFID systems: passive vs. active and a novel low-power RF radio transceiver for IEEE 802.15.4 (ZigBee) standard based applications," *Journal of Low Power Electronics*, vol. 3, no. 1, pp. 96-105, Apr. 2007.

[OP2] D. Zito, D. Pepe, B. Neri, F. Zito, D. De Rossi, A. Lanatà", "Feasibility study and design of a wearable system-on-a-chip pulse radar for contact-less cardiopulmonary monitoring," *International Journal of Telemedicine and Applications*, vol. 2008, 10 pages, 2008.

[OP3] D. Zito and D. Pepe, "LC-active VCO for CMOS RF transceivers," *International Journal of Circuit Theory and Applications*, accepted for publication.

International Conferences

[OP4] D. Zito, D. Pepe and B. Neri, "Low-power RF transceiver for IEEE 802.15.4 (ZigBee) standard applications," in *13th IEEE International Conference on Electronics, Circuits and Systems*, Nice, France, Dec. 2006, pp. 1312-1315.

[OP5] D. Zito, D. Pepe and B. Neri, "Wide-band frequency-independent equivalent circuit model for integrated spiral inductors in (Bi)CMOS technology," in *13th IEEE International Conference on Electronics, Circuits and Systems*, Nice, France, Dec. 2006, pp. 478-481.

[OP6] D. Zito, D. Pepe, B. Neri and G. Scandurra, "Modeling and design of the CMOS boot-strapped inductor for 5-6 GHz applications," in *13th IEEE International Conference on Electronics, Circuits and Systems*, Nice, France, Dec. 2006, pp. 471-474.

[OP7] D. Zito, D. Pepe and B. Neri, "High-performance VCO for 5-GHz WLANs in 0.35 um CMOS standard technology," in *13th IEEE International Conference on Electronics, Circuits and Systems*, Nice, France, Dec. 2006, pp. 188-191.

[OP8] D. Zito, D. Pepe, B. Neri, D. De Rossi and A. Lanatà, "Wearable system-on-a-chip pulse radar sensors for the health care: system overview," in *IEEE International Conference on Advanced Information Networking and Applications (International Workshop on Smart Homes andTele-Health)*, Niagara Falls, Canada, May 2007, pp. 766-769.

[OP9] D. Zito, D. Pepe, B. Neri and D. De Rossi, "Feasibility study of a low-cost system-on-a-chip UWB pulse radar on silicon for heart monitoring," in *IEEE International Waveform Diversity and Design Conference*, Pisa, Italy, June 2007, pp. 32-36.

[OP10] F. Zito, D. Zito and D. Pepe, "UWB 3.1-10.6 GHz CMOS transmitter for system-on-a-chip nano-power pulse radars," in *IEEE 3rd Conference on PhD Research in Microelectronics and Electronics*, Bordeaux, France, July 2007, pp. 189-192.

[OP11] D. De Rossi, A. Lanatà, E. P. Scilingo, D. Zito, D. Pepe and B. Neri,"An ultra wide bandwidth wearable system for cardiopulmonary monitoring," in *4th International Conference on Personalised Healthcare (pHeath)*,Porto Carras, Greece, June 2007, (invited).

[OP12] D. Zito, D. Pepe, B. Neri, D. De Rossi, A. Lanatà, A. Tognetti, E. P. Scilingo,"Wearable system-on-a-chip UWB radar for health care and its application to the safety improvement of emergency operators," in *29th International Conference of the IEEE Engineering in Medicine and Biology Society*, Lyon, France, Aug. 2007, pp. 2651-2654.

[OP13] D. Zito, D. Pepe, T. Taris, J.-B. Begueret, Y. Deval, B. Neri and D. Belot, "A novel LNA topology with transformer-based input integrated matching and its 60-GHz millimeter-wave CMOS 65-nm design," in *14th IEEE International Conference on Electronics, Circuits and Systems*, Marrakech, Morocco, Dec. 2007, pp. 188-191.

[OP14] E. P. Scilingo, A. Lanatà, D. Zito, D. Pepe, D. De Rossi,"Wearable monitoring of cardiopulmonary activity through radiant sensing," in *IEEE International Workshop on Wearable Micro and Nanosystems for Personalised Health (pHealth)*, Valencia, Spain, May 2008, (invited).

[OP15] D. Zito, D. Pepe, M. Mincica, F. Zito, D. De Rossi, A. Lanatà, E. P. Scilingo, A. Tognetti,"Wearable system-on-a-chip UWB radar for contact-less cardiopulmonary monitoring: present status," in *30th International Conference of the IEEE Engineering in Medicine and Biology Society*, Vancouver, Canada, Aug. 2008, pp. 5274-5277.

[OP16] D. Zito, D. Pepe, M. Mincica, F. Zito, D. De Rossi,"Wearable SoC UWB (3.1-10.6 GHz) radar for cardiopulmonary monitoring," in *IEEE International Conference on VLSI-SoC*, Rhodes, Greece, Oct. 2008, (invited).

National Conference

[OP17] D. De Rossi, A. Lanatà, U. Mengali, B. Neri, D. Pepe, E. P. Scilingo and D. Zito,"Wearable wireless sensors for human health care and safeguard: the case study of system-on-a-chip UWB micro-power radars," in *101st AEIT Conference*, Capri, Italy, Sep. 2006.

Bibliography

[1] "IEEE standard 802.15.4," IEEE, 2003.

[2] "Zigbee alliance," ZigBee Alliance. [Online]. Available: www.zigbee.org

[3] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification*, 2nd ed. Wiley and Sons, 1999.

[4] "ETSI EN 300-440-1 v.1.3.1," European Telecommunications Standard Institute, 2001.

[5] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-uW minimum RF input power," *IEEE Journal of Solid State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[6] R. Glidden, C. Bockorick, S. Cooper, C. Diorio, D. Dressler, V. Gutnik, C. Hagen, D. Hara, T. Hass, T. Humes, J. Hyde, R. Oliver, O. Onen, A. Pesavento, K. Sundstrom, and M. Thomas, "Design of ultra-low-cost UHF RFID tags for supply chain applications," *IEEE Communications Magazine*, vol. 42, no. 8, p. 140151, Aug. 2004.

[7] J. P. Curty, J.P, N. Joehl, C. Dehollain, and M. J. Declercq, "Remotely powered addressable UHF RFID integrated system," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2193–2202, Nov. 2005.

[8] D. Manstretta, R. Castello, F. Gatta, P. Rossi, and F. Svelto, "A 0.18um CMOS direct-conversion receiver front-end for UMTS," *IEEE International Solid State Circuits Conference*, vol. 39, no. 1, p. 1523, Jan. 2002.

[9] V. Cheung and H. Luong, "A 1V 10-mW monolithic bluetooth receiver in a 0.35um CMOS process," in *IEEE European Solid State Circuit Conference*, Estoril, Portugal, Sep. 2003, pp. 687–690.

[10] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A scalable high-frequency noise model for bipolar transistors sizing for low-noise amplifier design," *IEEE Journal of Solid State Circuits*, vol. 32, no. 9, pp. 1430–1439, Sep. 1997.

[11] G. Girlando and G. Palmisano, "Noise figure and impedance matching in RF cascode amplifier," *IEEE Transactions on Circuit and Systems II*, vol. 46, no. 11, p. 13881396., Nov. 1999.

[12] D. Zito, G. Devita, and B. Neri, "A new ultra low-power RF receiver topology for wireless communications systems," in *IEEJ International Analog VLSI Workshop*, Bordeaux, France, Oct. 2005.

[13] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of analog integrated circuits*, 4th ed. John Wiley and Sons, Inc., 2001.

[14] T. Tsukahara, M. Ishikawa, and M. Muraguchi, "A 2-V 2-GHz si-bipolar direct conversion quadrature modulator," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 263–267, Feb. 1996.

[15] D. Zito, "A novel low-power radio receiver topology for RF and microwave applications," *International Journal of Circuit Theory and Applications*, Jun 2008.

[16] Zolfaghari and B. Razavi, "A low-power 2.4-GHz transmitter/receiver CMOS IC," *IEEE Journal of Solid State Circuits*, vol. 38, no. 2, pp. 176–183, 2003.

[17] I. Kwon and K. Lee, "An integrated low power highly linear 2.4-GHz CMOS receiver front-end based on current amplification and mixing," *IEEE Microwave and Wireless Components Letters*, vol. 15, pp. 36–38, 2005.

[18] P. Choi, H. C. Park, S. Kim, S. Park, I. Nam, T. W. Kim, S. Park, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, S. M. Park, and K. Lee, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4 GHz," *IEEE Journal of Solid State Circuits*, vol. 38, pp. 2258–2268, Dec. 2003.

[19] A. Italia, F. Carrara, E. Ragonese, and G. Palmisano, "Design methodology for the optimization of transformer-loaded RF circuits," in *International Symposium on Circuits and Systems*, May 2005, pp. 3239–3242.

[20] S. Kim, I. Nam, T. Kim, K. Kang, and K. Lee, "A single-chip 2.4 GHz low-power CMOS receiver and transmitter for WPAN applications," in *Radio and Wireless Conference*, Aug. 2003, pp. 163–166.

[21] P. B. Khannur, "A CMOS power amplifier with power control and T/R switch for 2.45-GHz bluetooth/ISM band applications," in *IEEE Radio Frequency Integrated Circuits Symposium*, Philadelphia, PA, June 2003, pp. 145–148.

[22] K. S. Kundert, "Introduction to RF simulation and its application," *IEEE Journal of Solid State Circuits*, vol. 34, pp. 1298–1319, Sep. 1999.

[23] T. H. Lee and A. Hajimiri, "Oscillator of phase noise: a tutorial," *IEEE Journal of Solid State Circuits*, vol. 35, no. 3, pp. 326–336, Feb. 1998.

[24] D. Linten, "Low-power voltage-controlled oscillators in 90-nm CMOS using high-quality thin-film postprocessed inductors," *IEEE Journal of Solid State Circuits*, vol. 40, no. 9, pp. 1922–1931, Sep. 2005.

[25] Thanachayanont, "CMOS transistor-only active inductor for IF/RF applications," in *International Conference on Industrial Technology*, Dec. 2002, pp. 1209–1212.

[26] Y. C. Wu and M. F. Chang, "On-chip high-Q (3000) transformer-type spiral inductors," *Electronics Letters*, vol. 38, no. 3, pp. 112–113, Jan. 2002.

[27] G. Scandurra and C. Ciofi, "Design of high quality CMOS active inductances using integrated transformers," *WSEAS Transaction on Circuits and Systems*, vol. 5, no. 3, pp. 354–360, Mar. 2006.

[28] G. D'Angelo, L. Fanucci, A. Monorchio, A.Monterastelli, and B.Neri, "High-quality active inductors," *IEE Electronics Letters*, vol. 35, no. 20, pp. 1727–172, Sep. 1999.

[29] G. Scandurra, C. Ciofi, and D. Zito, "A new topology for transformer based CMOS active inductances," in *IEEE PhD Research in Microelectronics and Electronics*, July 2005, pp. 27–30.

[30] "IEEE P802.11, wireless LAN medium access control and physical layer specifications," IEEE, Piscataway, NJ, Jan. 1996.

[31] "ETSI TS 101 475, broadband radio access networks, HiperLANType2, physical layer," European Telecommunications Standards Institute.

[32] A. Bavisi, S. Dalmia, M. Swaminathan, and F. Ayazi, "A 802.11a WLAN oscillator with high Q embedded passives on laminate type organic package," in *IEEE Topical Conference on Wireless Communications Technology*, Oct. 2003, pp. 166–167.

[33] G. D. Astis, D. Cordeau, J. Paillot, and L. Dascalescu, "A 5-GHz fully integrated full PMOS low-phase-noise LC VCO," *IEEE Journal of Solid State Circuits*, vol. 40, no. 10, pp. 2087–2091, Oct. 2005.

[34] W. Chien-Cheng, C. Hsien-Chin, and F. Wu-Shiung, "An ultra-wideband CMOS VCO with 3-5 GHz tuning range," in *IEEE Radio-Frequency Integration Technology*, 30 Nov.-2 Dec. 2005, pp. 87–90.

[35] J.-Y. Foo and R. J. Weber, "Low power 5GHz quadrature phase CMOS lc oscillator with active inductor," in *International Symposium on Communications and Information Technologies*, Oct. 2004, pp. 1084–1089.

[36] J. HeHe and J. G. L. Xie, "Fabrication and simulation of copper spiral on-chip inductors for RF wireless communication," in *IEEE International Conference on Microwave and Millimeter Wave Technology*, Beijing, China, Aug. 2002, pp. 713–716.

[37] E. Ragonese, T. Biondi, A. Scuderi, and G. Palmisano, "A lumped scalable physics-based model for silicon spiral inductors," in *IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications*, Manchester, UK, Nov. 2002, pp. 119 –124.

[38] C.P.Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Electron Devices*, vol. 47, pp. 560–568, Mar. 2000.

[39] C. Yu, R. Groves, N. D. Zamdmer, J.-O. Plouchart, R. Wachnik, H. Xuejue, T.-J. King, and H. Chenming, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *IEEE Journal of Solid State Circuits*, vol. 38, no. 3, pp. 419–426, Mar. 2003.

[40] P. Arcioni, R. Castello, G. D. Astis, G. Sacchi, and E. Svelto, "Measurement and modeling of Si integrated inductors," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, no. 5, pp. 1372–1378, Oct. 1998.

[41] S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid State Circuits*, vol. 34, pp. 1419–1424, Oct. 1999.

[42] D. Melendy, P. Francis, C. Pichler, H. Kyuwoon, G. Srinivasan, and A. Weisshaar, "A new wideband compact model for spiral inductors in RFICs," *IEEE Electron Device Letters*, vol. 23, no. 5, pp. 273–275, May 2002.

[43] A. Niknejad and R. Meyer, "Analysis of eddy-current losses over conductive substrates with applications to monolithic inductors and transformers," *IEEE MTT*, vol. 49, pp. 166–176, Jan. 2001.

[44] "New public safety applications and broadband internet access among uses envisioned by FCC authorization of ultra-wideband technology," Federal Communications Commission, 2002. [Online]. Available: http://www.fcc.gov/Bureaus/Engineering_Technology/News_Releases/2002/nret0203.html

[45] "47 CFR part 15," Federal Communications Commission, 2002. [Online]. Available: http://www.fcc.gov/oet/info/rules/

[46] "Report summary from UWB radio systems committee," Ministry of Internal Affairs and Communications (MIC), 2006. [Online]. Available: http://www.soumu.go.jp/joho_tsusin/eng/pdf/060327_uwb_report.pdf

[47] "ETSI ultra wide band," European Telecommunications Standards Institute, 2008. [Online]. Available: http://www.etsi.org/WebSite/Technologies/UltraWideBand.aspx

[48] J. C. Lin, "Microwave sensing of physiological movement and volume change: A review," *Bioelectromagnetics*, vol. 13, pp. 557–565, 1992.

[49] A. D. Droitcurt, O. Boric-Lubecke, V. M. Lubecke, J. Lin, and G. T. A. Kovacs, "Range correlation and I/Q performance benefits in single-chip silicon radars for noncontact cardiopulmonary monitoring," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 3, pp. 838–848, Mar. 2004.

[50] T. E. McEwan, "Body monitoring and imaging apparatus and method," U.S. Patent 5 573 012, Nov. 12, 1996.

[51] I. J. Immoreev and S. V. Samkov, "Ultra-wideband (UWB) radar for remote measuring of main parameters of patient's vital activity," *Radio physics and radio astronomy*, vol. 7, no. 4, pp. 404–407, Dec. 2002.

[52] E. M. Staderini, "UWB radars in medicine," *IEEE Aerospace and Electronic Systems Magazine*, vol. 17, no. 1, pp. 13–18, Jan. 2002.

[53] S. F. Cleary, F. Nickless, L. M. Liu, and R. Hoffman, "Studies of exposure of rabbits to electromagnetic pulsed fields," *Bioelectromagnetics*, vol. 1, no. 3, pp. 345–352, 1980.

[54] J. A. D'Andrea, B. L. Cobb, and J. O.Lorge, "Lack of behavioral effects in the rhesus monkey: high peak microwave pulses at 1.3 GHz," *Bioelectromagnetics*, vol. 10, no. 1, pp. 65–76, 1989.

[55] T. J. Walters, P. Mason, C. Sherry, C. Steffen, and J. H. Merritt, "No detectable bioeffects following acute exposure to high peak power ultra-wide band electromagnetic radiation in rats," *Aviation, Space and Environmental Medicine*, vol. 66, no. 6, pp. 562–567, June 1995.

[56] C. J. Sherry, D. W. Blick, T. J. Walters, and G. C. Brown, "Lack of behavioral effects in non-human primates after exposure to ultrawideband electromagnetic radiation in the microwave frequency range," *Radiation Research*, vol. 143, no. 1, pp. 93–97, July 1995.

[57] J. Merritt, J. L. Gel, and W. D. Hurt, "Considerations for human exposure standards for fast-rise-time high-penk-power electromagnetic pulses," *Aviation, Space and Environmental Medicine*, vol. 6, no. 66, pp. 586–589, June 1995.

[58] J. R. Jauchem, R. L. Seaman, H. M. Lehnert, S. P. Mathur, K. L. Ryan, M. R. Frei, and W. D. Hurt, "Ultra-wideband electromagnetic pulses: lack of effects on heart rate and blood pressure during two-minute exposures of rats," *Bioelectromagnetics*, vol. 19, no. 5, pp. 330–333, 1998.

[59] M. Klemm and G. Troester, "Textile UWB antennas for wireless body area networks," *IEEE Transaction on Antennas and Propagation*, vol. 54, no. 11, pp. 3192–3197, Nov. 2006.

[60] E. D. Mese, *Appunti al corso di Teoria e Tecnica Radar*. SEU Pisa.

[61] C. Gabriel and S. Gabriel, "Compilation of the dielectric properties of body tissues at RF and microwave frequencies," 2002. [Online]. Available: http://www.brooks.af.mil/AFRL/HED/hedr/reports/dielectric/home.html

[62] D. Andreuccetti, R. Fossi, and C. Petrucci, "Calculation of the dielectric properties of body tissues in the frequency range 10 Hz-100 GHz," 2002. [Online]. Available: http://niremf.ifac.cnr.it/tissprop/htmlclie/stfrtag

[63] H. Schantz, "Near field channel mode," IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs), 2006.

[64] A. Monorchio, "Appunti di compatibilità elettromagnetica," draft 1.01. [Online]. Available: http://www2.ing.unipi.it/homepages/agostino.monorchio/emc.html

[65] K. Kiminami, A. Hirata, and T. Shiozawa, "Double-sided printed bow-tie antenna for UWB communications," *IEEE Antennas and Wireless Propagation Letters*, vol. 3, no. 9, pp. 152–153, 2004.

[66] E. Staderini, "An UWB radar based stealthy lie detector." [Online]. Available: www.hrvcongress.org/second/first/placed_3/Staderini_Art_Eng.pdf

[67] T. Zasowski, F. Althaus, M. Stager, A. Wittneben, and G. Troster, "UWB for noninvasive wireless body area networks: channel measurements and results," in *IEEE Conference on Ultra Wideband Systems and Technologies*, Reston, VA, Nov. 2003, pp. 285–289.

[68] K. Marsden, H. J. Lee, D. S. Ha, and H. S. Lee, "Low power CMOS re-programmable pulse generator for UWB systems," in *IEEE Conference on Ultra Wideband Systems and Technologies*, Reston, VA, Nov. 2003, pp. 443–447.

[69] M. I. Skolnik, *Radar Handbook*. McGraw Hill Book Company, 1970.

[70] T. E. Kolding, "On-wafer calibration techniques for Giga-Hertz CMOS measurements," in *IEEE International Conference on Microelectronic Test Structures*, IEEE, Ed., Goteborg, Sweden, Mar. 1999, pp. 105–110.

[71] A. Bevilacqua and A. M. Nicknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6 GHz wireless receivers," *IEEE Journal of Solid State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[72] A. Ismail and A. A. Abidi, "A 3-10 GHz low noise amplifier with wideband LC-ladder matching network," *IEEE Journal of Solid State Circuits*, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.

[73] C.-F. Liao and S.-I. Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6 GHz UWB receivers," *IEEE Journal of Solid State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[74] Y.-J. E. Chen and Y.-I. Huang, "Development of integrated broad-band CMOS low-noise amplifiers," *IEEE Transaction on Circuits and Systems I*, vol. 54, no. 10, pp. 2120–2127, Oct. 2007.

[75] P. Heydari, "Design and analysis of a performance-optimized CMOS UWB distributed LNA," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1892–1904, Sep. 2007.

[76] K.-H. Chen, J.-H. Lu, B.-J. Chen, and S.-I. Liu, "An ultra-wide-band 0.4 10-GHz LNA in 0.18-um CMOS," *IEEE Transaction on Circuits and Systems II*, vol. 54, no. 3, pp. 217–221, Mar. 2008.

[77] F. Zito, "Generatore di impulsi UWB in tecnologia CMOS 90 nm per applicazioni wireless in biomedicina," Master's thesis, University "Mediterranea" of Reggio Calabria, Reggio Calabria, Italy, Nov. 2006.

[78] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford University Press.

[79] S. Bagga, A. V. Vorobyov, S. A. P. Haddad, A. G. Yarovoy, W. A. Serdijn, and J. R. Long, "Codesign of an impulse generator and miniaturized antennas for IR-UWB," *IEEE Transaction on Microwave Theory and Techniques*, vol. 54, no. 4, pp. 1656–1666, Apr. 2006.

[80] L. Stoica, A. Rabbachin, and I. Oppermann, "A low-complexity noncoherent IR-UWB transceiver architecture with TOA estimation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 4, pp. 1637–1646, Apr. 2006.

[81] T. Kikkawa, P. K. Saha, N. Sasaki, and K. Kimoto, "Gaussian monocycle pulse transmitter using 0.18 um CMOS technology with on-chip integrated antennas for inter-chip UWB communication," *IEEE Journal of Solid State Circuits*, vol. 43, no. 5, pp. 1303–1312, May 2008.

[82] L. Stoica, A. Rabbachin, H. Repo, S. Tiuraniemi, and I. Oppermann, "An ultra wideband system architecture for tag based wireless sensor networks," *IEEE Transactions on Vehicular Technology*, vol. 54, no. 5, pp. 1632–1645, Sep. 2005.

[83] M. Maymandi-Nejad and M. Sachdev, "A monotonic digitally controlled delay element," *IEEE Journal of Solid State Circuits*, vol. 40, no. 11, pp. 2212–219, Nov. 2005.

[84] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "Sige bipolar transceiver circuits operating at 60 GHz," *IEEE Journal of Solid State Circuits*, vol. 40, no. 1, pp. 156–167, Jan. 2005.

[85] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M.-T. Yang, P. Schvan, and S. P. Voinigescu, "Algoritmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE Journal of Solid State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[86] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE Journal of Solid State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[87] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.

[88] J. R. Long and M. A. Copeland, "A 1.9 GHz low-voltage silicon bipolar receiver front-end for wireless personal communication systems," *IEEE Journal of Solid State Circuits*, vol. 30, no. 12, pp. 1438–1448, Dec. 1995.

[89] M. T. Rehia and J. R. Long, "A 1.2V reactive-feedback 3.1-10.6 GHz low noise amplifier in 0.13 um CMOS," *IEEE Journal of Solid State Circuits*, vol. 42, no. 5, pp. 1023–1033, May 2007.

[90] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77 GHz phased-array transceiver with on-chip antennas in silicon: receiver and antennas," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[91] T. Dickson, M. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. Voinigescu, "30-100-GHz inductors and transformers for millimeter wave (Bi)CMOS integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 123–133, Jan. 2005.

[92] J. E. Post, "Optimizing the design of spiral inductors on silicon," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 1, pp. 15–17, Jan. 2000.

[93] O. El-Gharniti, E. Kerherve, and J.-B. Begueret, "Modeling and characterization of on-chip transformers for silicon RFIC," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 4, pp. 607–615, Apr. 2007.

List of Symbols and Abbreviations

Abbreviation	Description	Definition
ADS	Advanced Design System	page 9
BSI	Boot-Strapped Inductor	page 1
CW	continuous wave	page 25
CAD	computer aided design	page 34
EIRP	effective isotropic radiated power	page 2
EM	electro-magnetic	page 18
ESD	electro-static discharge	page 40
FCC	federal communications commission	page 25
Fig.	Figure	page 2
GPR	ground penetrating radar	page 25
ICP_{1dB}	input referred 1 dB compression point	page 7
IIP_3	input referred 3^{rd} order intercept point	page 8
ISM	industrial, scientific and medical	page 2
LNA	low noise amplifier	page 4
LO	local oscillation	page 12
NFmin	minimum noise figure	page 7
OCP_{1dB}	output referred 1 dB compression point	page 10
PA	power amplifier	page 9
PAE	power-added efficiency	page 10
PGS	patterned ground shield	page 66
PLL	phase locked loop	page 12
PN	phase noise	page 12
PLS	post-layout simulation	page 40
PSD	power spectral density	page 25
PRF	pulse repetition frequency	page 29
Q	quality factor	page 1
QPSK	quadrature phase shift keying	page 9
RFIC	radio-frequency integrated circuits	page 18
RFID	radio-frequency identification device	page 1
tag	active transponder	page 1
SNR	signal-to-noise-ratio	page 28
SoaC	system-on-a-chip	page 25
TIIMCA	transformer-based input integrated matching in cascode amplifiers	page 71
UWB	ultra-wideband	page 25

Abbreviation	Description	Definition
VCO	voltage controlled oscillator	page 1
VNA	vector network analyzer	page 32
WBAN	wireless body area network	page 25
WLAN	wireless local area network	page 1
WPAN	personal wireless area network	page 68

List of Figures

List of Tables

Index